

# DDR4 Gets a new Testing Document via JEDEC and FuturePlus Systems

## *Protocol Checks Standardization Leads To Quality Implementations*

June 5th, 2017 Bedford NH: JEDEC, the organization that writes the worlds memory standards, today announced the publication of a new testing document related to the DDR4 Memory Standard.

- This is the first time JEDEC has produced a document that spells out various protocol checks for the DDR4 Memory Standard
- FuturePlus Systems was the main sponsor for this effort that lasted 2 ½ years
- Server, Test and Measurement and Simulation Verification companies participated in the Review

Cloud Computing is pervasive in our society today and DDR Memory is at the heart of every Server. Ensuring proper testing and verification of the DDR4 protocol is key to ensuring that the data will not be corrupted. “As critical applications become more and more cloud based, the industry must address Server Memory Quality Testing”, explained JEDEC Technical Working Group Member Barbara Aichinger, Vice President of FuturePlus Systems. “ We worked hard to get the various industry stake holders to agree on the contents of this document”

FuturePlus Systems offers a Compliance Audit for Server Memory Channels and DIMMs. This testing includes electrical, protocol, SPD check, Row Hammer, Performance and Mode Register Settings. For more information visit [Memory Channel Validation](#) and [DIMM/SODIMM Validation Testing](#).

**About FuturePlus Systems:** FuturePlus Systems has been a key player in the growth of the computer industry over the last 25 years. Its tools in memory and display technologies are used by engineers all over the world. FuturePlus Systems is a Strategic Solutions Partner to Keysight Technologies and its predecessors Agilent Technologies and Hewlett-Packard for over 20 years. The company is also a member of the Tektronix Embedded Tools Partner program. Learn More about FuturePlus Systems [here](#) and the DDR Detective [here](#).

Press Contact: Barbara Aichinger  
FuturePlus Systems Corporation  
Barb.Aichinger@FuturePlus .com  
603-472-5905

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