Keysight Digital BGA Interposer Catalog

Keysight Technologies provides a range of Ball Grid Array (BGA) interposers, optimized for oscilloscope or logic analyzer measurements, that enable accurate testing directly at the ball grid array of memory/ processor systems

March 2020

KEYSIGHT TECHNOLOGIES

Memory System Validation

Keysight Technologies has the measurement tools you need to validate the very latest memory technologies. These include logic analyzers, oscilloscopes and software for automated compliance, decode, and protocol checking.

To complement our high speed digital instruments and software, Keysight offers probing solutions with a comprehensive range of Ball Grid Array (BGA) interposers. When positioned between the processor memory controller and the memory device, the interposers allow you to make signal quality or protocol measurements with minimal effect on the system-under-test.

Memory technology is constantly advancing in speed and density, and you need probing solutions that keep up with these developments. Keysight Technologies is at the forefront of the latest memory standards, chip technologies, and measurement techniques. Your Keysight Applications Engineer and Keysight's Interposer Design Team can assist you with selecting the best BGA interposer and probing technique for your application.

You can choose from a large selection of existing interposer designs, or define probing solutions customized to your specific needs. Keysight's standard interposers are available for several JEDEC standard packages with a variety of ball counts. The selection guide in this catalog gives you an overview of the interposers available and provides links to the corresponding data sheets. For additional DRAM packages or to meet different mechanical requirements, Keysight's proven development process can produce custom BGA interposer designs of the highest quality.

Browse the catalog and then contact your local Keysight Applications Engineer for advice on the right products and measurement techniques to ensure the successful validation of your memory system.

Mark Schnaible
Applications EngineeringManager
Keysight Technologies

Selection Guide

Interposers optimized for Oscilloscope Measurements	JEDEC Standard	Pin Count
DDR5 78 BGA Signal Integrity Interposer	JESD209-5	78
LPDDR3 178 BGA Signal Integrity Interposer	JESD209-3B	178
LPDDR4 200 BGA Signal Integrity Interposer	JDSD209-4A	200
LPDDR3 253 BGA Signal Integrity Interposer	JESD209-3B	253
GDDR5 170 BGA Signal Integrity Interposer	JESD212B.01	170

Interposers optimized for Logic Analyzer Measurements	JEDEC Standard	Pin Count
LPDDR2 121 BGA Interposer	JESD209-2F	121
eMMC 153 or 169 NAND BGA Logic Analyzer Interposer	JESD84-B50 eMMC	153 or 169
LPDDR2/3 168 BGA Logic Analyzer Interposer	JESD209-2F & JESD209-3B	168
LPDDR4 200 BGA Logic Analyzer Interposer	JDSD209-4A	200
LPDDR3 253 BGA Logic Analyzer Interposer	JESD209-3B	253
LPDDR4 366 BGA Logic Analyzer Interposer	-	366
DDR4 x16 BGA Interposer Cable Adapter	JESD79-4	96

See www.keysight.com for information on other DDR2, DDR3, and DDR4 BGA interposers.

DDR5 78

BGA Signal Integrity Interposer

Probes JESD209-5, 78 ball DDR5 memory devices

Signals Probed

	1	2	3	4	5	6	7	8	9	
A	LBDQ	GND	VPP				ZQ	GND	LBDQS	A
B	VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	B
C	GND	DQ0	DQS_t				DM_n TDQS_t	DQ1	GND	C
D	VDDQ	GND	DQS_c				TDQS_c	GND	VDDQ	D
E	VDD	DQ4	DQ6				DQ7	DQ5	VDD	E
F	GND	VDDQ	GND				GND	VDDQ	GND	F
G	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	G
H	ALERT_n	GND	CS_n				CK_c	GND	VDD	H
J	VDDQ	CA4	CA0				CA1	CA5	VDDQ	J
K	VDD	CA6	CA2				CA3	CA7	VDD	K
L	VDDQ	GND	CA8				CA9	GND	VDDQ	L
M	CAI	CA10	CA12				CA13	CA11	RESET_n	M
N	VDD	GND	VDD				VPP	GND	VDD	N
	1	2	3	4	5	6	7	8	9	

The DDR5 Interposer provides access to the signals highlighted below and passes all power and ground signals between the system and the memory chip. Separate power planes and power filter capacitor locations are used for VDD and VDDQ power rails.

Key Features

- The DDR5 High Performance Signal Integrity Interposer is a rigid, 78 ball, DDR5, BGA interposer, optimized for oscilloscope use. This interposer is designed to support DDR5- 4800 with single channel, x8 DRAM chips.
- Probes a 78 ball DDR5 x8 DRAM chip, JESD209-5 footprint variation MO-207 DT-z, with a maximum chip package size of 9 x 12 mm.
- For tight keep-out volume applications, a DDR5 High Performance Riser is included in the DDR5 High Performance Signal Integrity Interposer Kit

Selection Guide

Specifications

JEDEC Standard:
JESD209-5

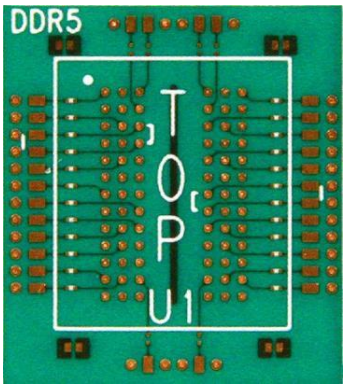
Ball Count:
78

DRAM Size:
9 mm x 12 mm

Configuration:
Single channel x8 DRAM
(JESD209-5 footprint variation
MO-207 DT-z)

Interposer size:
18.0 mm x 16.0 mm nominal

Connectors:
Solder-down test points and solder balls on bottom



KEYSIGHT TECHNOLOGIES

LPDDR3 178

BGA Signal Integrity Interposer

Probes JESD209-3B, 178 ball LPDDR3 memory devices

Selection Guide

Signals Probed

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU
B	DNU	GND	ZQ0	ZQ1	GND	GND		DQ31	DQ30	DQ29	DQ28	GND	DNU
C		CA9	GND	NC	GND	GND		DQ27	DQ26	DQ25	DQ24	VDDQ	
D		CA8	GND	VDD2	VDD2	VDD2		DM3	DQ15	DQS3_t	DQS3_c	GND	
E		CA7	CA6	GND	GND	GND		VDDQ	DQ14	DQ13	DQ12	VDDQ	
F		VDDCA	CA5	GND	GND	GND		DQ11	DQ10	DQ9	DQ8	GND	
G		VDDCA	GND	GND	VDD2	GND		DM1	GND	DQS1_t	DQS1_c	VDDQ	
H		GND	VDDCA	VrefCA	VDD2	VDD2		VDDQ	VDDQ	GND	VDDQ	VDD2	
J		CK_c	CK_t	GND	VDD2	VDD2		ODT	VDDQ	VDDQ	VrefDQ	GND	
K		GND	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	GND	VDDQ	VDD2	
L		VDDCA	CS0_n	CS1_n	VDD2	GND		DM0	GND	DQS0_t	DQS0_c	VDDQ	
M		VDDCA	CA4	GND	GND	GND		DQ4	DQ5	DQ6	DQ7	GND	
N		CA2	CA3	GND	GND	GND		VDDQ	DQ1	DQ2	DQ3	VDDQ	
P		CA1	GND	VDD2	VDD2	VDD2		DM2	DQ0	DQS2_t	DQS2_c	GND	
R		CA0	NC	GND	GND	GND		DQ20	DQ21	DQ22	DQ23	VDDQ	
T	DNU	GND	GND	GND	GND	GND		DQ16	DQ17	DQ18	DQ19	GND	DNU
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU

The LPDDR3 178 BGA Interposer is optimized for oscilloscope measurements. It provides access to the LPDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the LPDDR interface while providing access to selected bus signals between the processor and LPDDR memory chip.
- Provides solder pads for use with Keysight E2677A or N5381A InfiniiMax single-ended/differential solder-in or Keysight N5425A ZIF probe head.
- Includes S parameter file to configure the oscilloscope to render waveforms as they exist at the DRAM pins.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 11.5 mm x 11 mm.
- For dimensional drawings see final page.

Specifications

JEDEC Standard:
JESD209-3B

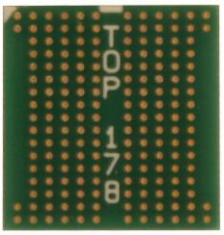
Ball Count:
178

DRAM Size:
11.5 mm x 11 mm

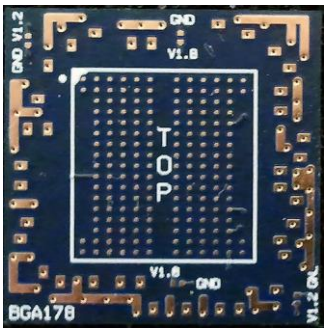
Configuration:
Single channel x32 DRAM (JEDEC MO-311A footprint)

Interposer size, pitch:
19 mm x 19 mm nominal, 0.8 mm x 0.65 mm

Connectors:
Solder-down test points and solder balls



LPDDR3 178 Ball Riser



KEYSIGHT TECHNOLOGIES

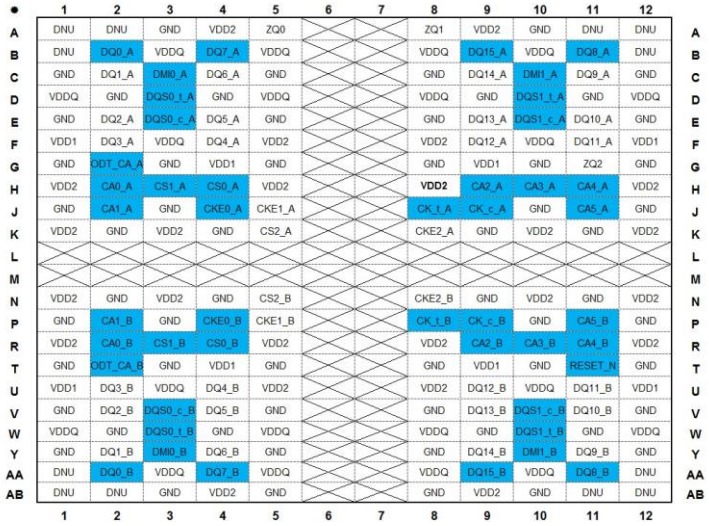
LPDDR4 200

BGA Signal Integrity Interposer

Probes JESD209-4A, 200 ball LPDDR4 memory devices

Selection Guide

Signals Probed



	1	2	3	4	5	6	7	8	9	10	11	12	
A	DNU	DNU	GND	VDD2	ZQ0			ZQ1	VDD2	GND	DNU	DNU	A
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU	B
C	GND	DQ1_A	DMI0_A	DQ6_A	GND			GND	DQ14_A	DMI1_A	DQ9_A	GND	C
D	VDDQ	GND	DQS0_t_A	GND	VDDQ			VDDQ	GND	DQS1_t_A	GND	VDDQ	D
E	GND	DQ2_A	DQS0_c_A	DQ5_A	GND			GND	DQ13_A	DQS1_c_A	DQ10_A	GND	E
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1	F
G	GND	ODT_CA_A	GND	VDD1	GND			GND	VDD1	GND	ZQ2	GND	G
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2	H
J	GND	CA1_A	GND	CKE0_A	CKE1_A			CK_t_A	CK_c_A	GND	CA5_A	GND	J
K	VDD2	GND	VDD2	GND	CS2_A			CKE2_A	GND	VDD2	GND	VDD2	K
L													L
M													M
N	VDD2	GND	VDD2	GND	CS2_B			CKE2_B	GND	VDD2	GND	VDD2	N
P	GND	CA1_B	GND	CKE0_B	CKE1_B			CK_t_B	CK_c_B	GND	CA5_B	GND	P
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2	R
T	GND	ODT_CA_B	GND	VDD1	GND			GND	VDD1	GND	RESET_N	GND	T
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1	U
V	GND	DQ2_B	DQS0_c_B	DQ5_B	GND			GND	DQ13_B	DQS1_c_B	DQ10_B	GND	V
W	VDDQ	GND	DQS0_t_B	GND	VDDQ			VDDQ	GND	DQS1_t_B	GND	VDDQ	W
Y	GND	DQ1_B	DMI0_B	DQ6_B	GND			GND	DQ14_B	DMI1_B	DQ9_B	GND	Y
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU	AA
AB	DNU	DNU	GND	VDD2	GND			GND	VDD2	GND	DNU	DNU	AB
	1	2	3	4	5	6	7	8	9	10	11	12	

The LPDDR4 200 BGA Signal Integrity Interposer is optimized for oscilloscope measurements. It provides access to LPDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the LPDDR interface while providing access to selected signals between the processor and LPDDR4 memory chip.
- Provides solder-down test pads with plated-through-holes that connect to Keysight E2677A or N5381A solder-in probe heads, or N5425A ZIF probe tip.
- Includes S-parameter file to configure the oscilloscope to render waveforms as they exist at the DRAMpins.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 10x15mm.
- For dimensional drawings see final page.

Specifications

JEDEC Standard:
JDSD209-4A

Ball Count:
200

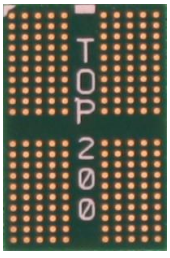
DRAM Size:
10 mm x 15 mm

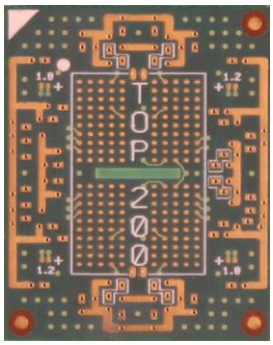
Pitch:
0.8 mm x 0.65 mm

Configuration:
Dual channel x16 DRAM (JEDEC MO-311 footprint)

Interposer Size:
20 mm x 25 mm,

Connectors:
Solder-down test points and solder balls on bottom





KEYSIGHT TECHNOLOGIES

LPDDR3 253

BGA Signal Integrity Interposer

Probes JESD209-3B, 253 ball LPDDR3 memory devices

Selection Guide

Signals Probed

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	NC	GND	GND	GND	GND	VDDCA	VDD2	GND	VDDCA	VrefCAa	VDD2	GND	VDDQ	GND	VDD1	VDD1	NC
B	GND	VDD1	GND	GND	CA0a	CA3a	CS1na	CKta	VDDCA	CA7a	ZQ0a	VDDQ	DQ28b	DQ29b	DQ30b	DQ31b	VDD2
C	GND	GND	VDD2	GND	CA1a	CA4a	CKE0a	CKca	CA5a	CA8a	ZQ1a	VDDQ	DQ24b	DQ25b	DQ26b	DQ27b	VDD2
D	GND	GND	GND	GND	CA2a	CS0na	CKE1a	RFU	CA6a	CA9a	RFU	GND	DQ15b	DM3b	DQS3cb	DQS3tb	GND
E	VDDCA	ZQ0b	ZQ1b	RFU	GND	GND	GND	GND	GND	GND	GND	GND	DQ11b	DQ12b	DQ13b	DQ14b	VDDQ
F	GND	CA7b	CA8b	CA9b	GND							GND	DM1b	DQ8b	DQ9b	DQ10b	GND
G	GND	VDDCA	CA5b	CA6b	GND							VDDQ	DQS1cb	DQS1tb	GND	GND	VDDQ
H	VDD2	CKcb	CKtb	RFU	GND							GND	ODTb	DM0b	GND	VDD2	VrefDQb
J	VrefCAb	CS1nb	CKE0b	CKE1b	GND							RFU	DQS0cb	DQS0tb	DQ6b	DQ7b	GND
K	VDDCA	CA3b	CA4b	CS0nb	GND							VDDQ	DQ2b	DQ3b	DQ4b	DQ5b	VDDQ
L	VDD2	CA0b	CA1b	CA2b	GND							GND	DQ23b	DM2b	DQ0b	DQ1b	VDDQ
M	GND	VDDQ	VDDQ	GND	GND	GND	VDDQ	GND	RFU	VDDQ	GND	VDDQ	DQ21b	DQ22b	DQS2cb	DQS2tb	GND
N	VDDQ	DQ19a	DQ23a	DQ0a	DQ4a	DM0a	DQS0ca	ODTa	DQS1ca	DQ13a	DQ24a	DQ25a	GND	DQ18b	DQ19b	DQ20b	GND
P	GND	DQ18a	DQ22a	DM2a	DQ3a	DQ7a	DQS0ta	DM1a	DQS1ta	DQ12a	DM3a	DQ26a	DQ29a	GND	DQ16b	DQ17b	VDDQ
R	VDD1	DQ17a	DQ21a	DQS2ca	DQ2a	DQ6a	GND	GND	DQ9a	DQ11a	DQ15a	DQS3ca	DQ28a	DQ31a	VDD2	GND	GND
T	VDD1	DQ16a	DQ20a	DQS2ta	DQ1a	DQ5a	GND	VDD2	DQ8a	DQ10a	DQ14a	DQS3ta	DQ27a	DQ30a	GND	VDD1	GND
U	NC	VDD2	VDD2	GND	VDDQ	GND	VDDQ	VrefDQa	GND	VDDQ	VDDQ	GND	GND	VDDQ	GND	GND	NC

LPDDR3 BGA253 2-Channel x32
11.0x11.5 mm, 0.5 mm pitch
17 rows x 17 columns

The LPDDR3 253 BGA Interposer is optimized for oscilloscope measurements. It provides access to the LPDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the LPDDR interface while providing access to selected bus signals between the processor and LPDDR memory chip.
- Provides solder pads for use with Keysight E2677A or N5381A InfiniiMax single-ended/differential solder-in, or Keysight N5425A ZIF probe head.
- Includes S parameter file to configure the oscilloscope to render waveforms as they exist at the DRAM pins.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 11x11.5 mm.
- For dimensional drawings see final page.

LPDDR3 253 Ball Riser

Specifications

JEDEC Standard:
JESD209-3B

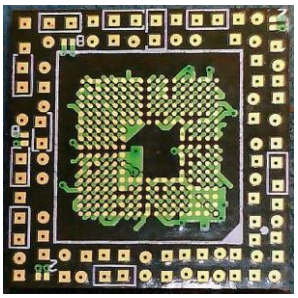
Ball Count:
253

DRAM Size:
11 mm x 11.5 mm

Configuration:
Dual channel x32 RAM (JEDEC MO-276 footprint)

Interposer size, pitch:
16.7 x 16.9 mm nominal, 0.5 mm

Connectors:
Solder-down test points and solder balls



KEYSIGHT TECHNOLOGIES

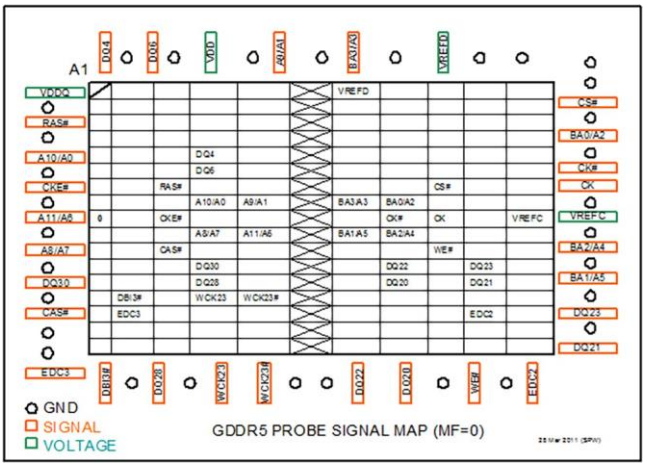
GDDR5 170

BGA Signal Integrity Interposer

Probes embedded GDDR memory devices

Selection Guide

Signals Probed



The GDDR5 170 BGA Interposer is optimized for oscilloscope measurements. It provides access to the GDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the GDDR5 interface while providing access to selected bus signals between the processor and LPDDR memory chip.
- Provides solder pads for use with Keysight E2677A or N5381A InfiniiMax single-ended/differential solder-in or Keysight N5425A ZIF probe head.
- Includes S parameter file to configure the oscilloscope to render waveforms as they exist at the DRAM pins.

Specifications

JEDEC Standard:
JESD212B.01

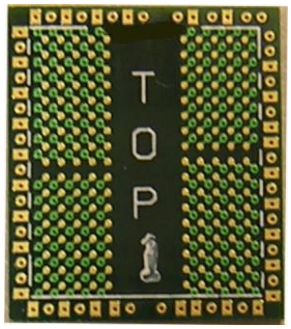
Ball Count:
170

DRAM Size:
12 mm x 14 mm

Configuration:
Embedded GDDR

Interposer size, pitch:
14.2 x 16.4 mm nominal, 0.8 mm

Connectors:
Solder-down test points and solder balls



KEYSIGHT TECHNOLOGIES

Information subject to change

LPDDR2 121

BGA Interposer

Probes JESD209-2F, 121 ball LPDDR2 memory devices

Selection Guide

Signals Probed

	1	2	3	4	5	6	7	8	9	10	11
A	DNU	DNU	NC	NC	NC	NC	VDD2	NC	NC	DNU	DNU
B	DNU	NC	NC	NC	NC	NC	VDD1	DQ15	DQ14	GND	DNU
C	NC	NC	NC		NC	NC	NC		DQ11	DQ12	DQ13
D	VDD2	NC								DQ10	GND
E	GND	ZQ	CA9						DQ8	DQ9	VDDQ
F	VDD1	CA8			NC	NC	NC			DQS1_t	GND
G	GND	CA7	CA6		NC	NC	NC		DQS1_c	DM1	VDDQ
H	VDDCA	CA5			NC	NC	NC			VrefDQ	VDD2
J	VDD2	VrefCA	GND		NC	NC	NC		DQS0_c	DM0	VDD1
K	CK_t	CK_c			NC	NC	NC			DQS0_t	VDDQ
L	CS0_n	CS1_n	NC						DQ7	DQ6	GND
M	CA4	CA3								DQ5	VDDQ
N	VDDCA	CA2	CA1		CKE0	NC	NC		DQ3	DQ2	GND
P	DNU	GND	CA0	NC	CKE1	VACC	DQ0	DQ1	DQ4	GND	DNU
R	DNU	DNU	GND	VDDQa	VDD1	GND	VDD2	GND	VDDQ	DNU	DNU

The LPDDR2 121 BGA Interposer is optimized for logic analyzer measurements and can also be used for oscilloscope measurements. It provides access to the LPDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the LPDDR interface while providing access to selected bus signals between the processor and LPDDR memory chip.
- Rigid/flex probe can be soldered in place or used with a BGA socket.
- Logic Analyzer measurements require one modified Keysight E5845A adapter cable (sold separately) to access CKE signals.
- Oscilloscope measurements require two Keysight W3635B scope probe adapters (sold separately).

Specifications

JEDEC Standard:
JESD209-2F

Ball Count:
121

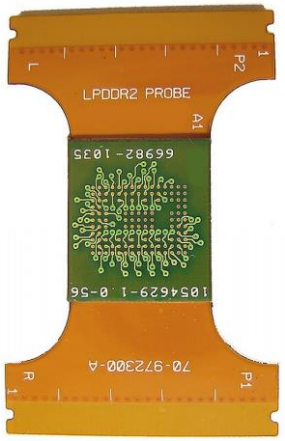
DRAM Size:
10 mm x 11 mm

Configuration:
Single channel, x16 RAM

Interposer size, pitch:
33.4 mm x 21 mm, (Rigid portion 12.5 mm x 11 mm), 0.5mm

Connectors:
Zero Insertion Force (ZIF)

E5845A Adapter Cable



KEYSIGHT TECHNOLOGIES

eMMC 153 or 169 NAND

BGA Logic Analyzer Interposer

Probes ONFI NAND 153 or 169 ball memory devices

Selection Guide

Signals Probed

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	RFU	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDD	NC	GND	RFU	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	VCC	GND	RFU	RFU	RFU		NC	NC	NC	E
F	NC	NC	NC		VCC					RFU		NC	NC	NC	F
G	NC	NC	RFU		GND					RFU		NC	NC	NC	G
H	NC	NC	NC		DSTRB					GND		NC	NC	NC	H
J	NC	NC	NC		RFU					VCC		NC	NC	NC	J
K	NC	NC	NC		RSTN	RFU	RFU	GND	VCC	RFU		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	GND	NC	VCCQ	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	GND	VCCQ	GND	RFU	NC	NC	RFU	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

The eMMC 153 ball Logic Analyzer Interposer is optimized for protocol measurements with a Keysight logic analyzer. It provides access to the highlighted signals and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the eMMC interface while providing access to selected signals between the processor and memory chip.
- Rigid-flex-rigid structure with one Soft Touch Pro connector. Requires one E5406A cable (sold separately) to connect to the logic analyzer.
- Includes configuration file for set up of the logic analyzer.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 12 mm x13 mm.
- For dimensional drawings see final page.

Specifications

JEDEC Standard:
JESD84-B50 eMMC

Ball Count:
153 or 169

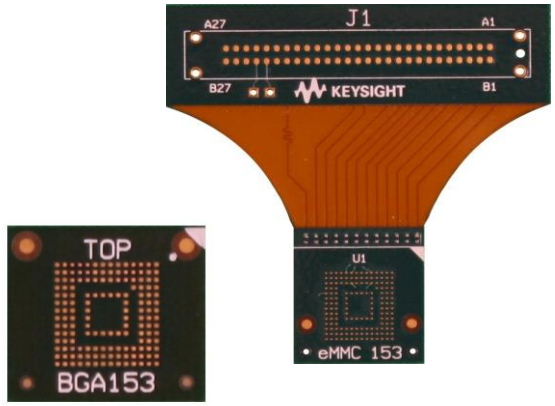
DRAM Size:
11.5 mm x 13 mm

Pitch:
0.5 mm

Configuration:
Single channel (JEDEC MO-276 footprint)

Interposer Size (rigid portion):
13 mm x 13.5 mm

Connectors:
Single Soft Touch Pro



eMMC 153 Ball Riser

KEYSIGHT TECHNOLOGIES

LPDDR2/3 168

BGA Logic Analyzer Interposer

Probes JESD209-2F and JESD209-3B, 168 ball LPDDR2/3 memory devices

Selection Guide

Signals Probed

●	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDD1	GND	DQ30	DQ29	GND	DQ26	DQ25	GND	DQS3n	VDD1	GND	NC	NC
B	NC	NC	VDD1	NC	NC	NC	NC	NC	NC	GND	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3	VDDQ	DM3	VDD2	NC	NC
C	GND	VDD2																				DQ15	GND
D	NC	NC																				VDDQ	DQ14
E	NC	NC																				DQ12	DQ13
F	NC	NC																				DQ11	GND
G	NC	NC																				VDDQ	DQ10
H	NC	NC																				DQ8	DQ9
J	NC	NC																				DQS1	GND
K	NC	NC																				VDDQ	DQS1n
L	NC	NC																				VDD2	DM1
M	NC	GND																				VrefDQ	GND
N	NC	VDD1																				VDD1	DM0
P	ZQ0	VrefCA																				DQS0n	GND
R	GND	VDD2																				VDDQ	DQS0
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	GND
V	GND	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CKn	CK																				DQ1	GND
AA	GND	VDD2																				VDDQ	DQ0
AB	NC	NC	CS0n	CS1n	VDD1	CA1	GND	CA3	CA4	VDD2	GND	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2	VDDQ	DM2	VDD2	NC	NC
AC	NC	NC	CKE0	CKE1	GND	CA0	CA2	VDDCA	NC	NC	ZQ1	GND	DQ17	DQ19	GND	DQ21	DQ23	GND	DQS2n	VDD1	GND	NC	NC

BGA168 LPDDR2-3 PoP Probe
12 X 12 mm, 0.5 mm pitch
23 rows x 23 columns

The LPDDR2/3 168 BGA Interposer is optimized for logic analyzer measurements. It provides access to the LPDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Provides access to memory address, control, and data bus signals between a processor and LPDDR memory chip.
- Enables correct operation of the LPDDR interface while being probed with (2) Keysight U4154A logic analyzer modules.
- Riser of 1.2 mm height is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 12 mm x 12 mm.
- For dimensional drawings see final page.

Specifications

JEDEC Standard:
JESD209-2F & JESD209-3B

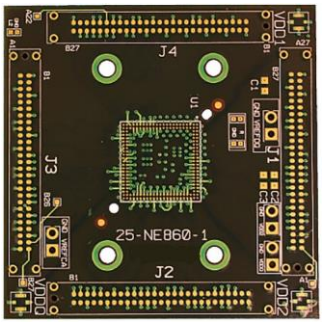
Ball Count:
168

DRAM Size:
12 mm x 12 mm

Configuration:
Single channel, x32 RAM chip (JEDEC drawing MO-273 package xCCBxB)

Interposer size, pitch:
47 mm x 47 mm, 0.5 mm

Connectors:
Industry standard connector-less footprint (Soft Touch Pro)



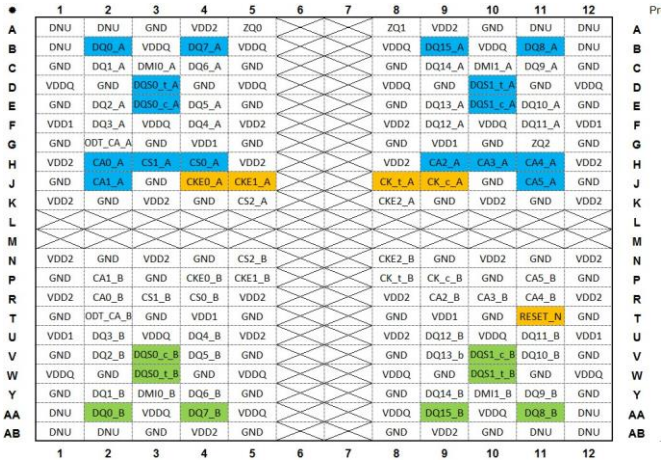
KEYSIGHT TECHNOLOGIES

LPDDR4 200

BGA Logic Analyzer Interposer

Probes JESD209-4A, LPDDR4 200 ball memory devices

Signals Probed



	1	2	3	4	5	6	7	8	9	10	11	12	
A	DNU	DNU	GND	VDD2	ZQ0			ZQ1	VDD2	GND	DNU	DNU	A
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU	B
C	GND	DQ1_A	DMI0_A	DQ6_A	GND			GND	DQ14_A	DMI1_A	DQ9_A	GND	C
D	VDDQ	GND	DQS0_t_A	GND	VDDQ			VDDQ	GND	DQS1_t_A	GND	VDDQ	D
E	GND	DQ2_A	DQS0_c_A	DQ5_A	GND			GND	DQ13_A	DQS1_c_A	DQ10_A	GND	E
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1	F
G	GND	ODT_CA_A	GND	VDD1	GND			GND	VDD1	GND	ZQ2	GND	G
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2	H
J	GND	CA1_A	GND	CKE0_A	CKE1_A			CK_t_A	CK_c_A	GND	CA5_A	GND	J
K	VDD2	GND	VDD2	GND	CS2_A			CKE2_A	GND	VDD2	GND	VDD2	K
L													L
M													M
N	VDD2	GND	VDD2	GND	CS2_B			CKE2_B	GND	VDD2	GND	VDD2	N
P	GND	CA1_B	GND	CKE0_B	CKE1_B			CK_t_B	CK_c_B	GND	CA5_B	GND	P
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2	R
T	GND	ODT_CA_B	GND	VDD1	GND			GND	VDD1	GND	RESET_N	GND	T
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1	U
V	GND	DQ2_B	DQS0_c_B	DQ5_B	GND			GND	DQ13_b	DQS1_c_B	DQ10_B	GND	V
W	VDDQ	GND	DQS0_t_B	GND	VDDQ			VDDQ	GND	DQS1_t_B	GND	VDDQ	W
Y	GND	DQ1_B	DMI0_B	DQ6_B	GND			GND	DQ14_B	DMI1_B	DQ9_B	GND	Y
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU	AA
AB	DNU	DNU	GND	VDD2	GND			GND	VDD2	GND	DNU	DNU	AB
	1	2	3	4	5	6	7	8	9	10	11	12	

The LPDDR4 200 BGA Logic Analyzer Interposer is optimized for protocol measurements with a Keysight logic analyzer. It provides access to the highlighted LPDDR signals and passes all power and ground signals between the processor and the memory chip.

Key Features

- Enables correct operation of the LPDDR interface while providing access to selected signals between the processor and LPDDR4 memory chip. Probes a single clock to support single data channel operation.
- Rigid-flex-rigid structure with one Soft Touch Pro connector. Requires one modified E5406A cable (sold separately) to connect to the logic analyzer.
- Includes configuration file for set up of the logic analyzer.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 10x15 mm.
- For dimensional drawings see final page.

Selection Guide

Specifications

JEDEC Standard:
JDSD209-4A

Ball Count:
200

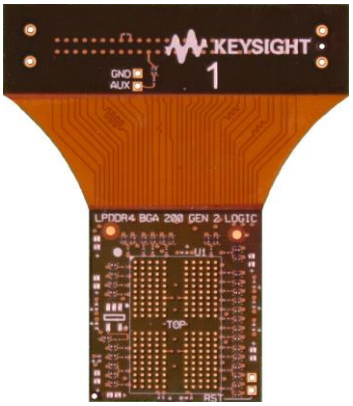
DRAM Size:
10 mm x 15 mm

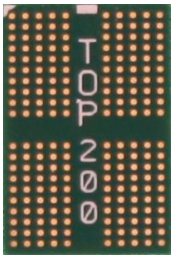
Pitch:
0.8 mm x 0.65 mm

Configuration:
Single channel x32 DRAM (JEDEC MO-311 footprint)

Interposer Size (rigid portion):
19 mm x 21 mm

Connectors:
Single Soft Touch Pro





LPDDR4 200 Ball Riser

KEYSIGHT TECHNOLOGIES

LPDDR3 253

BGA Logic Analyzer Interposer

Probes JESD209-3B, 253 ball LPDDR3 memory devices

Selection Guide

Signals Probed

•	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	NC	GND	GND	GND	GND	VDDCA	VDD2	GND	VDDCA	VrefCAa	VDD2	GND	VDDQ	GND	VDD1	VDD1	NC
B	GND	VDD1	GND	GND	CA0a	CA3a	CS1na	CKta	VDDCA	CA7a	ZQ0a	VDDQ	DQ28b	DQ29b	DQ30b	DQ31b	VDD2
C	GND	GND	VDD2	GND	CA1a	CA4a	CKE0a	CKca	CA5a	CA8a	ZQ1a	VDDQ	DQ24b	DQ25b	DQ26b	DQ27b	VDD2
D	GND	GND	GND	GND	CA2a	CS0na	CKE1a	RFU	CA6a	CA9a	RFU	GND	DQ15b	DM3b	DQS3cb	DQS3tb	GND
E	VDDCA	ZQ0b	ZQ1b	RFU	GND	GND	GND	GND	GND	GND	GND	GND	DQ11b	DQ12b	DQ13b	DQ14b	VDDQ
F	GND	CA7b	CA8b	CA9b	GND							GND	DM1b	DQ8b	DQ9b	DQ10b	GND
G	GND	VDDCA	CA5b	CA6b	GND							VDDQ	DQS1cb	DQS1tb	GND	GND	VDDQ
H	VDD2	CKcb	CKtb	RFU	GND							GND	ODTb	DM0b	GND	VDD2	VrefDQb
J	VrefCAb	CS1nb	CKE0b	CKE1b	GND							RFU	DQS0cb	DQS0tb	DQ6b	DQ7b	GND
K	VDDCA	CA3b	CA4b	CS0nb	GND							VDDQ	DQ2b	DQ3b	DQ4b	DQ5b	VDDQ
L	VDD2	CA0b	CA1b	CA2b	GND							GND	DQ23b	DM2b	DQ0b	DQ1b	VDDQ
M	GND	VDDQ	VDDQ	GND	GND	GND	VDDQ	GND	RFU	VDDQ	GND	VDDQ	DQ21b	DQ22b	DQS2cb	DQS2tb	GND
N	VDDQ	DQ19a	DQ23a	DQ0a	DQ4a	DM0a	DQS0ca	ODTa	DQS1ca	DQ13a	DQ24a	DQ25a	GND	DQ18b	DQ19b	DQ20b	GND
P	GND	DQ18a	DQ22a	DM2a	DQ3a	DQ7a	DQS0ta	DM1a	DQS1ta	DQ12a	DM3a	DQ26a	DQ29a	GND	DQ16b	DQ17b	VDDQ
R	VDD1	DQ17a	DQ21a	DQS2ca	DQ2a	DQ6a	GND	GND	DQ9a	DQ11a	DQ15a	DQS3ca	DQ28a	DQ31a	VDD2	GND	GND
T	VDD1	DQ16a	DQ20a	DQS2ta	DQ1a	DQ5a	GND	VDD2	DQ8a	DQ10a	DQ14a	DQS3ta	DQ27a	DQ30a	GND	VDD1	GND
U	NC	VDD2	VDD2	GND	VDDQ	GND	VDDQ	VrefDQa	GND	VDDQ	VDDQ	GND	GND	VDDQ	GND	GND	NC

LPDDR3 BGA253 2-Channel x32
11.0x11.5 mm, 0.5 mm pitch
17 rows x 17 columns

The LPDDR3 253 BGA Interposer is optimized for logic analyzer measurements. It provides access to the LPDDR signals highlighted and passes all power and ground signals between the processor and the memory chip.

Key Features

- Provides access to memory address, control, and data bus signals between a processor and LPDDR memory chip.
- Enables correct operation of the LPDDR interface while being probed with two Keysight U4154A logic analyzer modules.
- Rigid-flex-rigid structure with Soft Touch Pro (STP) connectors requires two modified E5406A cables (sold separately) for connection to the logic analyzer.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions: 11 mm x 11.5 mm.
- For dimensional drawings see final page.

Specifications

JEDEC Standard:
JESD209-3B

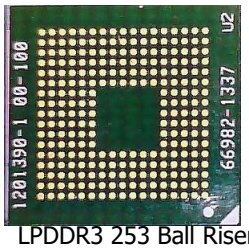
Ball Count:
253

DRAM Size:
11 mm x 11.5 mm

Configuration:
Dual channel x32 RAM (JEDEC MO-276 footprint)

Interposer size, pitch:
70 mm x 70 mm (Rigid Portion 26 mm x 26 mm), 0.5 mm

Connectors:
4 Soft Touch Pro Adapters



LPDDR3 253 Ball Riser

KEYSIGHT TECHNOLOGIES

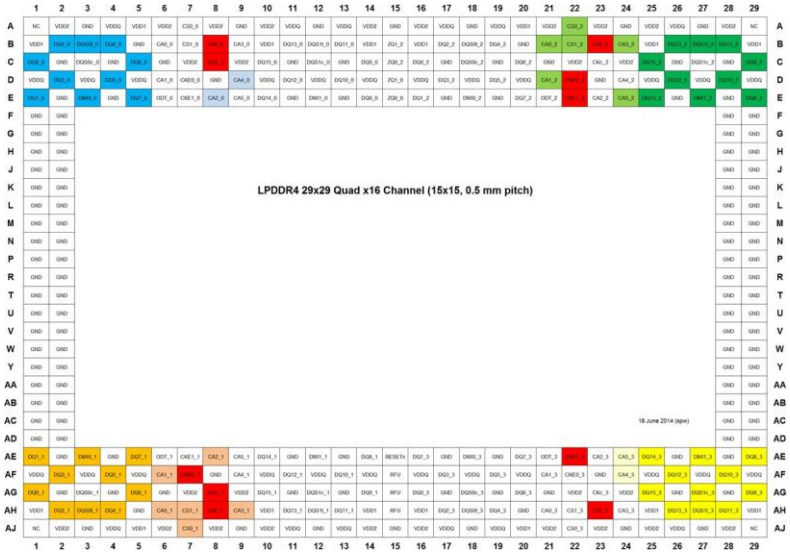
LPDDR4 366

BGA Logic Analyzer Interposer

Probes LPDDR4 366 ball memory devices

Selection Guide

Signals Probed



The LPDDR4 366 BGA Logic Analyzer Interposer is optimized for protocol measurements with a Keysight logic analyzer. It provides access to the highlighted LPDDR signals and passes all power and ground signals between the processor and the memory chip.

Key Features

– Enables correct operation of the LPDDR interface while providing access to selected address, control, and data bus signals between the processor and LPDDR4 memory chip.

– Rigid structure with four Soft Touch Pro connectors. Requires four modified E5406A cables (sold separately) to connect to the logic analyzer.

– Includes configuration file for set up of the logic analyzer.

– For dimensional drawings see final page.

Specifications

Ball Count:
366

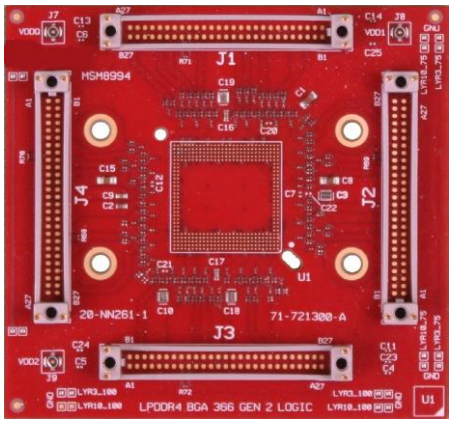
DRAM Size:
15 mm x 15 mm

Pitch:
0.5 mm

Configuration:
4 channel x16 DRAM

Interposer Size:
60 mm x 56 mm

Connectors:
Four Soft Touch Pro



KEYSIGHT TECHNOLOGIES

DDR4 x16

Cable Adapter

BGA Interposer ZIF to 90-pin Logic Analyzer Connector

Selection Guide

Signals Probed

	1	2	3	4	5	6	7	8	9	
A	VDDQ	GND	DQU0				DQSU_c	GND	VDDQ	A
B	VPP	GND	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	GND	C
D	VDD	GND	DQU6				DQU7	GND	VDDQ	D
E	GND	DMU_n	GND				DML_n	GND	GND	E
F	GND	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	GND	VDDQ	G
H	GND	DQL4	DQL2				DQL3	DQL5	GND	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	GND	CKE	ODT				CK_t	CK_c	GND	K
L	VDD	A14	ACT_n				CS_n	A16	VDD	L
M	VREFCA	BG0	A10				A12	A15	GND	M
N	GND	BA0	A4				A3	BA1	TEN	N
P	RST_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	GND	A11	PAR				NC	A13	VDD	T

The DDR4 x16 cable adapter, used with the Keysight W4631A DDR4 x16 4-wing BGA Interposer, provides access to DDR4 signals highlighted.

Key Features

- Logic analyzer cable used to connect Keysight U4154A logic analyzer module to Keysight W4631A DDR4 x16 4-wing BGA interposer.
- Enables all DDR4 x16 data traffic to be monitored using a single U4154A logic analyzer module.
- DDR4 x32 data can be monitored with: (2) W4631A DDR4 x16 BGA interposers, (2) DDR4 x16 cable adapters, and (2) U4154A logic analyzer modules.

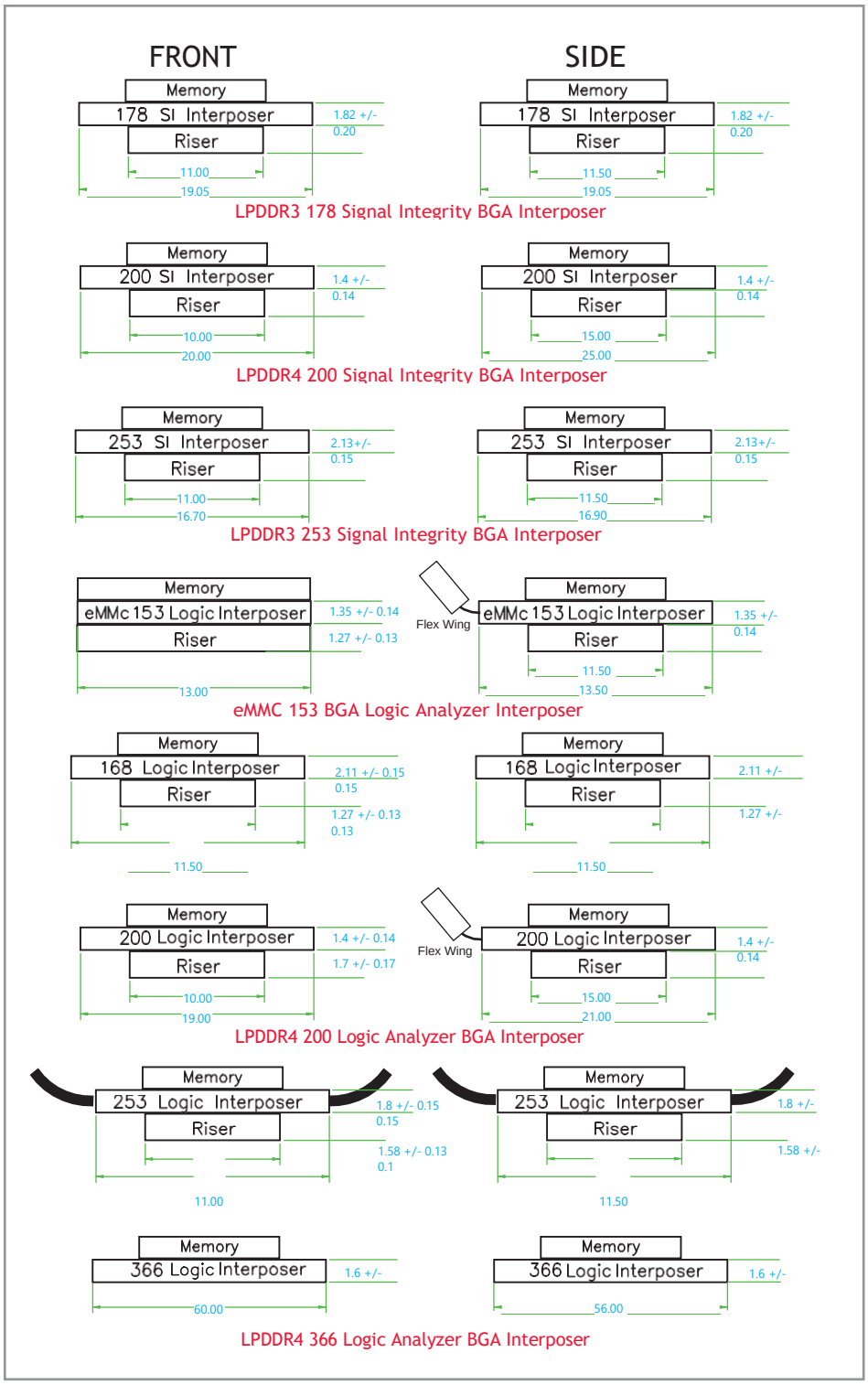
Specifications

Configuration:
DDR4 x16 DRAM (JEDEC MO-207 Variation DY-z footprint)

Connectors:
Four (4) Zero-Insertion Force (ZIF) to Five (5) 90-Pin Logic Analyzer pods

KEYSIGHT TECHNOLOGIES

Keysight Digital Interposers
Dimensional Drawings



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