

FOR IMMEDIATE RELEASE

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Boost DDR5 Debugging with 6400+ MT/s UDIMM & SODIMM Interposers

FuturePlus Systems, a leader in computer bus protocol analysis tools, proudly announces the release of two high-performance DDR5 interposers for CA Bus (Command/Address) signal analysis: the FS2611 DDR5 UDIMM Interposer and the FS2612 DDR5 SODIMM Interposer. These tools offer advanced capabilities for analyzing DDR5 memory traffic with speed, accuracy, and ease of use.

FS2611 DDR5 UDIMM Interposer: CA Bus Analysis at 6400+ MT/s

Designed for JEDEC-compliant DDR5 UDIMM and CUDIMM modules, the FS2611 enables comprehensive CA Bus visibility at speeds of 6400+ MT/s*. Supporting two Keysight U4164A logic analyzer modules, key features include:

- Passive, single-point probing for minimal signal intrusion and maximum signal eye margin
- Full CA Bus capture and decode across both CHA and CHB
- Clock Divider functionality for enhanced trace depth and analyzer performance
- Seamless integration with Keysight EyeScan (5 ps x 5 mV resolution)
- Built-in test pads for Sideband Bus probing with FS27x0 analyzers

The FS2611 is the ideal solution for engineers validating high-speed DDR5 systems at the UDIMM level.

FS2612 DDR5 SODIMM Interposer: CA Bus Analysis at 6400+ MT/s

The FS2612 supports DDR5 SODIMM and CSODIMM platforms, enabling CA Bus signal analysis at 6400+ MT/s*. Tailored for compact memory configurations, it features:

- Dual-channel CA Bus capture using two Keysight U4164A logic analyzers
- Passive single-point probing for high signal fidelity
- Clock Divider to double trace depth and improve analyzer efficiency
- Keysight EyeScan support for fast signal integrity diagnostics (5 ps x 5 mV resolution)
- Integrated test points for quick access to the Sideband Bus

The FS2612 is perfect for validating DDR5 SODIMM memory in laptops, embedded platforms, and small form factor systems.

Keysight's DDR5 State Analysis software supports both interposers and are fully compatible with the Keysight M9505A chassis and U4164A-02G modules.

For more information or to request a quote, visit www.FuturePlus.com or contact Protocol.Decode@FuturePlus.com.

*Performance operation is designed to, not specified or guaranteed.

FuturePlus Systems, LLC

9 Executive Park Drive, Suite 101

Merrimack, NH 03054 USA

Phone: +1 603 472-5905

About FuturePlus Systems

FuturePlus Systems is a leading provider of protocol analysis tools for the computer design industry. For over two decades, the company has delivered advanced interposer and software solutions that help engineers validate and debug high-speed memory and serial bus technologies, including DDR, DisplayPort, and more. FuturePlus products are used by system architects and validation engineers worldwide to accelerate time-to-market and ensure reliable system performance. To learn more, visit www.FuturePlus.com.