

Quick Review: DDR5 Interposer & Analyzer operation with clock divider

This quick reference explains how FuturePlus FS2611 and FS2612 slot interposers work with the Keysight U4164A logic analyzer to capture DDR5 command/address (CA) traffic while leaving data (DQ) untouched while using a clock divider.

Signals	What Interposer Adds	How System Compensates
DQ (Data)	Extra trace length	Controller training (write/read leveling, Vref, EQ) run with interposer installed
CA (Cmd/Addr)	Extra trace length	Timing centering run with interposer installed
CK (Clock)	Per-channel ÷2 clock sent only to analyzer. System DDR Clock (undivided) goes to the DUT in the extender card connector	Divider keeps analyzer clock ≤2.5 GHz while system still runs full speed

Fun Facts:

- DDR5 label speed (e.g., 8000 MT/s) always refers to DQ transfer rate.
- CA speed is full rate on RDIMM, half rate on UDIMM/SODIMM.
- CA and clock signals reach the DUT at full speed.
- Only the Clock signal is divided (per sub-channel) before reaching the analyzer.
- CA lines reach the analyzer at full speed for accurate capture.
- DQ lines are not probed; they pass through to the DUT.
- Normal DDR5 training by the memory controller compensates any extra delay added by the interposer.
- The U4164A is operated in Dual Sample Mode when using the clock divider
- The minimum eye size on the CA bus at the probe point on the interposer must be 100psx100mv
- So two variables must be met: DDR clock speed less than or equal to 5GHz AND minimum eye size of 100mvx100ps.

