FuturePlus® Systems

Power Tools for Bus Analysis

Quick-Start Guide

For Agilent 16700 and 16900 Series Logic Analyzers

FS4410 Serial RapidIO Analysis Probe

March 06, 2007

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sRIO State Analysis Probe - FS4410

1680/90 – 16800 - 16900 - Quick Start Instructions

It is strongly recommended that the user carefully follow the User Manual the first time the probe is used on a new sRIO link.

Step 1 Software Installation - **Refer to the User Manual** for the steps required to install the Protocol Decoder on the 16900 logic analyzer, load the Probe Manager software and required USB drivers on a Windows-based system, and also the Transaction Viewer software.

Step 2. Use the General Purpose Probe feature in the Overview section of the 16900 Logic Analyzer application to connect the logic analyzer cables to the FS4410 probe.

Step 3. Attach the probing cable, and the reference Cable if desired, to the probe and to the target system. Attach the USB cable from the probe to the PC where the Probe Manager application has been installed.

Step 4. Power up the logic analyzer, the PC where the Probe Manager application resides (if not on the 16900), the FS4410 probe, and the target system in this order.

Step 5. Open the FS4410-FS1134 folder on the desktop and load the logic analyzer with the appropriate configuration file.

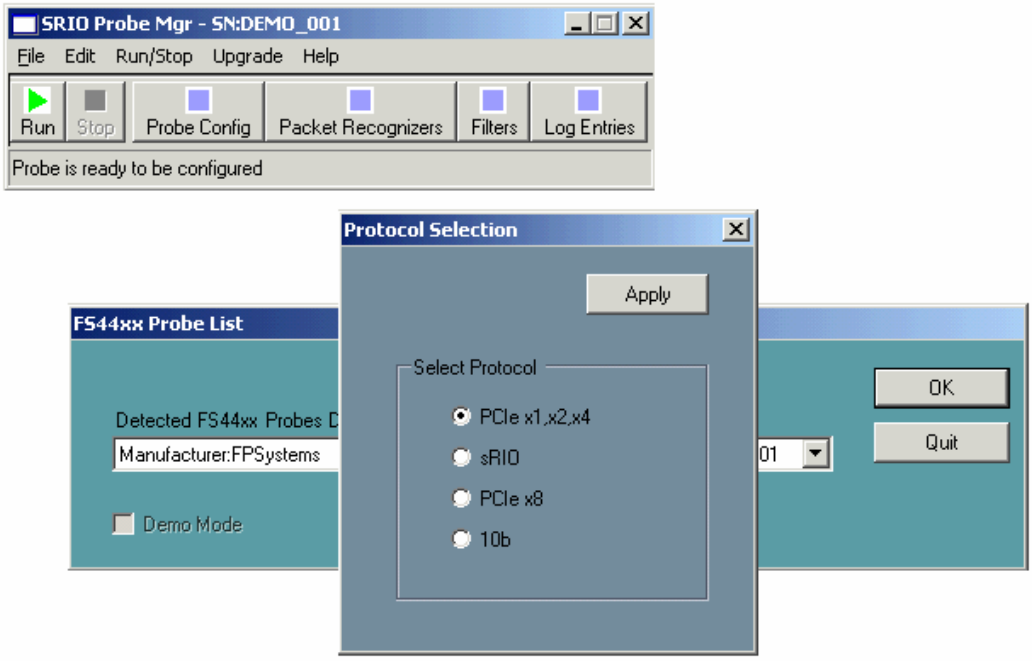
Configuration files for 8b mode only. Refer to the User Manual for 10b mode configuration files.

169xx Analyzer	X1 2 way any cable		X4 2 way using any cable					
	Any link speed		1.25		2.5		3.125 Gbs	
	1 way	2 way	1 way	2 way	1 way	2 way	1 way	2 way
16750/1/2, 16910/1	SR441_11	SR441_12	SR441_11	SR441_12	SR441_13	SR441_14	SR441_13	SR441_14
16753-6 or 1695x	SR441_15	SR441_16	SR441_15	SR441_16	SR441_15	SR441_16	SR441_15	SR441_16
16760	SR441_19	SR441_19	SR441_19	SR441_19	na	na	na	na
16740/1/2	SR441_11	SR441_12	SR441_11	SR441_12	na	na	na	na
1680x	SR441_50	SR441_51	SR441_50	SR441_51	SR441_50	SR441_51	na	na
1680/90	SR441_21	SR441_22	SR441_21	SR441_22	na	na	na	na

Refer to the User Manual for more detail on the application of each of these configuration files.

Probe Manager

This Windows based application controls the configuration and operation of the FS4410 probe. The Probe Manager application detects all FS4410 probes that are connected to the USB bus and starts up with the device selection window which allows the user to select which probe will be controlled and which FPGA file will be loaded.



The Probe Manager application is organized into 4 sections, each having their own dialogue window.

- Probe Configuration – Covers the type of probe cable used and basic aspects of the link being probed.
- Packet Recognizers – Provides access to the registers used to set 3 Packet Recognizers provided per Link which may be used to specify packet based triggering parameters.
- Filters – Allows the user to specify the types of packets to be filtered.
- Log Entries – Captures and displays run time probe status in a log file.

The Help button provides version information for the software and the currently loaded FPGA file.
The Upgrade button allows updating of the currently loaded FPGA code.

Refer to the User Manual for more information on the Probe Manager.

Logic Analyzer Setup

The configuration files include some basic Trigger settings using Event codes (user should qualify with Default Store bit). This allows easy set-up of the analyzer to trigger on any event, just one specific event or a combination of events.

Probe LED Indicators

Link A or B Signal LED color	Meaning
Green	Link OK
Dark	Loss of Signal
Orange	8b10b Data Error
Red	Receiver Fault: Lost Lock, Lost Sync, FIFO Over/ Under run (See details in Log)

Link A or B Data LED color	Meaning
Green	Data clocking Into Analyzer
Dark	No Data clocking into Analyzer
Orange	8b10b Data Error, Framing, Idle or Alignment Error
Red	Processor Clock Error (stop and re-run probe)

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sRIO State Analysis Probe - FS4410

16700 - Quick Start Instructions

It is strongly recommended that the user carefully follow the User Manual the first time the probe is used on a new sRIO link.

Step 1 Software Installation - **Refer to the User Manual** for the steps required to install the Protocol Decoder on the 16700 logic analyzer, the Probe Manager software and required USB drivers on a Windows-based system, and also for the Off-line installation of the Windows-based Protocol Decoder and Transaction Viewer software. **These steps only need to be performed once**.

Step 2. Connect the logic analysis cards to the FS4400.

Logic Analyzer	FS4410	Comment
Master Pod 1	A1	J clock first link
Master Pod 2	A2	
Master Pod 3	A3	
Master Pod 4	A4	
Expander Pod 1	B1	J clock second link
Expander Pod 2	B2	
Expander Pod 3	B3	
Expander Pod 4	B4	

Step 3. Attach the probing cable, and Reference Clock cable if required (see manual), to the probe and to the target system. Attach the USB cable from the probe to the PC where the Probe Manager application has been installed.

Step 4. Power up the logic analyzer, the PC where the Probe Manager application resides, the FS4410 probe, and the target system in this order.

Step 5. Load the logic analyzer with the appropriate configuration file from the logic/configs/FuturePlus/FS4410 directory. See chart below for the correct file to load.

Configuration files for 8b mode only. See the User Manual for 10b mode configuration files.

167xx Analyzer	X1 2 way any cable		X4 2 way using any cable					
	Any link speed		1.25		2.5		3.125 Gbs	
	1 way	2 way	1 way	2 way	1 way	2 way	1 way	2 way
16715/6/7 or 16750/1/2	SR441_1	load twice	SR441_1	load twice	SR441_3	load twice	SR441_3	load twice
16753-6	SR441_5	load twice	SR441_5	load twice	SR441_5	load twice	SR441_5	load twice
16760	SR441_9	load twice	SR441_9	load twice	na	na	na	na
16740/1/2	SR441_1	load twice	SR441_1	load twice	na	na	na	na

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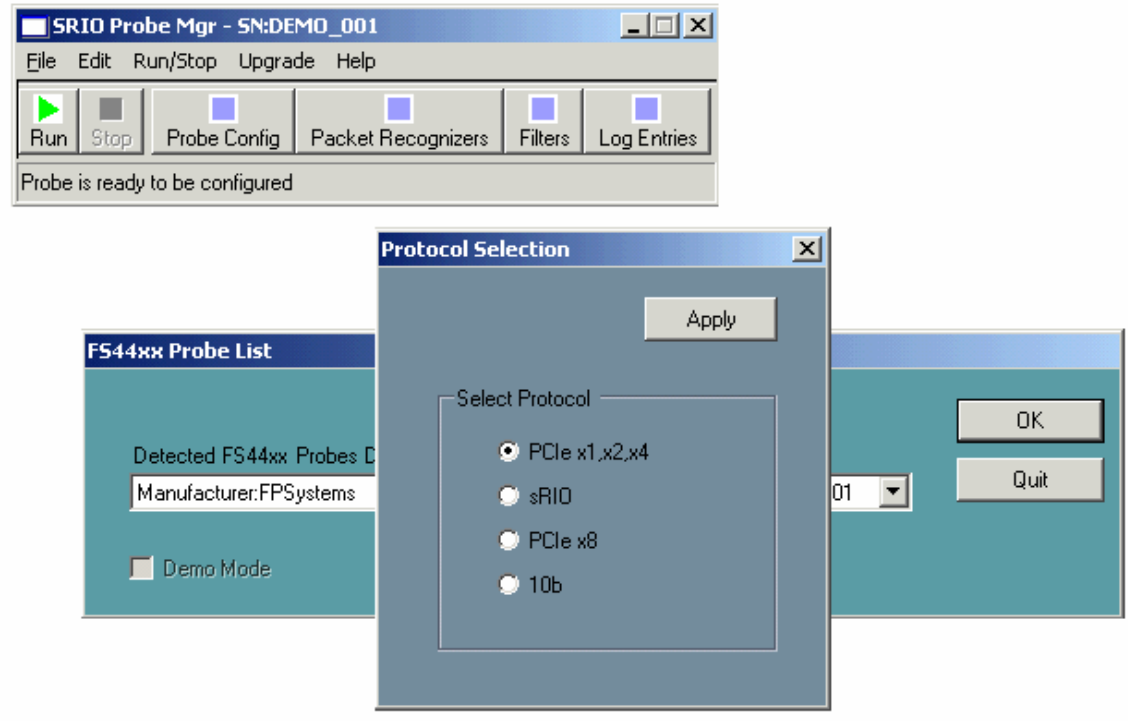

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