

VME64

VME64/VXI Analysis Probe and extender FS3100

Quick Start Instructions

State Analysis

Step 1. Set the State/Timing switch to the down (State) position for state analysis.

Step 2. Set jumpers across pins 1 and 2 of jumpers J2 through J6 if the daisy chain on signals BG3IN* through BG0IN* and IACK* need to continue to the next slot. Otherwise, set jumpers across pins 2 and 3. Note that if the Analysis Probe interface board is used as an extender, the jumpers must be set across pins 2 and 3.

Step 3. After removing the probe tip assemblies from your logic analyzer cables, plug the logic analyzer cables into the 40 pin cable headers on the FS3100 module. The table below gives the correspondence between the FS3100 cable headers and the logic analyzer cables.

16717/8/9, 16750/1/2, 1674x, 1691x				
<u>1660 POD</u>	<u>16550 POD</u>	<u>1655x POD</u>	<u>FS3100 Header</u>	<u>Comment</u>
1	1 Master	1 Master	1	
2	2	2	2	
3	3	3	3	
4	4	4	4	
5	5	1 Expander	5	
6	6	2	6	
7	1 Expander	3	7	Double probe cable-D64 Only
8	2	4	8	Double probe cable-D64 Only

Step 4. Install the FS3100 module into a slot in the target VME.

Step 5. Load the logic analyzer with the appropriate file (see table below) from the Analysis Probe software diskette.
See the users manual for A64/D64 support.

A32/D64 VME bus

<u>Logic Analyzer</u>	<u>File name</u>	<u>Comment</u>
1660	F660_00	
16550	F550_00	2 16550 cards necessary (Expander below Master)
16555, 1670	F555_00	2 16555 cards necessary (Expander below Master)
167XX	F555_00	2 1671x, 1675x, 1674x (Expander below Master)
1691x	VM310_1*	2 1671/4/5x, 1951x (Expander below Master)

A32/D32 Support

<u>Logic Analyzer</u>	<u>File name</u>	<u>Comment</u>
1660	F550_02	
16550	F550_02	1 16550 card necessary
16554/5/6/7	F555_02	2 16554/5/6/7 cards necessary
1670	F555_02	
167XX	F555_02	2 1671x, 1675x, 1674x (Expander below Master)
1691x	VM310_3*	2 1671/4/5x, 1951x (Expander below Master)

* VME Protocol Decoder loads by default, see User Manual.

Step 6. To acquire data touch the RUN button on the Listing screen.

Timing Analysis

Set the State/Timing switch to the up (Timing) position for timing analysis. Follow steps 2-5 above and **then** change the type field in the logic analyzer configuration menu from STATE to TIMING. To acquire data touch the run button.

You're ready to GO!