

DDR DRAM Analysis Probe – FS2336

Quick Start Instructions

1. Check Logic Analyzer – It is recommended that 16753/4/5/6 cards be used because of their superior setup/hold performance and signal loading characteristics. The 167xx should have operating system version A.02.70.00 or higher installed for 2 card timing or 3 card state configurations. Operating system version A.02.80.00 or higher is required for 4 card state dual sample configuration. 169xx analyzer should have A.02.00.00 system software or higher.

2. Connect the probe to the logic analyzer per the following table:

FS2336 Conn (J)	Analyzer Pod 2 card timing configuration	Analyzer Pod 3 card state configuration	Analyzer Pod 4 card dual sample config
J1 Odd	D1 (master)	E1	C3 (master)
J1 Even	D2 (master)	E2	E1
J2 Odd	D3 (master)	D1 (master)	C1 (master)
J2 Even	D4 (master)	D2 (master)	E3
J3 Odd	E1	D3 (master)	C2 (master)
J3 Even	E2	D4 (master)	D1
J4 Odd	E3	E3	D3
J4 Even	E4	E4	B1

For 169xx users refer to “General Purpose Probe Feature” section of the configuration file for analyzer connections.

3. Install the Protocol Decoder and Configuration files from the floppy using the 16700/702 software installation procedure outlined in the FS2336 manual. This will install a protocol decoder called “IFS2336E” in the ia directory, and will install configuration files in the /logic/configs/FuturePlus/FS2336 directory that allow you to easily configure the analyzer for timing or state operation with the FS2336. For 169xx users use the CD that came with the product and double click the FS2336.exe file to install. Refer to the User Manual for FS1141 installations if your product was provided with this tool. After installation there will be a folder on the desktop with shortcuts to the configuration files.

167xx	169xx	Timing	State
16753/4/5/6	1675x,1691x, 1695x	DR236_1	DR236_2 (Read Only)
16753/4/5/6	1675x,1691x, 1695x		DR236_3 (Write Only)
16753/4/5/6	1675x,1691x, 1695x		DR236_4 (Data Eyescan)
16753/4/5/6	1675x,1691x, 1695x		DR236_5 (Address Eyescan)
16753/4/5/6	1675x,1691x, 1695x		DR236_6 (dual sample)*

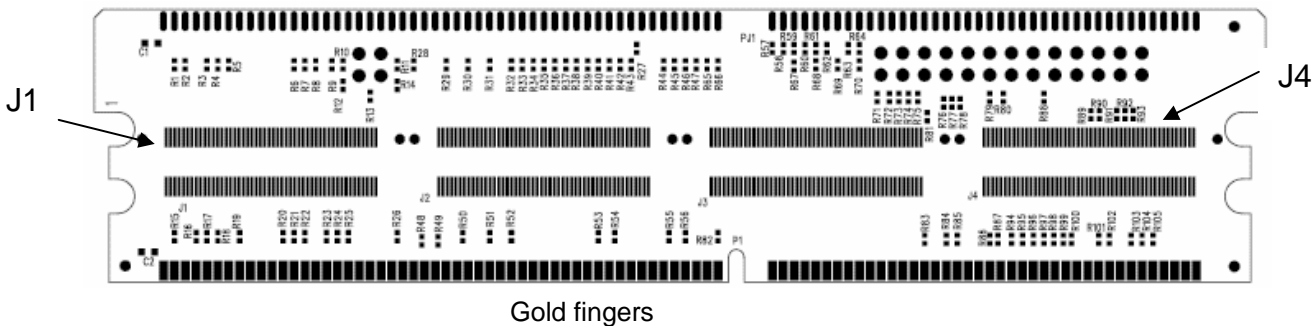
*Requires OS of A.02.80.00

4. Load the appropriate configuration file. If you are doing timing analysis you are set to capture data without further set up once the timing configuration file is loaded. If you are doing state analysis you must adjust the setup and hold settings to capture data properly. Please consult the FS2336 manual on adjusting the setup and holds properly.

5. Once the setup and holds are calibrated per the User Manual you are ready to capture data using state analysis.

Probe Connections

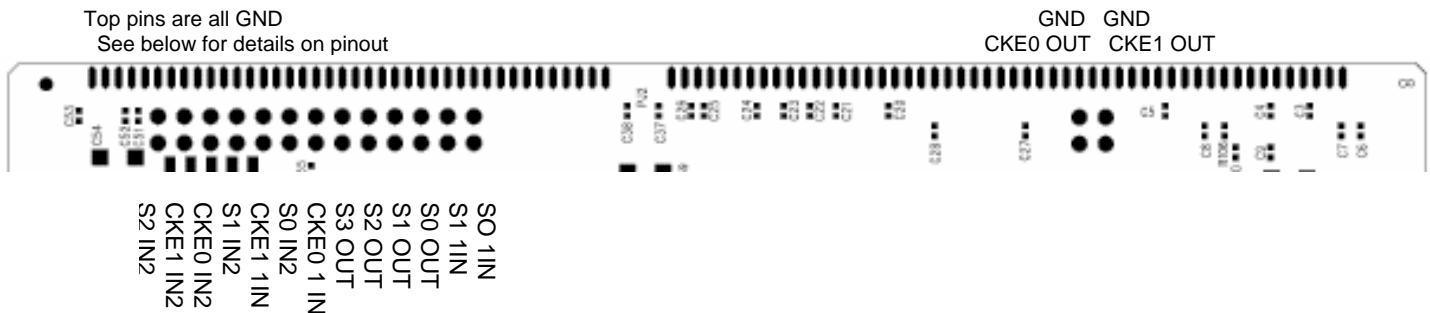
The 16753/4/5/6 and 1691/5x cards require the E5378A adapter cables. 1 Adapter cable is required for 2 pods. Alternatively the “right angle” cables, FS1026 (E5388A), may be used with the FS2336 to eliminate potential interference with adjacent DIMM modules. The drawing below details the location of J1 and J4.



Interconnection Points

The FS2336 probe provides interconnection access to the Chip Select and Clock Enable signals by means of right angle pin headers on the back side of the probe. These headers are standard .020” square pins on .100” centers and they are wired so that the each signal has a companion ground signal on the inside pin of the pair. The following is a detail of their location on the probe as seen from the rear (non-100 pin connector) side of the probe. Refer to the FS2336 User Manual for more details.

***Be careful when using the probe with adjacent dual sided DIMMs
Pin headers can touch components on the adjacent DIMM***



Using EyeScan – see the User Manual for instructions.

For Technical Support call 603-471-2734
For Sales information call 719-278-3540
Please visit our web site at www.futureplus.com
 FS2336 QS rev. 1.4