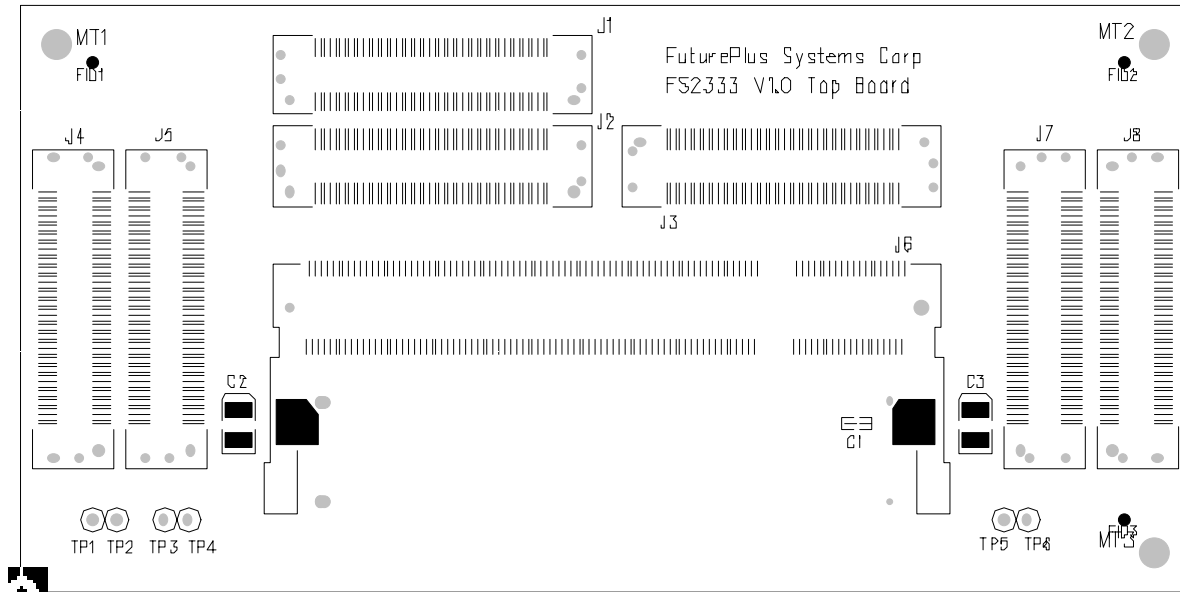


# FS2333 SODIMM DDR Probe Quicksheet

1. Determine if the target system requires a Right-hand or Left-hand probe connection. Select the appropriate Lower board, reference the silkscreened legend on the back of each Lower board.
2. Attach the Lower board to the SODIMM Probe Upper board. This requires mating the 2 Bergstack connectors. They are keyed to prevent reversing this connection.
3. At this time insert a SODIMM memory module into the probe at J6 if one is to be used with the probe.
4. Attach the logic analyzer cables to the probe. The number of cables required depends on whether timing or state analysis is required. Reference the following FS2333 Upper board drawing and table of probe cable connections.



Probe Cable	Analyzer Pod*
J3 odd	B1 (master)
J3 even	B2 (master)
J7 odd	B3 (master)
J7 even	D1 (expander 3)
J2 odd	C1 (expander 1)
J2 even	C3 (expander 1)
J5 odd	A1 (expander 2)
J5 even	A3 (expander 2)

\*For dual sample config. (requires OS A.02.80.00)

For **169xx users** refer to “general purpose probe feature” section of the configuration file for analyzer connections.

5. Once all the connections have been made to the probe, insert the probe into the target board.

6. Load the configuration file per the table below and the instructions in the User Manual and on the Software Entitlement Certificate. Please note that this product is licensed and needs to be installed per the instructions if it is to work for an indefinite period of time. This product will run in “demo mode” for several days without licensing.

167XX	169XX	Timing	State
1675x	1675X, 1691X, 1695X	*DR233_3	**DR233_4 4 card State analysis for Read and Write
16753/4/5/6		*DR233_2	**DR233_4 4 card State analysis for Read and Write
16717/8/9		*DR233_3	

\*Requires 2 cards configured as 1 machine

\*\*Requires 4 cards configured as 1 machine

7. If Timing mode analysis is desired the FS2333 is all set to capture data.
8. If State mode analysis is desired, then the probe and the FS2333 Data Decode tool need to be set-up first with information regarding the target platform and memory devices. This includes:
- CAS Latency – In number of CK0 cycles for Read command to data valid.
  - Burst length – Usually fixed as 2, 4, or 8 data strobes per Read or Write.
  - Write delay - The number of CK0 cycles for Write Command to data valid.
  - Chip Selects – Either 1 or 2 depending on what is probed.
9. The FS2333 inverse assembler requires that measurements of Read and Write traffic be made using TimingZoom so that the appropriate valid states can be identified by the IA. Please see the User Manual for detailed instructions.

For Technical Support call 603-471-2734

For Sales information call 719-278-3540

Please visit our web site at [www.futureplus.com](http://www.futureplus.com)

---

# FuturePlus Systems

---