PCI Compliance Testing
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Agenda
☐ Overview of the PCI SIG Compliance Test Program
☐ Case Study System
   ☐ Timing Verification
   ☐ Performance
   ☐ Signal Integrity
☐ Summary and Questions

PCI Special Interest Group
☐ The PCI SIG (www.pcisig.com)
   ☐ 500+ member companies
   ☐ Technical Support
   ☐ Control the Specification and revisions
   ☐ Source of new PCI technology related developments
   ☐ Host the PCI Compliance Workshops

The PCI Compliance Checklist
☐ Written by members of the PCI Special Interest Group
☐ The purpose of the checklist is to promote interoperability in the PCI industry
☐ Required to get on the PCI SIG Integrator’s list
☐ Current Rev is 2.1
☐ Found on PCI SIG web page (www.pcisig.com)

The PCI Compliance Program
☐ Program Objectives
   ☐ Increase ramp of PCI products in the market by having trouble free interoperability for the end-user
   ☐ Focus only on the PCI content of the product as much as possible
   ☐ Increase acceptance of PCI by emphasizing design discipline and adherence to the spec

The PCI Compliance Program is a program that promotes PCI testing. This testing has two forms. The first, is for designers to use the PCI Compliance Checklist to ensure that their designs meet all the rules of the specification on an item for item basis. The second type of testing is to make sure that these designs all work together in various system configurations running various software applications. This is, for the most part, a voluntary program. There is no formal certification process and no certificate or label awarded to those who pass.

The PCI Compliance Workshops
☐ Sponsored by the PCI SIG
☐ Held 2 to 3 times a year
☐ Purpose:
   ☐ Provide a forum for devices to be tested together
   ☐ Get engineers talking about how to make PCI truly “Plug and Play”

The PCI Special Interest Group has held eleven PCI Compliance Workshops to date. The most recent was last week here in Berlin. All PCI Compliance Workshops are available to PCI SIG members and the dates and locations for future workshops will be listed on the PCI SIG home page www.pcisig.com.

What’s in the PCI Compliance Checklist?
☐ The checklist is a list of items that detail proper PCI bus operation.
The checklist is divided into the following areas:
- Motherboards
  - Electrical
- BIOS
- Components
  - Electrical
  - Configuration
  - Protocol
- Expansion Cards
  - Electrical
  - Configuration
  - Mechanical
- Systems
  - Mechanical

The Checklist is a minimum set of tests that must pass on every design and is divided into 5 main sections:
- Motherboard
- BIOS
- Component
- Expander cards
- System

Under these headings you can see the sub sections of Electrical, Configuration, Protocol and in the case of Systems, Mechanical.

Checklist items

Some checklist items can be verified by inspection of the design.
- For example
  - ME12-"The following signals are pulled up with a resistor of the correct value: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PER#, LOCK#?"

Some checklist items are best verified in simulation and then in the lab.
- For example
  - CE42-"All bussed signals are driven valid between 2ns and 11ns after CLK for 33Mhz PCI, between 2 and 6ns for 66Mhz PCI"

Included here are a couple items from the Checklist. As can be seen, some of the checklist items are more appropriate for a design review. Others can be tested in simulation and then in the lab.

Integrator’s List

Confidential to members of the PCI SIG

Inclusion on the list cannot be used for marketing purposes

Purpose:
- Encourage interoperability testing
- Encourage compliance testing
- Acknowledge those who have passed

The Integrators List was devise by the PCI SIG in order to promote PCI testing and interoperability. It is a list of known good PCI products. The Integrators List is confidential and only available to PCI SIG members.

Integrators List cont.

To get on the List:
- PCI SIG Member
- Satisfactory completion of the PCI Compliance Checklist
- Passed test criteria at the PCI Compliance Workshop
- Product must be production ready

For a product to be listed it must:
- Have completed and satisfactory PCI Compliance Checklist on file at the PCI SIG
- Have passed the test criteria set forth at the PCI Compliance Workshops
- Be production ready

This list is updated after each workshop. And contains the following disclaimer:
“The PCI Special Interest Group disclaims all warranties and liabilities for the use of any product listed in this document and assumes no responsibility for any errors that appear in this document nor for the completed PCI Checklist and/or compliance testing performed for any of the listed products.

Embedded PCI Designs

Most PCI design applications can use the tools developed for the PC PCI industry
- The protocol and timing rules of PCI are the same regardless of application
- The embedded PCI designer must look for:
  - Tools with compatible form factors
  - Chip based tools

Industries that choose to leverage the PCI technologies in their applications will be able to take advantage of the numerous tools and documents developed for the PC PCI industry. The embedded designer must consider their form factor when choosing PCI tools. The current leading form factor for the PCI technology is the desktop form factor, second is CompactPCI and PMC (PCI Mezzanine).

How do I get my design tested?

PC Industry
- Join the PCI SIG
- Get the PCI Compliance Checklist
- Attend the PCI Compliance Workshops
- Work with other vendors to do interoperability testing
  - Go well beyond the checklist and do robust system testing and verification

Embedded PCI
- Get the PCI Compliance Checklist
- IF your design can be tested in PC’s attend the workshops.

Currently the compliance program is geared toward the PC industry. The embedded PCI designer can use the tools and the compliance checklist to accomplish a similar level of testing. CompactPCI and PMC tools are readily available on the market.

Compliance Test Summary

PCI Designers have the advantage of a well written specification and test checklist
- Use the Compliance Test Checklist
  - At design time
  - For verification

However, the Checklist provides only a minimum set of tests

Proper electrical testing will insure interoperability in the field
- If your designs can be tested in a PC, attend the compliance workshops

The PCI designer is fortunate to have a well written specification that has been extensively reviewed and supplemented with a Compliance Test Checklist. The PCI designer can use the Compliance Test Checklist both at design time and at verification time. However, the PCI designer will have to go well beyond the PCI Compliance Checklist in order to ensure that their design is compliant. Rigorous system and interoperability testing along with examination of design margins will ensure a reliable, compliant design.

Case Study System
- Ziatech CompactPCI System

Get the Compliance Checklist
- Attend the compliance workshops.
Pentium CPU
PCI Bus (10 slots)
- Ethernet (bus mastering)
- SCSI

How the analysis was done

- The Test Equipment used
  - HP Prototype Analyzer HP16505A
    - HP16500C mainframe
    - HP16555A logic analyzers
    - HP 16534A Oscilloscope
    - HP 16517A/518A high speed timing cards
  - CompactPCI Preprocessor
    - with extender card functionality

Here is a list of test equipment that was used to monitor the system. A CompactPCI Preprocessor was used to provide connection from the test equipment to the PCI bus under test.

CompactPCI Preprocessor

The CompactPCI Preprocessor is a 3U form factor (extended length) that allows a convenient connection between your HP logic analyzer and a CompactPCI system. All the signals on the CompactPCI connector are brought to the logic analyzer through high impedance matching termination networks. No flying leads! To prevent reflections from the added etch length of the extender card connector high speed clamping diodes are mounted near the extender card connector. The CompactPCI Preprocessor can also operate in the system slot with the CPU on the extender card connector. This allows the viewing of all the REQ# and GNT# signals. The product comes with complete configuration files for all HP logic analyzers and a PCI Inverse Assembler.

For more information on this product please visit our WEB site at www.futureplus.com.

Workspace

Here is the workspace that was used to study our CompactPCI system. The single icon on the left is the logic analyzer. As the work progressed, scope and high speed timing card icons were added. The icons on the right are the various measurement windows. The data can be put in chart form, viewed as a waveform or as a state listing. It can even be filtered so only the cycles of interest are viewed.

What did we look for?

- Timing Verification
- Performance Characteristics
- Signal Integrity

Timing Verification

- We tested the Command lines for setup per checklist item CE46:
  - To make the measurement
    - Connect the C/BE[3::0]# lines and the CLK to the high speed timing card via the CompactPCI Preprocessor test points
    - Use the setup and hold macro to program a setup time of 6ns to the rising edge of CLK
  - Use this technique to test any setup and hold time that you have specified for your design

Slot to Slot clock skew

The HP16517A/518A was chosen for this particular test because it has built in timing violation trigger macro’s that make triggering on setup and hold violations very easy.

This test dictates that all bussed signals be examined. For this example only the command lines will be tested. The HP16517A was attached to the test points of the CompactPCI Preprocessor. The HP16517A /518 setup and hold macro was programmed for 6 ns since the macro can only be programmed in increments of 2 ns. This does not mean we will miss the violation. It means we have set a slightly stricter criteria. If the analyzer triggers we will be able to make a measurement down to a resolution of 250 ps and thus rule out any “false positives”. What this equipment will do is monitor the bus and if a violation is ever detected it will trigger. This means that the command lines will be tested against EVERY rising edge of the clock for this violation. The HP16517A/518A has up to 80 channels so many signals can be examined at once. After the command lines we looked at slot to slot clock skew.

Setup and Hold on C/BE lines
Timing verification is an important part of most digital designs and PCI is no exception. In fact, timing seems to be the major headache for most PCI designers. Test CE46 from the PCI Compliance Checklist says that all bussed inputs must require no more than 7ns of setup time. This particular specification has caused the most headaches for PCI interface and motherboard designers. This requirement also implies that the system must provide this setup at all PCI inputs.

Our case study system did not cause the high speed timing card to trigger. Therefore no violation was found. In order to characterize our system we backed off the trigger until we found the setup/hold that the system was operating at. This is a good method of measuring the timing margins of the system.

Tval on C/BE lines

Test CE42 is the drive valid spec for PCI. All bussed signals must be driven valid 2 to 11ns after the rising edge of the clock (33Mhz). Our case study system showed no Tval violation on the C/BE signals and those signals were driven valid within 5ns.

Corresponding State Listing

This slide shows the corresponding state listing, triggered from the high speed timing card. If a violation existed this would show the bus master, the data and the transaction type that was present when the violation occurred.

FRAME# setup/hold

This slide shows FRAME# and the PCI clock. Tval was measured at approximately 5ns which provides the system with ample setup time.

Clock Skew (slot 1 to 5)

We also examined the system for clock skew. This picture shows no violation of the PCI Clock Skew specification in our case study system. Per the PCI Specification section 4.3.1 “The maximum allowable clock skew is 2 ns.” The measurement was made at the CompactPCI Preprocessor test points (close to the connector).

Clock Skew (rising edge)
Performance Characteristics

- **GNT# to the start of transaction**
  - 8 clocks maximum, 2 to 3 clocks recommended
- **Bus Utilization**
  - Wait states
  - Idle states

The PCI SIG has compiled a list of PCI “Do’s and Don’ts” that are distributed at the PCI Compliance Workshops. On that list is an item that reads “Target inserts too many wait states before returning the first data”. This is inefficient use of the bus bandwidth and can impact devices with low latency requirements. Per the PCI Specification and the checklist, if the target cannot deliver the first data within 16 clocks the target must retry the access. Also the target is required to complete subsequent data phases within 8 clocks from the completion of the previous data phase.

Another performance metric is how quickly the master can start a transaction once GNT# has been asserted. The specification and the checklist require that the master drive the AD and C/BE lines within 8 clocks and 2 to 3 clocks is recommended.

The following slides show how our case study system performs against these metrics.

**GNT# to FRAME#**

GNT# to FRAME# is a measure of how quickly the master once given a grant can utilize the bus. The above screen shot is from the HP16505A prototype analyzer running the System Performance Analysis software. The CompactPCI Preprocessor was used as the means of monitoring FRAME# and GNT#. The Ethernet bus mastering card was placed in the CompactPCI Preprocessor’s extender card connector and a simple block copy program was run. The ethernet card performed very well. GNT# to FRAME# was always one clock tic.

**Transaction Types**

This SPA (System Performance Analysis) chart shows a distribution of transaction types for the system while our copy program was running.

**What traffic is the enet card contributing?**

Using the SPA software I can qualify the trace and show only the traffic when GNT# is asserted. Since the ethernet card is in the extender card connector its GNT# will be used to do the qualification. As expected the ethernet card is doing memory reads and writes.

**Distribution of Addresses**

(I/O and Memory)
To further qualify the traffic I can take a look at what address ranges are being generated by the copy program. The I/O addresses are well concentrated between x00002008 and x00002040. The memory addresses are a bit more scattered but are between x00f75010 and x00FA91C0. This method of viewing the data can help find code bottlenecks that could contribute to poor system performance.

**Burst Traffic**

This chart shows a time distribution of the length of the memory bursts. The timer starts when TRDY# and IRDY# are both asserted and stops when either releases. In our case study system a clock tic is 32 ns. The largest number of bursts occur in the 10 to 12 clock tics range.

**TP26-Wait States**

No violation of TP26 (the target always completes the initial data phase within 16 clocks.) could be found while running our copy program. By backing off the number of consecutive wait states that we looked for in the trigger spec, we could find where the system was operating. We found only two consecutive target initiated wait states.

**Signal Integrity**

- Factors that contribute to PCI Signal Integrity

- Problems
  - Bus contention
    - Slow turn-off or tri-state times
  - Edge rate
    - Too fast an edge rate causes ringing
  - Signal routing
    - Stubs and impedance mismatches
  - Signal loading
    - PCI has strict rules on loading
  - Logic errors that cause glitches to propagate

Chapter 4 of the PCI Specification covers the electrical environment for PCI. Signal Integrity investigation is most important in high volume applications where variation in parts, connectors, capacitors and resistors can cause failures. These types of failures sometimes show up in manufacturing but in some cases show up in the field when the user tries to install his new PCI board in his existing PCI based system. As high volume consumer Manufacturers know, failures in the field are the most expensive to fix. Costs for customer service, support and field replacement of boards can be astronomical. In addition, a company’s reputation for quality can be severely tarnished.

For PCI, a robust signal integrity analysis of the design is a cost effective step in the overall design and verification process.
This is TRDY# and the clock. Note that TRDY# is pulled high by the system and then when driven drops to a slightly lower voltage level.

Summary

☐ Our Case Study system performed well!
  ☐ Better than the PC systems we’ve examined in the past
☐ All PCI designers regardless of application can take advantage of the PCI Compliance Checklist
☐ The PCI designer must go well beyond the Compliance Checklist to achieve a fully compliant PCI design

This presentation has taken a brief look at how the industry is approaching PCI test through the PCI Compliance Test Program. A CompactPCI system was used as a case study for a few compliance measurements. Our case study system performed well. No violations were found. PCI has continually improved and the problems that engineers are finding are migrating away from the simple protocol and design errors and migrating to the more complicated system and electrical issues.

It is estimated that PCI is currently being used or will soon be used by every major computer manufacturer in the world. In order to ensure its success proper testing is being promoted by the PCI industry.

Additional Resources

☐ Preprocessors
  ☐ Pentium
  ☐ PowerPC
  ☐ ISA Bus
  ☐ USB
  ☐ VME
  ☐ PMC-PCI Mezzanine
  ☐ CardBus

☐ Software Debug
  ☐ HP’s Software Analyzer

The Pentium and PowerPC Preprocessors along with the HP Software Analyzer are available from Hewlett-Packard Company.

The PCI, USB, PMC, VME, ISA, CardBus and the PCI Preprocessor Plus are available from FuturePlus Systems (719-380-7321 or www.futureplus.com).

VME and PMC