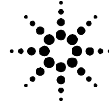


**FuturePlus® Systems
Corporation**



Agilent Technologies
Innovating the HP Way

Premier Solution Partner

FIBRE CHANNEL PROBE FS4320

Users Manual

For use with Agilent Technologies Logic Analyzers

Revision 1.1

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Agilent Technologies is also an authorized reseller of many FuturePlus products. Contact any Agilent Technologies sales office for details.

Product Warranty

Due to the variety of possible customer target implementations, the FS4320 Fibre Channel probe has a 30 day acceptance period by the customer from the date of receipt. If the customer does not contact FuturePlus Systems within 30 days of the receipt of the product it will be said that the customer has accepted the product. If the customer is not satisfied with the FS4320 Fibre Channel probe they may return the FS4320 within 30 days for a refund.

This FuturePlus Systems® product has a warranty against defects in material and workmanship for a period of 1 year from the date of shipment. During the warranty period, FuturePlus Systems will, at its option, either replace or repair products proven to be defective. For warranty service or repair, this product must be returned to the factory.

For products returned to FuturePlus Systems for warranty service, the Buyer shall prepay shipping charges to FuturePlus Systems and FuturePlus Systems shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to FuturePlus Systems from another country.

FuturePlus Systems warrants that its software and hardware designated by FuturePlus Systems for use with an instrument will execute its programming instructions when properly installed on that instrument. FuturePlus Systems does not warrant that the operation of the hardware or software will be uninterrupted or error-free.

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The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, or improper site preparation or maintenance. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. FUTUREPLUS SYSTEMS SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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IMPORTANT - Please **read** this license agreement carefully before opening the media envelope. Rights in the software are offered only on the condition that the customer agrees to all terms and conditions of the license agreement. Opening the media envelope indicates your acceptance of these terms and conditions. If you do not agree to the licensing agreement, you may return the unopened package for a full refund.

License Agreement

In return for payment for this product, FuturePlus Systems grants the Customer a SINGLE user LICENSE in the software subject to the following:

Use of the software

- Customer may use the software on any one Agilent 1670x mainframe and any one 1680/90/900 logic analyzer or PC for offline analysis.
- Customer may make copies or adaptations of the software.
- Customer may not reverse assemble or decompile the software.

Copies and Adaptations

- Are allowed for archival purpose only.
- When copying for adaptation is an essential step in the use of the software with the logic analyzer and/or logic analysis mainframe so long as the copies and adaptations are used in no other manner. Customer has no right to copy software unless it acquires an appropriate license to reproduce from FuturePlus Systems.
- Customer agrees that it does not have any title or ownership of the software, other than the physical media.

Ownership

- Customer acknowledges and agrees that the software is copyrighted and protected under the copyright laws.
- Transfer of the right of ownership shall only be done with the consent of FuturePlus Systems.

Sublicensing and Distribution

Customer may not sublicensing the software or distribute copies of the software to the public in physical media or by electronic means or any other means without the prior written consent of FuturePlus Systems.

Introduction

Thank you for purchasing the FuturePlus Systems FS4320 Fibre Channel State Analysis Probe. We think you will find the FS4320, along with your Agilent Technologies Logic Analyzer, a valuable tool for helping to characterize and debug your Fibre Channel-based systems. This Users Guide will provide the information you need to install, configure, and use the Fibre Channel Probe. If you have any questions about this Guide or use of this probe, please contact FuturePlus Systems Corporation.

Definitions

Logic Analyzer Modules

"Module" - A set of logic analyzer cards that have been configured (via cables connecting the cards) to operate as a single logic analyzer whose total available channels is the sum of the channels on each card. A trigger within a module can be specified using all of the channels of that module. Each module may be further broken up into "Machines". A single module may not extend beyond a single 5 card in a 1670x frame. A 169xx frame can hold either 3 or 6 cards depending on the model.

"Machine" –

A set of logic analyzer pods from a logic analyzer module grouped together to operate as a single state or timing analyzer.

FC

Abbreviation for Fibre Channel

FS4320 Probe Description

The FS4320 Fibre Channel (FC) Probe allows a user to perform State Analysis measurements on up to 6 optical Fibre Channel links operating at either 1.0625 or 2.125 Gbps. The serial data on the FC (Fibre Channel) links is converted to parallel data streams and clocked into the logic analyzer using a 55 Mhz master clock for all six data streams.

Probe Technical Feature Summary

- Probing of up to 6 FC links at either 1 or 2 Gbps speeds while transmitting in either Tee or Repeat modes.
- Front panel control of probe output to logic analyzer includes, Idle and Primitive Stripping, CRC identification, and built in test selection.
- Test packet generation capability when used with the optional FS1121 product.
- All 6 probe outputs are clock to the logic analyzer by one 55 Mhz Master clock.
- Protocol Decode software for both the 16700 and 1680/90 logic analyzers which displays Frame information, including Header, Payload and validation of CRC value. Software also contains Preferences Menus, which gives the user flexibility in how information is displayed.

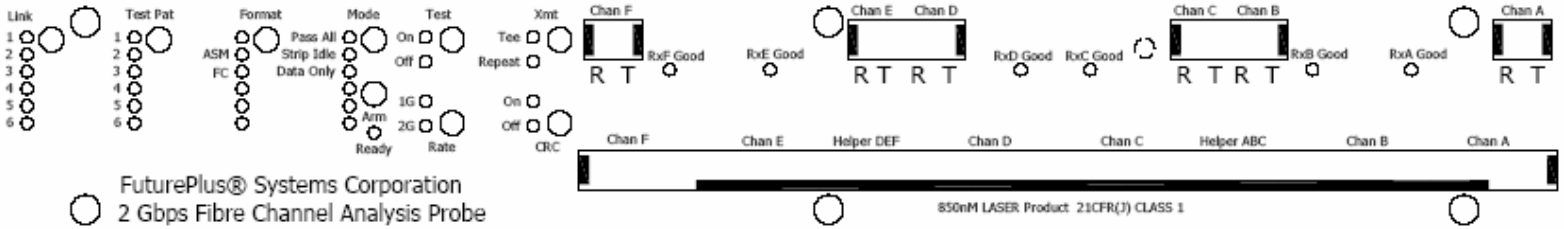
Probe Components

The following components have been shipped with your FS4320 FC Probe:

- FS4320 Fibre Channel Probe in 19" rack mount case
- Floppy disk containing 16700 protocol decoder installation files.
- Software Entitlement Certificate for 1670x based protocol decoder.
- This Users Guide and other information on CD-ROM.
- The FS1122 for use on 1680/90/900 analyzer or offline viewer on CD-ROM.
- Software Entitlement Certificate for FS1122 1680/90/900 analyzer or offline viewer
- Quick Start Sheet.
- 110VAC 3 prong power cord

FS4320 Fibre Channel Probe Connections

Front Panel



There are a number of Front panel connectors, indicators and switches. The following is a description of their functions.

Front Panel Connections

FC Inputs - 6 optical Fibre Channel LC duplex type connections for Receive and Transmit. Channels are named A, B, C, D, E, F.

Probe outputs to logic analyzer – 8 Mictor connectors compatible with Agilent logic analyzer adapter cable E5346A or E5380A. Connectors are organized so that FC data brought to LC duplex “A” is sent out of the probe on Mictor “A”. Status information for 3 input channels (A, B, C) and (D, E, F) are grouped together on the “Helper” connectors. Connector pin outs are described later in this manual.

Front Panel Switches and Indicators

Rx_ Good – Green indicator for each channel that confirms probe input is receiving FC traffic.

CRC – SHOULD ALWAYS BE IN THE “ON” POSITION.

This switch and associated indicators are only functional in a future enhancement of the FS4320 which will provide analysis of the FPDP FC format.

Xmt – This switch sets the transmit mode of the FS4320. In “Tee” mode, the probe operates as a node using 2 pairs of optical links. Information received in on one pair is sent out the other. For example, Channel A R and T is retransmitted through Channel B T and R. In “Repeat” mode the probe retransmits data received on a channel through the transmit side of that channel.

Rate – This switch sets the baud rate of the signals connected to the FS4320. “1G” is 1.0625Gbps and “2G” is 2.125Gbps.

Test - This switch is active when the associated LED is green. This switch causes the unit to transmit a test pattern on all transmit fibers. The type of test pattern is controlled by the “Format” switch and the “Test Pat” switch. When the unit is placed in Test mode, the “Xmt” switch should be in the “Tee” position.

Format switch in ASM position, Test Pat switch in following positions:

Test #1	IDLE words
Test #2	ASM packet with dummy Header fields
Test #3-6	undefined

Format switch in FC position, Test Pat switch in following positions:

Test #1	zero-length data packet (ZLDP)
Test #2	FC packet with dummy Header fields
Test #3-6	undefined

Arm – After the probe is powered on it must be “Armed” before decoding FC traffic. This insures that only complete packets are captured and decoded. When the probe is armed the “Ready” indicator will light. Once the probe starts to capture data the Ready light will go out and the probe will transfer data to the logic analyzer.

To capture data again, the logic analyzer should be armed, the data source reset (if possible), and the probe re-armed. This clears out any data stored in the probe and insures that a complete packet is captured.

Cross triggering (In and Out) of the probe and analyzer is possible through rear panel connections

Mode – This controls what data is passed from the probe to the logic analyzer. “Pass All” causes all data received on the input channels to be sent to the logic analyzer. “Strip Idle” invokes the probe to filter out all packets identified as Zero Data or Idle. “Data Only” mode passes payload data only. In this mode timing relationships in the probe change so that helper signals for the channels, either internally generated or passed from the rear external connector, may be sent to the logic analyzer earlier than the data is presented.

Format – This sets the format of the received data. “ASM” is an abbreviation for Anonymous Subscriber Messaging. “FC” is for Fibre Channel. There are 4 unused positions for the Format switch that are reserved for future functions.

Test Pat – This defines what internal test pattern the probe will generate.

Link – When using the FS4320 probe in order to capture as much data as possible across multiple links that were initially aligned at the source, then Channel Linking can be used. When the FS4320 FC probe “links” channels, it attempts to align the first byte in the first packet across all the channel outputs to the logic analyzer. This function helps to improve logic analyzer memory utilization in circumstances where some of the probed FC links may have data packets occurring at the same time. Linking stores the data packets for each linked channel in a FIFO. The contents of these FIFOs are clocked to the logic analyzer only after each linked FIFO contains data. If channels are not linked their received data is passed to the logic analyzer as it is received and without processing in a FIFO.

Slipping of linked data can occur if the FIFOs for some of the linked channels are full and others are not. This condition will be indicated by a high state on the Valid signal for that channel. In this circumstance the probe will repeat the data last sent on that channel to the probe.

Selecting “1” means that none of the 6 channels are linked. Selecting “2” means that Channel A and B are linked, “3” means a, B, and C are linked, etc.

Rear Panel Connections

LA Trig In or Trig In – These inputs function in a mode similar to the Arm switch on the front panel. A leading edge transition on these inputs is required. The FS4320 probe can be triggered by a logic analyzer through this connection. The “Run” button on the logic analyzer will arm the probe, which will then capture and pass data on the next complete packet.

Trig Out – This signal allows the FS4320 to arm the logic analyzer after it arms. This signal can also be used to connect to the “Trig In” connection on other FS4320 probes to establish a cascaded series of master and slave probes. In this case the “Arm” function of the master triggers all the slave probes.

Custom I/O – This DB25 female connector provides a rear panel egress for the Helper bits. Its pinout is defined later in this manual.

Maintenance – This male DB25 connector provides the connection to a host PC when using the optional Fibre Channel Test Generation software.

Connecting the FS4320 probe Logic Analyzer

This section contains information for connecting the FS4320 probe to the 1670X/1690X and 1680/90 series logic analyzers.

The configuration files are designed to analyze up to three FS4320 Fibre Channel links, grouped into two sets: Channels ABC and DEF. These sets are defined because the FS4320 probe generates signals on the helper channels that are associated with the channel ABC or DEF. The decoder software is dependent on the helper signals to decode the trace information contained in the channels ABC or DEF.

The analyzer can be used to monitor a single channel in the group of three (ABC or DEF). The single channel can be any one of the three that make up the set, but the other connections must still be maintained in order for the labels to appear in the trace file, otherwise the decoder can not be successfully loaded from the INVASM (1670X) or Tools (1680/90/900) pull down menus.

The FS4320 probe can be connected to as many as 6 optical Fibre Channel links, Channels A thru F. These connections are made using SC duplex type fiber optic cables.

The connection topology of the probe can be selected to be of either “Tee” or “Repeater” type. Tee requires that an adjacent pair of duplex connections be used. Repeater requires only one duplex connection.

1670X/1690X Logic Analyzer

The following section contains information to connect the FS4320 to the 1670X or 1690X logic analyzer.

Target connections

A maximum of three FS4320 Fibre Channel links can be connected to one logical machine. The three connected links must either be ABC or DEF. The 1670X/1690x analyzer can contain multiple machines. A second machine can be configured within the 1670X/1690X to monitor the second set of Fibre Channel links.

Logic Analyzer connections

Depending on the number of FC links being probed, the FS4320 will require the following adapter cables and logic analyzer pods.

Number of FC links probed	Number of LA pods required	Number of Cards required	Number of LA adapter cables (E5346 or E5380)
1	4	1	2
2	6	2	3
3	8	2	4
4	12	3	6
5	14	4	7
6	16	4	8

Table 1

Logic Analyzer Card Configuration

The configuration files are set-up with 2 logic analyzer cards melded together as one logic analyzer machine with one Protocol Decoder. This provides enough connections to process 3 FC links and their associated helper signals (Helper ABC or Helper DEF). A second machine is required if more than 3 FC links are to be analyzed. The second analyzer utilizes the same configuration (in different slots) with a second Protocol Decoder session.

The configuration file requires that channels ABC are grouped together for one analyzer machine, and channels DEF are grouped together for the other analyzer machine. This requirement is imposed on the configuration file because Helper ABC pod contains signals for channels ABC and Helper DEF pod contains signals for channels DEF.

The 3 Fibre channel configuration needs to be loaded twice, once into each machine to make a total of 6 fibre channel analysis.

The following table summaries the pod and channel assignments for the two 1670X/1690X analyzer machine configurations:

Fibre Channel link	Logic analyzer Pods	Probe connection
A, B, C	Master pod 1	Channel A odd
	Master pod 2	Channel A even
	Master pod 3	Channel B odd
	Master pod 4	Channel B even
	Expander pod 1	Channel C odd
	Expander pod 2	Channel C even
	Expander pod 3	Helper ABC odd
	Expander pod 4	Helper ABC even
D, E, F	Master pod 1	Channel D odd
	Master pod 2	Channel D even
	Master pod 3	Channel E odd
	Master pod 4	Channel E even
	Expander pod 1	Channel F odd
	Expander pod 2	Channel F even

Table 2

It is possible to monitor only one Fibre Channel link for analysis, in which case, the following table should be used as a connection guide. This scenario requires one logic analyzer machine utilizing one analyzer card.

Fibre Channel link	Logic analyzer Pods	Probe connection
A	pod 1	Channel A odd
	pod 2	Channel A even
	pod 3	Helper ABC odd
	pod 4	Helper ABC even

Table 3

Table 4 lists the configuration files used with the 1670X logic analyzer.

Logic Analyzer	State	Comments
16717/8/9, 1674x, 1675x	FC430_1	3 Fibre channel analysis
16717/8/9, 1674x, 1675x	FC430_2	1 Fibre channel analysis

Table 4

1680/90 Logic Analyzer

The following section contains information to connect the FS4320 to the 1680/90 logic analyzer.

Target connections

A maximum of three FS4320 Fibre Channel links can be connected to the 1680/90 logic analyzer. The three connected links must either be ABC or DEF.

Logic Analyzer Card Configuration

The 1680/90 logic analyzer utilizes a configuration file that is functionally identical to the 1670X configuration file. The 1680/90 can be used to monitor Fibre Channels ABC or Fibre Channels DEF. The monitoring of all six Fibre Channels requires a second 1680/90 logic analyzer (where the 1670X analyzer required a second machine).

Refer to the “Connecting the FS4320 to the Logic Analyzer” section to obtain the specifics for connecting the 1680/90 logic analyzer to the FS4320 probe. Please note: the 1680/90 will either use the first or second half of table 2.

Installing Protocol Decode Software

The FS4320 probe is delivered with two sets of installation software: one set is contained on a floppy disk and is used with the 1670X analyzer and the second set is contained on the CD-ROM and is used with the 1680/90/900 analyzer or can be used as an offline viewer if you do not have a 1680/90/900 analyzer.

1670X Installation

The floppy disk supplied with the FS4320 FC probe contains the software required to operate the probe. Install the software from the floppy using the 16700 software installation procedure. The procedure installs the protocol decoder in the appropriate directory and the configuration files will be copied into the /logic/configs/FuturePlus/FS4320 directory. The location of the configuration file provides the user with the capability to easily configure the analyzer for timing or state operation with the FS4320. The software only needs to be installed on the machine the first time you use the probe, once the software has been successfully installed, configuration file can be loaded from the directory listed above. See the sections below for information on which configuration file to use for your application. When you load a configuration file for state analysis, the protocol decoder should automatically load. If the protocol decoder does not auto load, you may load it from the listing screen under INVASM pull down menu of the state analysis dialog; choose the file named IFS4320E.

1680/90/900 Installation

Before installing the protocol decoder for the USB protocol on a PC you must install the Agilent logic analyzer software. Once the Agilent logic analyzer software is installed, you can install the FS4100 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the .exe file on the CD-ROM disk and then double click the .exe file name from within the File Explorer navigation panel. In order to analyze USB1.1 and USB2.0 you must run both .exe files, once both .exe files have been executed and successful installation/licensing has been done you will be ready to analyze both USB1.1 and USB2.0 protocols.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe Adapter is used.

Table 5 lists the configuration files used with both the 1680/90 logic analyzer.

Logic Analyzer	State	Comments
1680/90, 1675x, 1695x, 1691x	FC430_1.xml	3 Fibre channel analysis`
1680/90, 1675x, 1695x, 1691x	FC430_2.xml	1 Fibre channel analysis

Table 5

Licensing

The 1670X and 1680/90/900 analyzer series both employ licensing. This section contains information for the licensing of the FS4320 probe on the two different analyzer platforms.

1670X Licensing

The FS4320 product is a licensed product that is locked to a single Agilent 1670x frame. The licensing area for the 1670X mainframe analyzer is found under System Administration. Please follow the instructions on the Software Entitlement Certificate provided with this product.

A demonstration period (no licensing required) is provided by typing the word *demo* into the licensing area next to the product name. For use of the FS4320 product beyond the demonstration time, please contact FuturePlus Systems at www.futureplus.com or 719-278-3540.

The following shows the ADMIN tab under System Administration Tools.

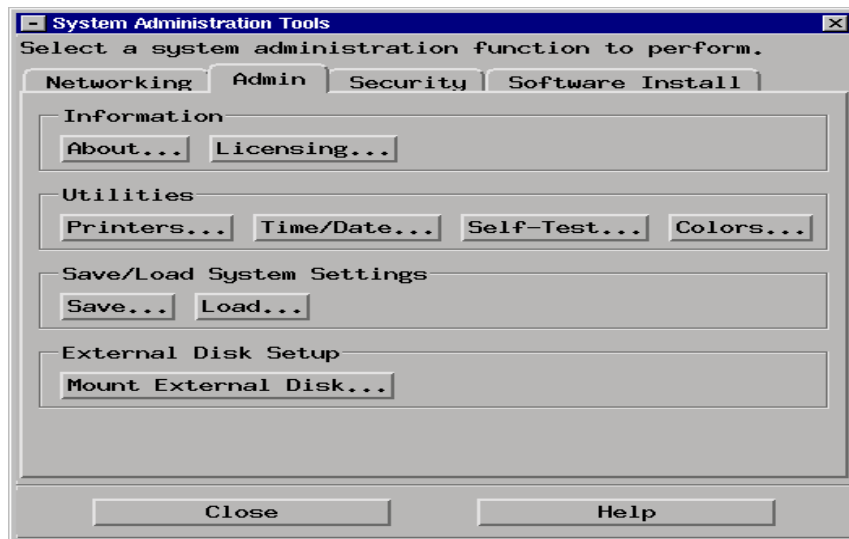


Figure 1

Once the FS4320 product is installed the password may be entered in the area shown below.

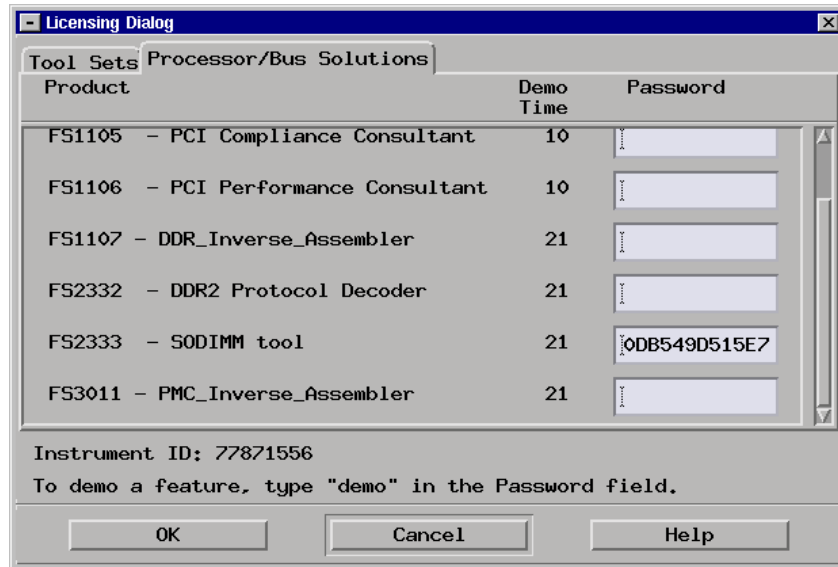


Figure 2

1680/90/900 Licensing

The Fibre Channel Inverse Assembler is a licensed product that is locked to a single PC hard drive.

The licensing process is performed by the Agilent logic analyzer. The instructions on this process are contained with the SW Entitlement certificate that is provided with the FS4320 product.

Fibre Channel Protocol Decoder Software

The Fibre Channel protocol decoder software has been developed for both the 1670X and the 1680/90/900 logic analyzers. Additionally, the 1680/90/900 decoder can be used with the PC based off line viewer tool.

The overall appearance of the PC-based Protocol Decoder is similar to other FuturePlus Systems products that run on the 1670X Agilent mainframes. The most notable differences that are likely to be encountered are due to PC environment requirements and the Agilent hosting software.

In all three products, 1670X, 1680/90/900 and Offline Viewer, the displaying of the protocol information will all be identical. The decoder identifies all "ordered sets", Fibre Channel frame sections and all of their sub-fields.

Each Fibre Channel frame section will be clearly identified by color and syntax. The decoders identify the Fibre Channel frame sections, e.g. frame header, frame optional headers, payload, and CRC and then display the 32 bit words of each section broken down to their hex sub-field values.

All three products will use color to further identify each state in the decoded listing. The color utilization is as follows:

Ordered Sets ---	Green
Frame Header	Blue
Optional Headers	Blue
Payload	Purple
CRC	Yellow/Red (if CRC value is incorrect)

There are minor differences in the operation of the decoders, for example, the filtering of invalid states is accomplished differently in the two decoders, but the decoders essentially present the identical sets of information.

The capture of Fibre Channel traffic from the FS4320 probe requires the following procedure:

- Hook up the appropriate number of cables
- Load a configuration file
- Set a trigger in the trigger menu (window)
- Arm the FS4320 probe by toggling the “Arm” switch
- Click the green arrow in either the workspace or listing window of the logic analyzer
- Generate Fibre Channel traffic
- When the trigger condition has been met, the analyzer will acquire data.
- Wait for the analyzer buffer to fill and then view the captured traffic in the listing window

1670X Decoder Software

Loading the configuration file will automatically load the Fibre Channel Protocol Decode software (FS4320) onto the workspace. If this does not happen, the user should verify that the decoder software installation was successful.

The FS4320 configuration file, FC4320.___A, should be located in the /logic/configs/FuturePlus/FS4320 directory. The configuration file can be loaded from within File->Load Configuration... pull down menu. To load the configuration, the user must navigate to the configuration file location, enter the file name and then click the “Load” push button located at the bottom left corner of the window (as seen in Figure 3).

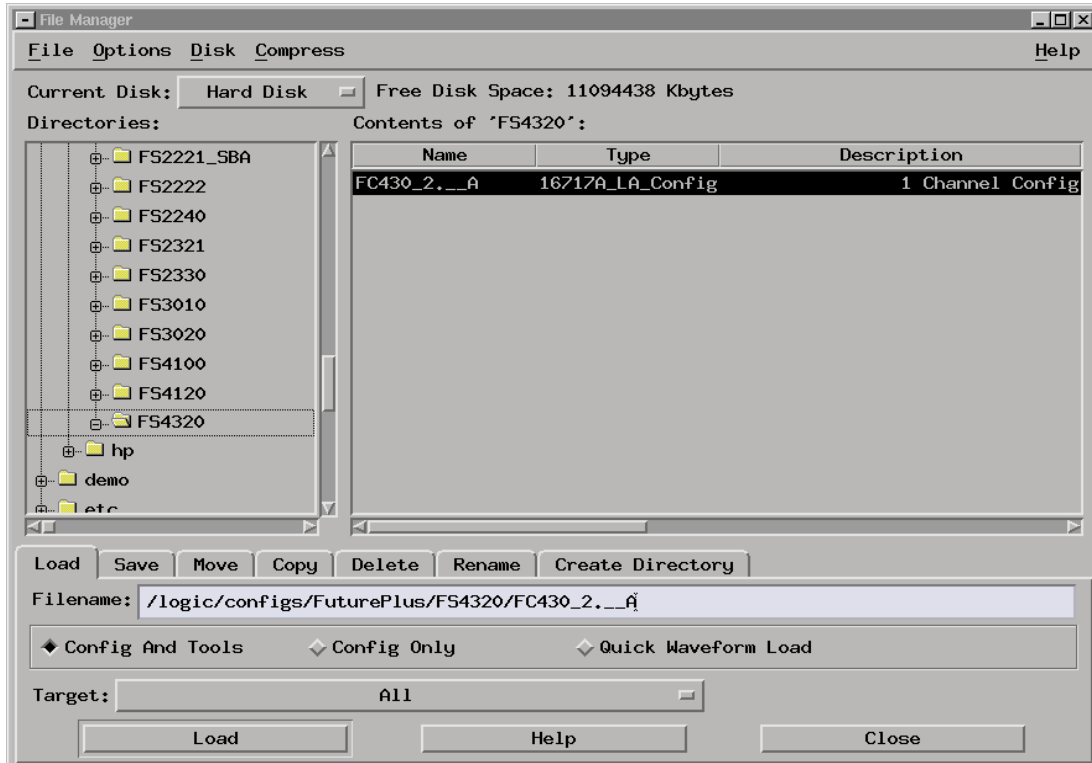


Figure 3 --- File Manager Display

After the configuration file has been successfully loaded, the 1670X workspace will contain the icons as depicted in the Figure 4. From the workspace window, the user can display the logic analyzer Trace File Listing window by double clicking the “Listing<1>” icon and capture Fibre Channel traffic by following the data capture procedure as described at the beginning of this section.

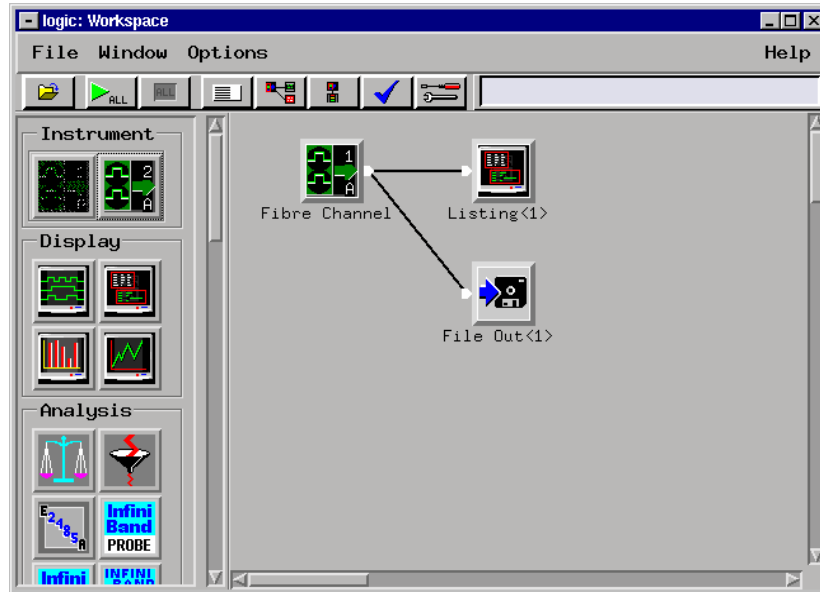


Figure 4 -- 1670X Workspace

The configuration file sets up one logical machine in the 1670X analyzer. The machine is capable of capturing and displaying up to 3 channels of data in hex format. The analyzer can only load one decoder (per logical machine) and thus will only decode one channel of hex data into the Fibre Channel protocol.

NOTE: Two logical machines are required to capture the six channels of data that the FS4320 probe is capable of capturing. To capture all size FC links, the workspace will have to contain a second set of icons to represent the second group of channels being monitored.

The configuration file assumes that the logical machine is monitoring channels ABC and Helper ABC **OR** channels DEF and Helper DEF. Mixing channels of the two groups is not permitted because the decoding of the channel data is dependent on signals contained within the “Helper” pods.

The user can opt to monitor only a subset of the channels within the channel group. For example, the user may only want to monitor channel A and ignore the other two channels. To accomplish this, the user simply needs to ensure that the Channel A and Helper ABC cables are connected to the analyzer. Capturing of the data follows that same procedure that is described in this section’s introduction. This same idea applies to the other two channels within the group.

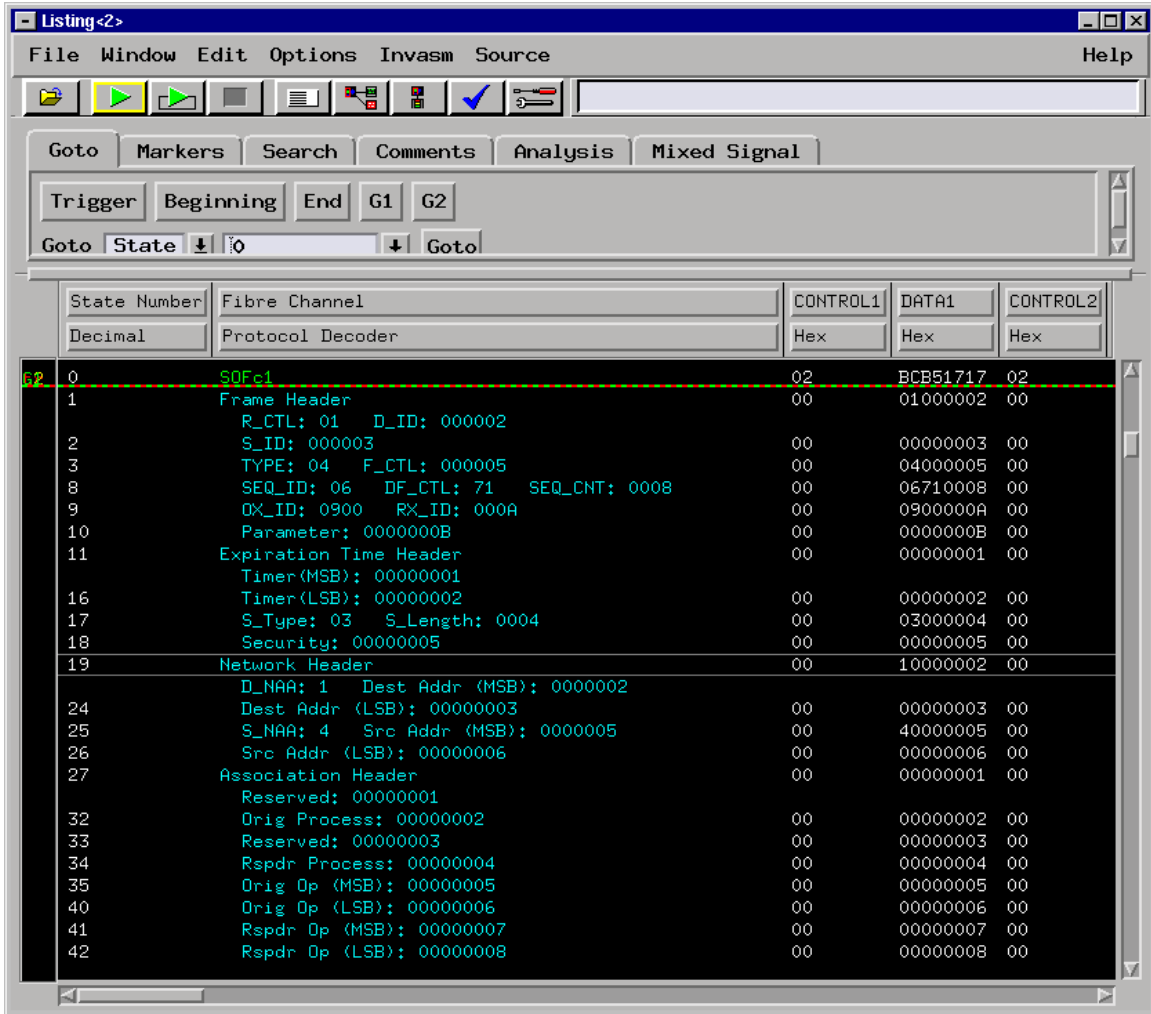


Figure 5 --- 1670X FS4320 Listing

The user may elect to decode any one of the three channels by pulling down the INVASM->Prefs menu item from the listing dialog and select Channel 1, Channel 2 ,or Channel 3 from the Channel Selection options.

It is recommended that if only one channel is to be monitored, then channel A should be the channel used. This recommendation is primarily based on the fact that the user preference's are defaulted to channel A as being the channel that will be decoded.

The preference dialog also allows the user to optionally decode the ASM header.

NOTE: If the user elects to have the ASM header decoded, the decoder assumes that the ASM header will be the first four words after the optional headers in the Fibre Channel frame payload.

The decoder will also assume that every payload will be decoded with the ASM header.

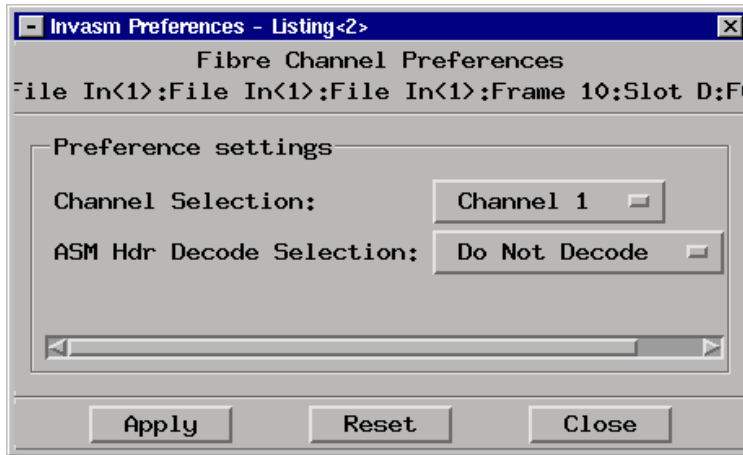


Figure 6 --- User Preference Dialog

Due to the design of FS4320 probe, the state listing does not contain valid data for every state contained in the listing. Consequently, the decoded listing will contain some blank states. The user may remove the invalid states by pulling down the INVASM->filter display and de-select the Invalid State option from within the "Show States of Type" grouping, and click the apply button as shown below.

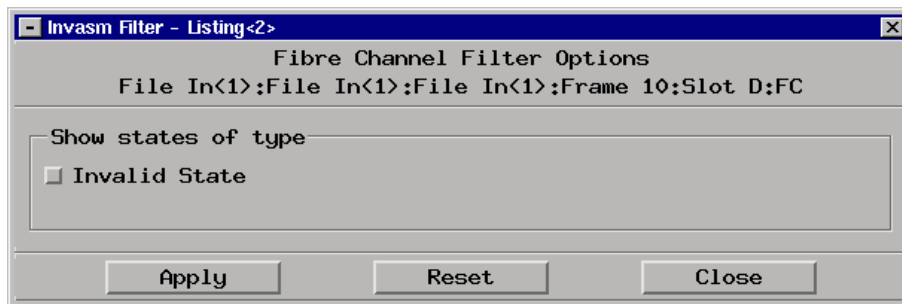


Figure 7 --- 1670X FS4320 Filter Dialog

1680/90/900 Decoder Software

Software installation begins after you have installed the Agilent 1680/90/900 logic analyzer software on your PC or you have a 169xx with the OS installed. Place the CD containing the FS4320 1680/90/900 software in your CD drive, open the drive and execute the .exe program. The installation software will create the necessary directories, and NT registry keys and values in order for the Decoder/IA to work seamlessly with the Agilent Logic Analyzer software.

After the installation finishes loading, license the software, then you can use the FC Protocol Decoder. Your screen views may be slightly different from those shown below, but the actions required are the same.

To load a configuration file select the FS4320 folder that was placed on the desktop during installation. After clicking on the folder, windows explorer should open and display the configuration files available. Select the configuration file that matches your analyzer by double clicking the file name. The analyzer application should launch, load the configuration file, and

load the protocol decoder. If this does not happen, the user should verify that the decoder software installation was successful.

The configuration file can be loaded from within File->Open pull down menu that is contained in the 1680/90/900 logic analyzer window. The user must navigate to the configuration file location, select the configuration file by highlighting it in the display, and then load it by clicking the “Open” pushbutton as seen below.

During the configuration file loading process, the logic analyzer will display the user preference dialog in which the user must specify which FS4320 probe channel (A, B or C) will be decoded. Additionally, the user may alter the setting of ASM Header decoding preference. Refer to Figure 8 below for the user preference dialog example.

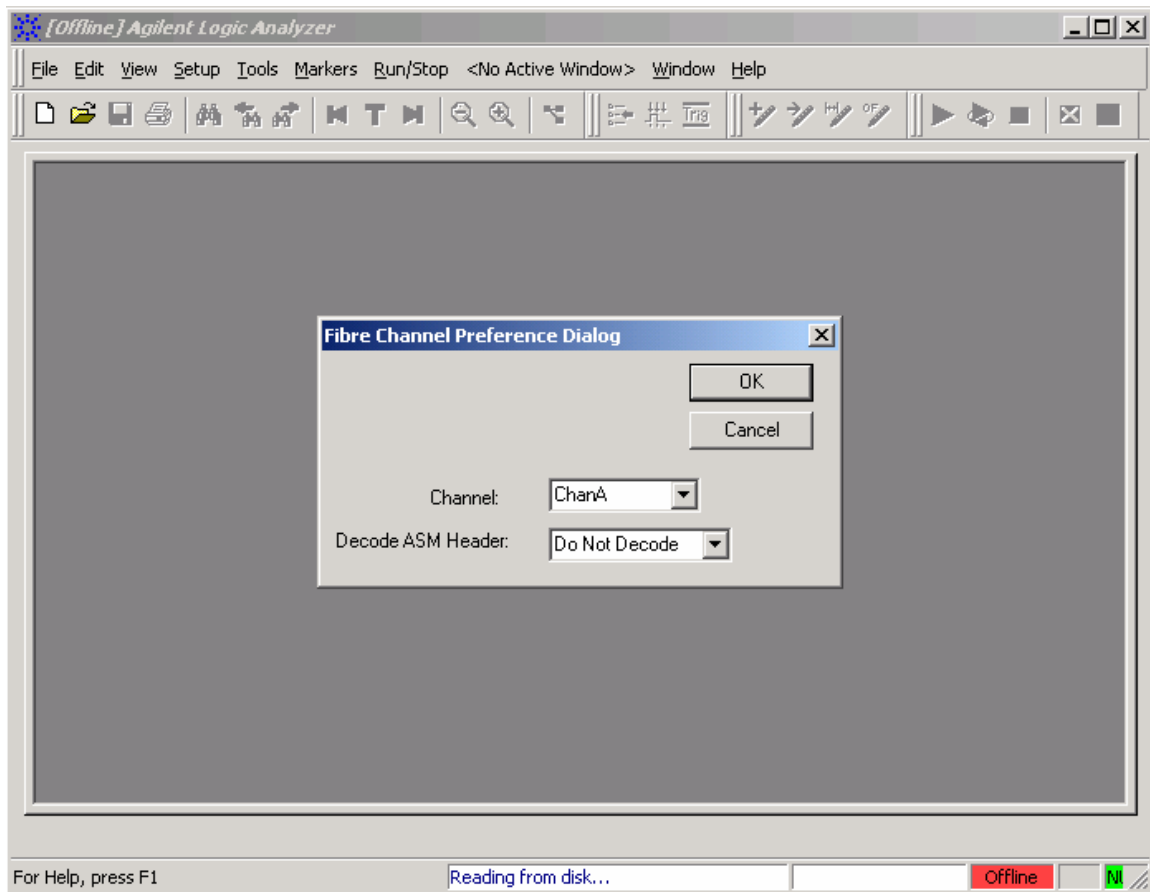


Figure 8--- 1680/90/900 User Preference Dialog

After the initial setting of the user preferences has been accomplished, the 1680/90/900 will display the data listing dialog, from which the user may capture data by following the procedure described in this section's introduction.

The user may elect to decode any one of the three channels by pulling down the Tools->FC Inverse Assembler – 1 - Preferences menu item from the listing dialog and select Channel A, Channel B or Channel C from the Channel Selection option.

It is recommended that if only one channel is to be monitored, then channel A should be the channel used. This recommendation is primarily based on the fact that the user preference's are defaulted to channel A as being the channel that will be decoded.

The preference dialog also allows the user to optionally decode the ASM header.

NOTE: If the user elects to have the ASM header decoded, the decoder assumes that the ASM header will be the first four words after the optional headers in the Fibre Channel frame payload.

The Format switch on the front panel has to be in the ASM position for this preference to work.

The decoder will also assume that every payload will be decoded with the ASM header.

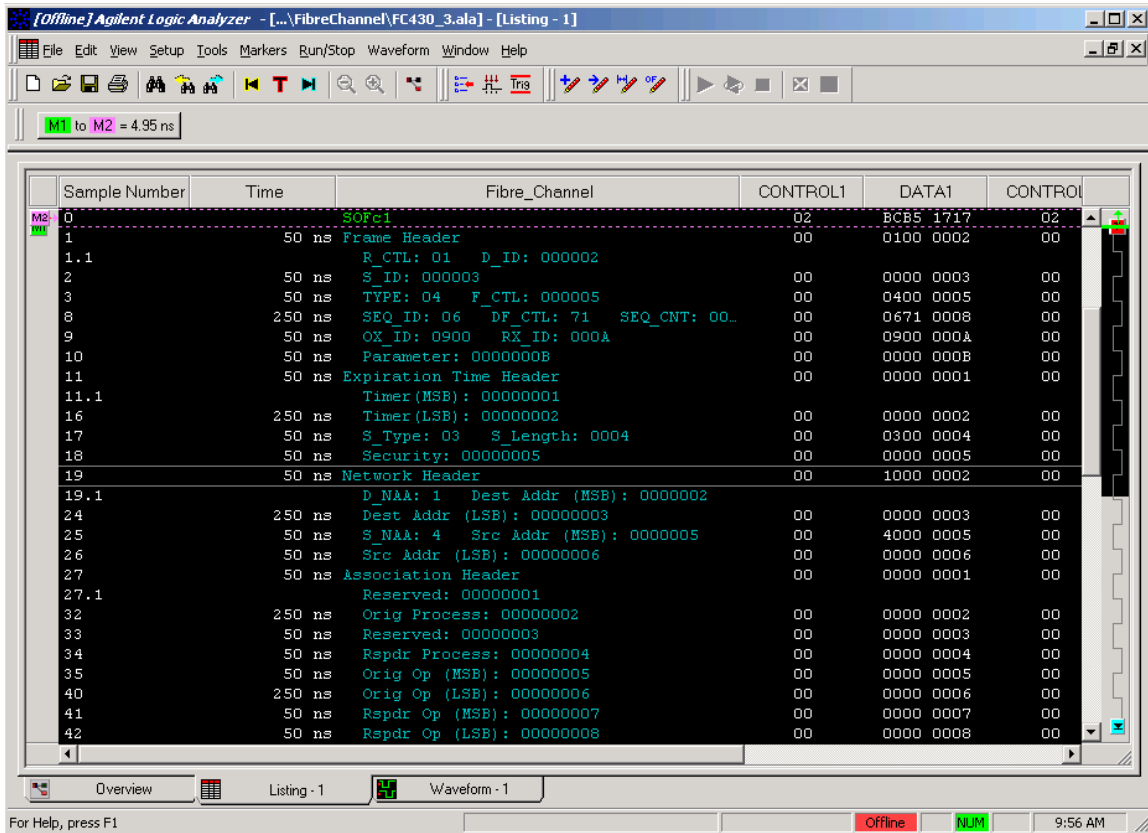


Figure 9

Due to the design of FS4320 probe, the state listing does not contain valid data for every state. Consequently, the decoded listing will contain some blank states. The user may removing the invalid states by pulling down the Tools->filter/colorization pull down menu option and establish a filter based on all occurrences of the 0x20 value contained in the General Tags label.

Offline Viewer Decoder Software

The Off Line Viewer software provides a state analysis environment for data that has been captured on a 1670X or 1680/90/900 analyzer.

The Offline Viewer application is the same as the 1680/90/900 software, but without the capability of capturing data. That is, it is not a full analyzer, but rather a tool that can be used off line to run the decoder on captured data that is stored in a data file.

If the data was captured on a 1680/90/900, the input file to the off line viewer must be a 1680/90/900 configuration file (*.ala) that contains both the setup information and the captured data.

If the data was captured on a 1670X analyzer, the captured data must be stored as a fast binary formatted output file. The trace file can then be migrated to the PC and user may import the fast binary file into the offline viewer program.

Before installing the Fibre Channel Offline Viewer; you must install the Agilent 1680/90/900 logic analyzer software. Refer to the section 1680/90/900 Decoder Software for instructions on how to load the Off Line Viewer onto a PC.

Once the Agilent logic analyzer software has been successfully loaded, the Fibre Channel Offline Viewer can be loaded onto the hard drive of your computer, by placing the FS4320 CD containing the FS4320 1680/90/900 software in your CD drive, opening the drive and executing the FS4320.exe program.

This Fibre Channel Offline Viewing software (FS1122) is a licensed product and is locked to a single PC hard drive. The actual licensing process is performed by Agilent. Registration instructions and requirements are printed on the SW Entitlement certificate provided with this product.

The installation software will create the necessary directories in order for the decoder to work seamlessly with the Agilent Logic Analyzer software. If an attempt to install the Protocol Decoder is made before your Agilent Logic Analyzer software is loaded, the decoder will not be installed properly in your computer's registry files.

After the installation finishes loading you can use the Fibre Channel Protocol Decoder.

The displaying of decoded Fibre Channel information can be accomplished in one of two separate methodologies:

- Importing a data file (and then loading the Inverse Assembler)
- Loading a configuration file

Importing a Data File

The Offline Viewer can display any valid trace file in a hex format by importing the file into the Agilent Logic Analyzer. Once the file has been imported, an Inverse Assembler tool may be invoked to decode the data into a protocol format.

To Import a file, pull down the FILE->Import pull down menu (as seen in the figure below) and navigate to location where the data file resides. Double click the file name of the data file to be imported (as seen in the figure below) and the data will be displayed in the data listing window without any decoding (as seen in Figure 11).

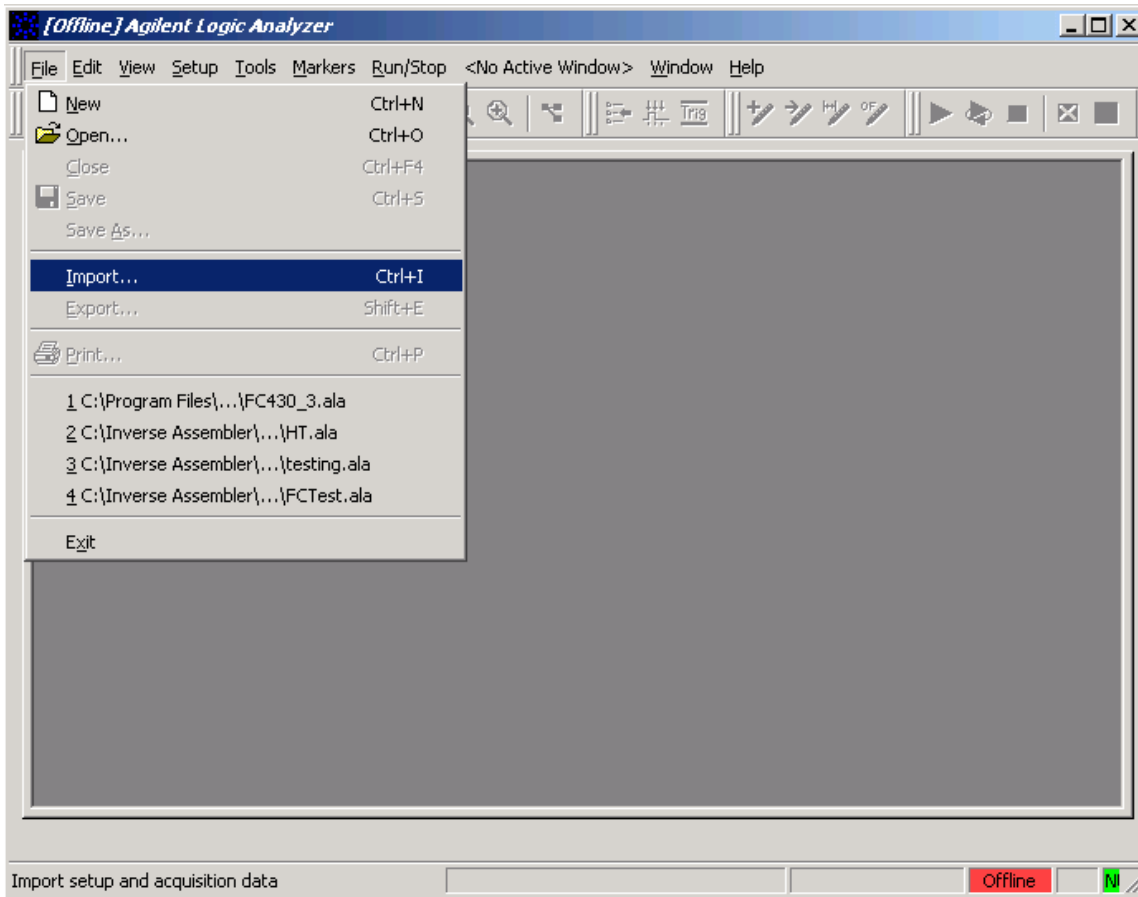


Figure 10--- 1680/90 & Offline Viewer Import Dialog

To decode the hex data into the Fibre Channel information, pull down the Tools->Inverse Assembler menu and select the FC Inverse Assembler tool (as seen in the figure below).

The selection of the FC Inverse Assembler tool will cause the user preference dialog to be displayed. The user will have to either accept the default settings or modify the and then click the OK pushbutton in order for the trace listing to be decoded into the Fibre Channel protocol information.

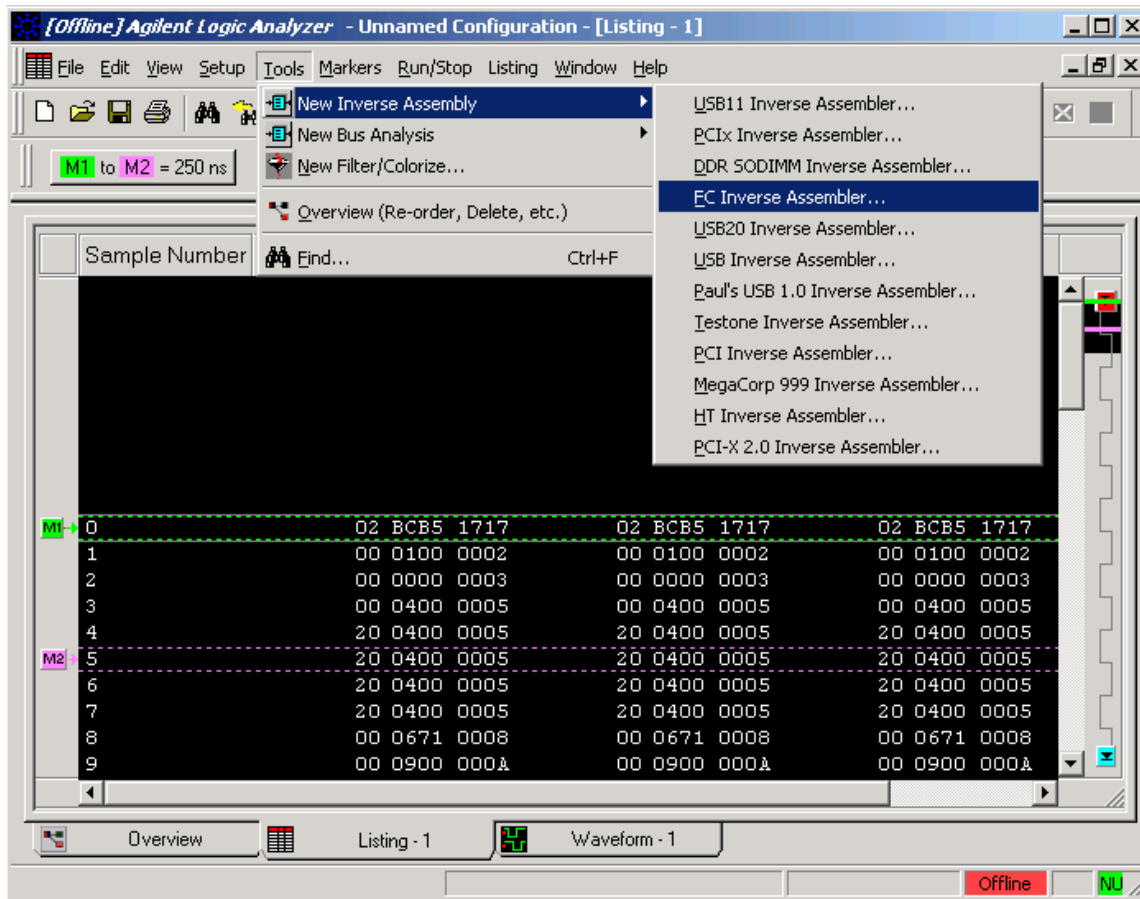


Figure 11--- Inverse Assembler Selection Dialog

The data, in whatever channel the user preferences selected, will be decoded into the Fibre Channel protocol, as seen in figure 9.

NOTE: Figure 8 has a user preference of Channel A being decoded

Creating and Opening a Configuration File

After the first time a data file has been imported and displayed with the Offline Viewer, the user may wish to create a configuration file that can be reused in subsequent viewing of the data.

The configuration file stores (among other things):

- Which labels are displayed in the listing screen
- The order of the labels
- The user preferences
- The user defined filters
- The Inverse Assembler used to decode the data contained in the listing

To save a configuration file, the user must pull down the File->Save As pull down menu and specify the location and file name of the configuration file in the appropriate widgets of the "Save As" dialog.

To open a configuration file, the user pulls down the File->Open pull down menu and specifies the location and file name of the configuration file to be opened. The Offline Viewer will display a data listing dialog without any data being displayed. The labels displayed, as well as their ordering will be the same as when the configuration file was created.

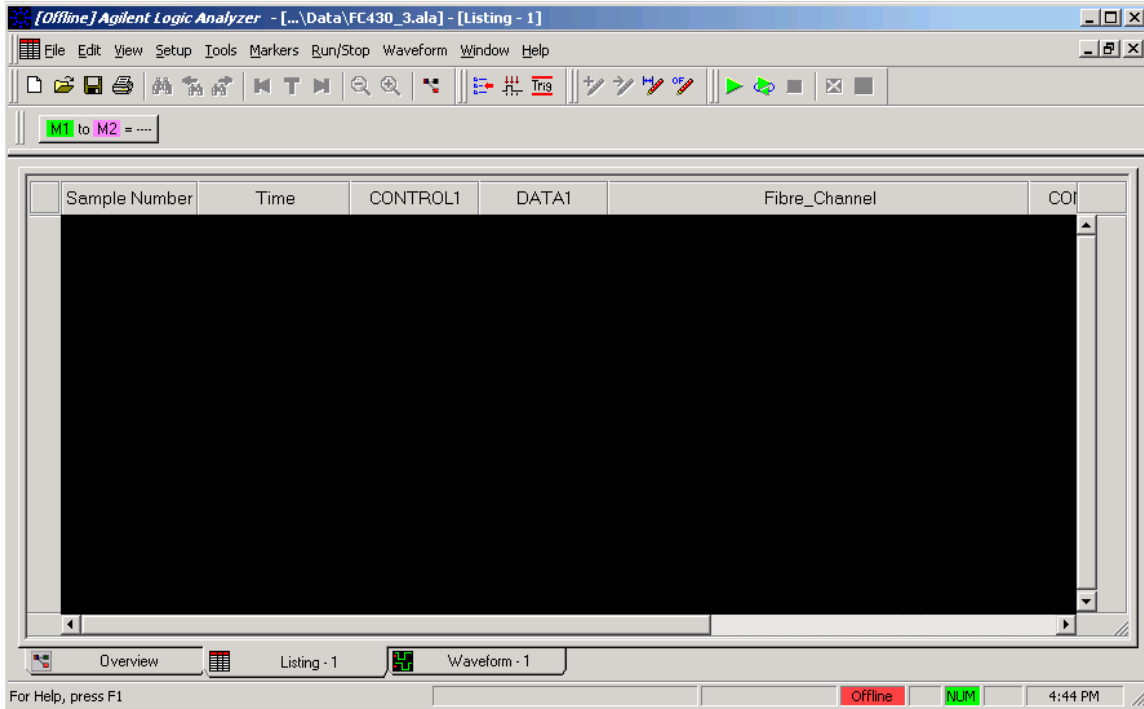


Figure 128 --- Configuration without Data

The user must import an appropriate data file in order to get data to be displayed as seen in Figure 9.

State Analysis

The Protocol Decoder is designed to work with up to 3 channels and the associated Helper signals from the FS4320. If additional channels are brought to the logic analyzer an additional machine needs to be loaded and the Protocol Decoder loaded into that machine.

The FS4320 requires that the Fibre Channel links being monitored are restricted to the follow two sets:

- Channel A, B or C with Helper ABC pod
- Channel D, E or F with Helper DEF pod

Any combination of the channels can be monitored, but channels from the two sets cannot be intermixed. That is, you can monitor channel A and/or Channel B and/or Channel C, but you cannot monitor channel A and/or Channel D, or any other similar combination.

Acquiring Data

This chapter explains how to configure the FS4320 to perform state analysis on the Fibre Channel links. The configuration software sets up the format specification menu of the logic analyzer for compatibility with the output of the FS4320.

Configure the trigger menu to acquire data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full; the trigger specification is TRUE, or when you select STOP.

The logic analyzer will flash “Slow or Missing Clock” if it does not see the Fibre Channel signal CLK toggling.

The logic analyzer will flash “Waiting in level 1” if the trigger specification has not been met.

Preferences

Preferences for the protocol decoder must be set properly depending on what Fibre Channel link is to be decoded. If the preferences are not set properly, incorrect decoding may result. Please check the preferences before you view the listing.

Typical incorrect decoding problems will be the wrong channel is being decoded or the ASM header is not being displayed.

On the 1670X analyzer, the preferences may be viewed by selecting “INVASM” from the listing window, then select “PREFERENCES” and a window like the following will appear on the screen.

On the 1680/90/900 and Offline Viewer, the preferences may be viewed by selecting the tools->FC Inverse Assembler – 1 – Preferences.

Make any changes necessary then select apply. You may change the preferences at any time you deem necessary

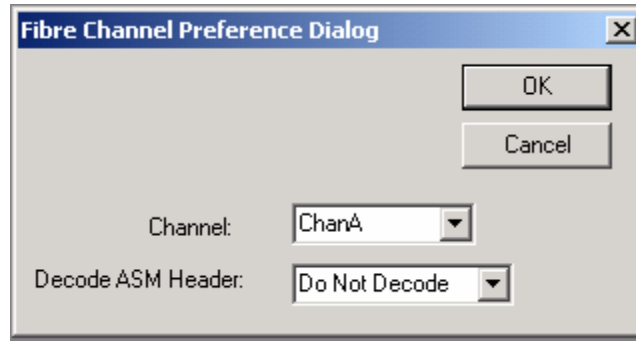


Figure 13--- User Preference Dialog

State Listing Display

The 1670X and 1680/90/900 have identical state listing displays. See Figure 5 and 9 for an example of the 1670X and 1680/90/900 state listing respectively.

The displays contain individual labels for each link as well as the “Helper” signals contained on the Helper ABC or Helper DEF connectors.

The state listing dialog contains only one output label which displays decoded ordered set commands and Fibre Channel Frames.

Frames are composed of several sections, e.g. frame header, optional header, payload, CRC, and their sub-fields.

The Display is capable of showing one set of decoded information for one of the three input links.

In both the 1670X and the 1680/90/900 displays, the labels can be moved to allow the user to personalize the display layout. This allows the user to group the output label in close proximity to the input label being decoded.

Protocol Decode Functionality

The FS4320 Decode Software will perform the following functions:

- ◆ Decode all Fibre Channel Ordered Sets, e.g. SOFc1, EOFt, Idle, etc.
- ◆ Identify Fibre Channel Frame sections, e.g. Frame header, Optional Headers, Payload, CRC
- ◆ Identify all Frame section sub-fields in hex format
- ◆ Identify the ASM header as the first four 32-bit words after the optional headers
- ◆ Identify ASM sub fields in hex format
- ◆ Color code the section header identification description text and the decoded sub-field hex values to match the frame section type (command). The colors used by the software are as follows:
 1. Ordered Sets --- Green
 2. Frame Header Blue
 3. Optional Headers Blue
 4. Payload Purple
 5. CRC Yellow/Red (if CRC value is incorrect)

Triggering and Symbols

Symbols are provided for the various SOF and EOF for triggering or filtering of data. The label that has symbols for SOF's is SOFTYP. The label that has symbols for EOF's is EOFTYP. To use symbols simply choose either SOFTYP or EOFTYP depending on what you are trying to capture from the trigger format specification or default storing and change the label format from Hex to Symbol. Click on the value of the label and you should be presented with a list of symbols available for that label, select the symbol you want and it will appear in the box next to the label. Below are the labels with the symbols and value of each symbol. When you use the 3 channel config there will be 3 sets of SOFTYP labels and 3 sets of EOFTYP labels, each label will have a number (ex. SOFTYP1 label for channel A or D depending on which channel analyzer is attached to).

SOFTYP Label

Symbol	Data 31-0
SOFC1	BCB51717
SOFI1	BCB55757
SOFN1	BCB53737
SOFI2	BCB53535
SOFI3	BCB55656
SOFN3	BCB53636
SOFf	BCB55858

EOFTYP Label

Symbol	Data 31-0
EOFt	1011 1100 10X1 0101 0111 0101 0111 0101
EOFdt	1011 1100 10X1 0101 1001 0101 1001 0101
EOFa	1011 1100 10X1 0101 1111 0101 1111 0101
EOFn	1011 1100 10X1 0101 1101 0101 1101 0101
EOFdti	1011 1100 10X0 1010 1001 0101 1001 0101
EOFni	1011 1100 10X0 1010 1101 0101 1101 0101

Traffic Generation Function – Optional product FS1121

The FS4320 hardware provides a simple test generator enabled by the “Test”, “Format”, and “Test Pat” front-panel switches and has been detailed in a previous section of this manual.

The FS4320 probe with the optional FS1121 software running on a PC connected to the FS4320 through it's rear panel male DB25 connector has additional transmit capability described in this section.

When the generator GUI window is opened, simple pattern generation or Repeat/Tee mode retransmission is halted and IDLE words (ASM/FC) or zero-length data packets (FPDP) are

transmitted on all channels. The capability offered by the Ctrl pattern generator option is independent, low-level control of up to six transmit channels and the ability to send and loop on up to 64 KB of user data. The optional software is available as FuturePlus product FS1121.

Intended to be used for a variety of related protocols and applications, the FS4320 Ctrl generator GUI window configures the FS4320 channel pairs [A/B, C/D, E/F] so that they output the same data (i.e. channel pairs share the same generator) allowing the user to construct test data sequences called "packets" (not to be confused with FPDP, ASM, or FC protocol packets). An FS4320 Ctrl packet is just a variable length play-list of 32-bit data elements (each with associated attribute flags). Once constructed, the user can select a packet and request it be downloaded to the FS4320 and played once or looped out of one of the three channel pairs. When packet data is not explicitly being transmitted through the GUI or DLL, either IDLE ordered-set (ASM/FC) or zero-length data packets (FPDP) are output.

For convenience, the generator provides mnemonics for common FPDP, ASM, FC protocol elements, i.e. ordered-sets, FPDP zero-length data, EOT and BOT packets, FC and ASM packet templates. In addition, a special CRC mnemonic can be inserted that will automatically compute the corresponding CRC value for preceding data entries (up until an element with its ordered-set flag set).

Packet Construction

FS4320 Ctrl packets or play-lists are created and deleted using the 'New Packet' and 'Delete Packet' buttons respectively. When a new packet is created, a default name <new#> is entered into the packet name selection box and the main list-box is cleared. The packet name can be changed at any time by editing it in the selection box. The selection box also lets you choose from among all the user's defined packets either for editing or playback.

Elements are added to a packet with the 'Insert...' button, which brings up a pop-up menu presenting various options to the user. The element is inserted at the line currently highlighted in the list-box or at the end of the packet if no line is highlighted. Selecting 'Data...' from the pop-up insertion menu brings up a dialog box, allowing the user to name the data field, enter its value, set a repeat count, and set its flags. One flag is the 'Comma' flag, identifying the data element as a Fibre Channel ordered-set. Another flag is the 'Step' flag, identifying the data element as the start of a new packet step (see the section on step-triggering below). A third flag that is not set in the data entry dialog, but is displayed in the packet list-box, is the CRC flag. This flag is set implicitly when you insert a CRC word into the packet.

When a CRC word is inserted into a packet, its value is automatically computed from the data words (i.e. words without its comma flag set) immediately preceding the CRC word up until a word with its comma flag set. This behavior is consistent with the rules for creating FPDP, ASM, and FC protocol packets. Also, an FS4320 Ctrl packet can comprise multiple protocol packets, each with their own CRC. Note that any change to the packet will re-compute all of its CRC words so they are always correct. Also, during playback, if CRC mode is off, the CRC words in packets are not played.

To delete an element in a packet, simply click on the appropriate line in the list-box and press the Delete key. To delete multiple elements, use the common Windows rules for selecting groups of lines (i.e. select one line then shift-click on another to select a range or ctrl-click on lines individually to add them to the selection), then press the Delete key. To edit an already existing element in a packet, double-click it in the list-box. Except for CRC words (which can't be edited), this will bring up the data entry dialog with the fields appropriately filled in. Note that the name field (denoted as 'type' in the list-box) is merely a user or default label and is not used in any way by the software. Thus, default labels can be changed, even labels with protocol meaning such as SOF, MEOF, etc.

Finally, a few keyboard shortcuts are available for data entry and packet editing. With the packet list-box as the keyboard focus, the user can press 'd' to insert a data element (pops up the data-entry dialog box). Also, the user can highlight a data entry and use the up-arrow and down-arrow keys to move it up and down within the packet respectively.

Saving Packet Configurations

The current packet configuration is saved to the file 'defaultFCA.cfg' when the application closes. Similarly it is restored from this file when the application is restarted. In addition, the File menu of the generator window offers 'Save Cfg...' and 'Load Cfg...' options that explicitly save and load the packet configuration.

Packet Playback

Controls at the bottom of the generator window facilitate looping or single-shot playback of the currently selected packet. The 'Channel' selection box determines which channel is to be controlled. As each channel can be independently controlled, selecting a new channel when in looping or step-trigger mode will not affect the current channel's playback status (i.e. it will continue looping or remain armed for a subsequent trigger in step-trigger mode). The 'Loop' check box configures a channel for loop playback. Left unchecked, when a packet is sent and played, it will play only once. Otherwise, it will loop repeatedly until stopped. The loop modifier also applies to step-trigger mode, allowing the step sequence of a packet to repeat with continued triggering.

The 'Step Trigger En' check box configures the FS4320 for step-trigger mode. Note that this mode applies to all channels, not just the currently selected channel. The 'Send/Play' button downloads the current packet to the channel playback memory of the FS4320 and enables playback. Depending on the loop and step-trigger mode settings, the channel will play once, loop repeatedly, or wait for a software or hardware trigger to begin playing. The 'Trigger' button is used to generate a software trigger event. It is enabled when step-triggering is enabled (i.e. 'Step Trigger En' is checked).

Step-trigger mode allows packets to comprise smaller sequential 'steps', each step being a unit that plays out in response to a trigger event. A trigger event in this context is either an assertion of the step-trigger input signal on the custom I/O connector of the FS4320 or a software trigger caused by the GUI trigger button or Trigger routine of the DLL. Please note this definition does not include the TrigIn and LA TrigIn inputs or the Arm front-panel switch.

A packet step is defined by setting a data element's step flag true, denoting the first word of the step. The first data element implicitly defines the first packet step. Indeed, if no element in the packet has its step flag set, the entire packet is the one and only step. For example, a packet could be repeatedly sent, once per trigger event, by setting the loop flag and operating in step-trigger mode.

One restriction in defining packet steps is that each step must be at least three words in length. This is due to the pipelining architecture of FS4320 playback. Packets that do not meet this criterion will flag an error message and will not download and play.

Example

Suppose you wanted to configure two channels to play the FPDP protocol packet sequences: (sync w/o data pkt, data pkt0, sync w/data pkt) and (sync w/o data pkt, data pkt1, sync w/data pkt). First, you would define the FS4320 Ctrl packets as follows:

- 1) Click on New Pkt button, edit the name to 'ChAPkt'.
- 2) Click on Insert..., select FPDP->Sync W/O Data Pkt
- 3) Click on Insert..., select FPDP->Zero Length Data Pkt

- 4) Click on Insert..., select FPDP->Sync W/Data Pkt
- 5) Edit the data value in data entry dialog that pops up for the Sync W/Data Pkt and click OK.
- 6) Select the CRC entry for the zero-length data packet (second CRC).
- 7) Type 'd' to insert a data element, enter '11111111' and type <return>.
- 8) Double-click on the second IDLE word (of the former zero-length data pkt)
- 9) Check the 'Step' box and type <return>.
- 10) Double-click on the SWDV word (or the Sync W/Data Pkt).
- 11) Check the 'Step' box and type <return>.
- 12) Repeat steps 1-11 for the second channels FS4320 Ctrl packet. Edit the packet name in step 1 to 'ChCPkt' and use the data value of '22222222' in step 7.

Next, we want to download the packets into channel playback memory and prepare for step-trigger playback.

- 1) Select 'ChAPkt' in the packet name box to make it current.
- 2) Click on 'Loop' and 'Step-trigger' check boxes.
- 3) Select 'Chan A/B' (FS4320) or 'Chan A' (FS4320) in the Channel selection box.
- 4) Click on 'Send/Play'.
- 5) Select 'ChCPkt' in the packet name box to make it current.
- 6) Select 'Chan C/D' in the Channel selection box.
- 7) Click on 'Send/Play'.

The probe is now configured to step and loop through the three protocol packet sequence on both channels in response to either a hardware trigger or software trigger. Clicking on 'Trigger 1' causes both channels to output the Sync W/O Data Pkts and the button label increments to 'Trigger 2'. Clicking the button again sends out the data packets. And clicking once more sends the Sync W Data Pkts.

Program Window

The programming window is used to upgrade the FS4320 firmware in the field. Bring the dialog up from the control window using the 'Control->Program...' menu option. While this dialog supports password protected features such as programming serial numbers and encoding firmware files, the only option available to users is programming the FS4320.

To upgrade the firmware of your FS4320 box, type in or browse for the .fca firmware file, and click the program button. The status bar at the bottom of the window will update the progress of the firmware upgrade. Click the 'Done' button to close the dialog when programming has completed.

DLL

Instead of using the FCACtrl.exe application, users can make use of the library FCACtrl.dll to interface with the FS4320 hardware. The DLL provides routines to control the front-panel switch state as well as download, play, and step-trigger generator packets.

In addition, using the remote-control feature of the GUI, FCACtrl.dll provides FS4320 control capability over a network. See the header file FCACtrl.h for more detailed documentation on the DLL routines. They are:

- int fcaOpen(int lpt, char* IPAddr);
- void fcaClose();
- long fcaControl(long crc, long xmit, long rate, long mode, long format, long link, long pattern, long ASMfilter, long msgID);
- long fcaARM();
- long fcaLoadAndPlay(long* data, long* flags, long cnt, long chan, long loop, long stepTriggerMode); long cnt, long chan, long loop);
- long fcaSWTrigger(long chan);
- long fcaStopPlay(long chan);
- float fcaGetVersion();
- long fcaComputeCRC32(long* data, long cnt);

The routines `fcaOpen` and `fcaClose` open and close respectively a local parallel port or remote TCP connection to an FS4320. In the remote case, the TCP connection is actually made to the `FCACtrl.exe` application running on the PC that owns the physical parallel port connection to the FS4320. The FS4320 Ctrl application must be explicitly set up to receive incoming TCP connections (only one at a time). This is done using the 'Control-Remote Control' menu option in the GUI control window.

Control of the front-panel FS4320 switches is achieved using the `fcaControl` and `fcaARM` routines. Generator playback is managed with the `fcaLoadAndPlay`, `fcaSWTrigger`, and `fcaStopPlay` routines. Finally, `fcaGetVersion` returns the DLL version and `fcaComputeCRC32` computes the CRC32 syndrome necessary for constructing FPDP/FC/ASM protocol packets.

General Information

Probe Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS4320 probe.

Standards Supported

Fibre Channel specification ANSI INCITS 230-1994 (R1999) Physical and Signaling Interface. Speeds of 1.0625Gbps or 2.125Gbps.

Power Requirements

100-240VAC, 1 amp.

Logic Analyzer Required

Agilent 16715/6/7/9, 16740/1/2, or 16750/1/2 installed in the 16700A or 16700B mainframe, 169xx mainframe, 1680/90.

Number of Probes Used

The FS4320 Probe interface uses 4 cable headers for 3 FC Channel outputs and it's associated Helper signals.

E5378 (FS1014) for use with 16753-6 cards

E5385 (FS1015) for use with 1671X or 16750-2 cards

FC Probe State Clock Frequency

55 Mhz

Environmental Temperature

Operating: 0 to 45 degrees C (+32 to +113 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 90% non-condensing. Avoid sudden, extreme temperature changes which would cause condensation on the FS2009 module.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the FS4320 module. If a failure is suspected in the FS4320 module contact the factory or your FuturePlus Systems authorized distributor.

Connector Pinouts – Channels D, E, and F are duplicates of A, B, and C

Probe Channel A Output

Probe Signal name	Logic Analyzer channel # - Odd	Mictor pin Odds	Mictor pin Evens	Logic Analyzer channel # Even	Probe Signal name
Valid1	CLK/16	5	6	CLK/16	Clk 1
Data1_31	15	7	8	15	Data1_15
Data1_30	14	9	10	14	Data1_14
Data1_29	13	11	12	13	Data1_13
Data1_28	12	13	14	12	Data1_12
Data1_27	11	15	16	11	Data1_11
Data1_26	10	17	18	10	Data1_10
Data1_25	9	19	20	9	Data1_9
Data1_24	8	21	22	8	Data1_8
Data1_23	7	23	24	7	Data1_7
Data1_22	6	25	26	6	Data1_6
Data1_21	5	27	28	5	Data1_5
Data1_20	4	29	30	4	Data1_4
Data1_19	3	31	32	3	Data1_3
Data1_18	2	33	34	2	Data1_2
Data1_17	1	35	36	1	Data1_1
Data1_16	0	37	38	0	Data1_0

Probe Channel B Output

Probe Signal name	Logic Analyzer channel # - Odd	Mictor pin Odds	Mictor pin Evens	Logic Analyzer channel # Even	Probe Signal name
Valid2	CLK/16	5	6	CLK/16	Clk 1
Data2_31	15	7	8	15	Data2_15
Data2_30	14	9	10	14	Data2_14
Data2_29	13	11	12	13	Data2_13
Data2_28	12	13	14	12	Data2_12
Data2_27	11	15	16	11	Data2_11
Data2_26	10	17	18	10	Data2_10
Data2_25	9	19	20	9	Data2_9
Data2_24	8	21	22	8	Data2_8
Data2_23	7	23	24	7	Data2_7
Data2_22	6	25	26	6	Data2_6
Data2_21	5	27	28	5	Data2_5
Data2_20	4	29	30	4	Data2_4
Data2_19	3	31	32	3	Data2_3
Data2_18	2	33	34	2	Data2_2
Data2_17	1	35	36	1	Data2_1
Data2_16	0	37	38	0	Data2_0

Probe Channel C Output

Probe Signal name	Logic Analyzer channel # - Odd	Mictor pin Odds	Mictor pin Evens	Logic Analyzer channel # Even	Probe Signal name
Valid1	CLK/16	5	6	CLK/16	Clk 1
Data3_31	15	7	8	15	Data3_15
Data3_30	14	9	10	14	Data3_14
Data3_29	13	11	12	13	Data3_13
Data3_28	12	13	14	12	Data3_12
Data3_27	11	15	16	11	Data3_11
Data3_26	10	17	18	10	Data3_10
Data3_25	9	19	20	9	Data3_9
Data3_24	8	21	22	8	Data3_8
Data3_23	7	23	24	7	Data3_7
Data3_22	6	25	26	6	Data3_6
Data3_21	5	27	28	5	Data3_5
Data3_20	4	29	30	4	Data3_4
Data3_19	3	31	32	3	Data3_3
Data3_18	2	33	34	2	Data3_2
Data3_17	1	35	36	1	Data3_1
Data3_16	0	37	38	0	Data3_0

Channel ABC Helper Signals

Probe Signal name	Logic Analyzer channel # - Odd	Mictor pin Odds	Mictor pin Evens	Logic Analyzer channel # Even	Probe Signal name
Clk1	CLK/16	5	6	CLK/16	BOTA
EOTA	15	7	8	15	SpareAB4
HoldBOTA	14	9	10	14	SpareAB3
NC	13	11	12	13	NC
SpareAB0	12	13	14	12	SpareCD1
BadCRCA	11	15	16	11	User3
SpareAB2	10	17	18	10	SpareCD0
BadCRCB	9	19	20	9	BOTC
BadCRCC	8	21	22	8	SpareCD2
HoldBOTC	7	23	24	7	User1
SpareAB1	6	25	26	6	NC
NC	5	27	28	5	BOTB
EOTB	4	29	30	4	HoldBOTB
CommaB	3	31	32	3	User0
CommaA	2	33	34	2	User4
CommaC	1	35	36	1	User2
EOTC	0	37	38	0	User5

Rear Panel Connections

The female DB25 connector labeled “Custom I/O” has the following pinout:

- 1 – 3.3Volts DC via 100 ohm resistor
- 2 – “HelperABC” user bit 0
- 3 – “HelperABC” user bit 1
- 4 – “HelperABC” user bit 2
- 5 – “HelperABC” user bit 3
- 6 – “HelperABC” user bit 4
- 7 – “HelperABC” user bit 5
- 8 – “HelperDEF” user bit 0
- 9 – “HelperDEF” user bit 1
- 10 – “HelperDEF” user bit 2
- 11 – “HelperDEF” user bit 3
- 12 – “HelperDEF” user bit 4
- 13 – 5 Volts DC via 100 ohm resistor
- 14 - ground
- 15 – “HelperDEF” user bit 5
- 16 – ground
- 17 – Uncommitted, make no connection
- 18 - ground
- 19 – Uncommitted, make no connection
- 20 - ground
- 21 – Uncommitted, make no connection
- 22 - ground
- 23 – Uncommitted, make no connection
- 24 - ground
- 25 – Uncommitted, make no connection

The user bits accept TTL levels, preferably externally limited to 3.3 volts.

There is a connector labeled “TMPC Only” . Make no external connection to this connector.

A grounding post is also provided on the rear panel.