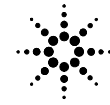


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# **IEEE1394 Analysis Probe FS4200**

## **Users Manual**

**For Agilent Technologies Logic Analyzers**

**Revision 1.6**

<b>HOW TO REACH US</b>	<b>5</b>
<b>PRODUCT WARRANTY</b>	<b>6</b>
<b>Limitation of warranty</b>	<b>6</b>
Exclusive Remedies	6
<b>Assistance</b>	<b>6</b>
<b>INTRODUCTION</b>	<b>7</b>
<b>How to Use This Manual</b>	<b>7</b>
<b>Document Notation</b>	<b>7</b>
<b>ANALYZING THE IEEE1394 SERIAL BUS</b>	<b>8</b>
<b>Accessories Supplied</b>	<b>8</b>
<b>Minimum Equipment Required</b>	<b>9</b>
<b>Setting up Analyzers installed in the 16500 mainframe and portable logic analyzers</b>	<b>9</b>
<b>Setting up the 16600/16700 Analyzer</b>	<b>10</b>
<b>Setting up the 169xx Analyzer</b>	<b>10</b>
<b>Loading 169xx configuration files and General Purpose Probe feature</b>	<b>10</b>
<b>Offline Analysis</b>	<b>11</b>
<b>Powering the IEEE1394 Analysis Probe</b>	<b>12</b>
<b>Connecting to the IEEE1394 Analysis Probe for 165xx or 167xx users</b>	<b>12</b>
State Analysis Only	12
State and Timing Analysis using a 6 POD Logic Analyzer card	12
State and Timing Analysis using Two 4 POD Logic Analyzer Cards	13
State and Timing Analysis using two Logic Analyzer Cards in Master & Expansion Configuration	13
<b>Installing the IEEE1394 Analysis Probe</b>	<b>13</b>
<b>165xx and 167xx Logic Analyzer Configuration Files</b>	<b>14</b>
<b>169xx Configuration files</b>	<b>15</b>
The IEEE1394 Inverse Assembler	15
<b>The Format Menu</b>	<b>16</b>
The STAT variable	16
The ADDR and DATA variables	16

Other Labels and Symbols	16
<b>Theory of Operation</b>	<b>16</b>
The PHY Interface to the IEEE1394 Serial Bus.	16
Configuration Rom Implementation	16
Self ID and Reading the "Company_ID"	17
The interface to the Logic Analyzer	17
<b>LED Indicators</b>	<b>18</b>
+5V LED	18
+3.3V LED	18
READY LED	18
IEEE1394 BUSY LED	18
<b>STATE ANALYSIS</b>	<b>19</b>
<b>Installation Quick Reference</b>	<b>19</b>
<b>Acquiring Data</b>	<b>19</b>
<b>The State Listing Display</b>	<b>20</b>
<b>Using Symbols to Trigger in State Mode.</b>	<b>20</b>
Triggering on a Packet Type	21
Triggering on a Destination Address	21
Triggering on a Source Address	21
Triggering on a Combination of Packet Fields.	21
<b>Qualifying Storage of Packets</b>	<b>21</b>
<b>Filtering Data Payload</b>	<b>21</b>
<b>Error Messages</b>	<b>21</b>
"ERR: PHY packet check failed."	21
"ERR: PHY packet type not recognized"	21
"ERR: Invalid Trans Label"	22
"ERR: Invalid Retry Code"	22
"ERR: Invalid Trans Label & Retry Code"	22
"ERR: Invalid Priority"	22
"ERR: Invalid Trans Label & Priority"	22
"ERR: Invalid Retry Code & Priority"	22
"ERR: Invld Trans Lbl, RT Code & Priority"	22
"ERR: Invalid Dest ID for CYCLE START:"	22
"ERR: Invalid destination offset" CYCLE START	22
"ERR: INVALID Data Length"	22
"HDR CRC ERR: RCVD CRC= "	22
"ERR: Reserved TCODE field in a Primary Packet."	22
"Invalid Extended TCODE= "	22
"ACK Parity Error"	23
"ERR: Input data Error - Aborting"	23
"ERR: Expected End of Packet not found; "	23
"ERR: EOP/CRC PROBLEM"	23
"DATA CRC ERR: RCVD CRC= "	23
"ERR: Packet not an integral number of quadlets"	23

<b>Post Processing Filters</b>	<b>23</b>
<b>TIMING ANALYSIS AND VIEWING THE IEEE1394 SERIAL BUS.</b>	<b>25</b>
<b>Installation Quick Reference</b>	<b>25</b>
<b>Timing</b>	<b>25</b>
<b>GENERAL INFORMATION</b>	<b>27</b>
<b>Characteristics</b>	<b>27</b>
Analysis Probe Interface Compatibility	27
Standards Supported	27
Power Requirements	27
Logic Analyzer Required	27
Number of Probes Used	27
Maximum Speed	27
Operations	27
Environmental Temperature	27
Altitude	27
Humidity	27
Testing and Troubleshooting	28
Servicing	28
<b>APPENDIX A: FORMAT DEFINITIONS</b>	<b>29</b>
<b>State Formats</b>	<b>29</b>
<b>Timing Format</b>	<b>32</b>

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# Introduction

The IEEE1394 Analysis Probe module provides a complete interface between an IEEE1394-95 or IEEE1394A serial bus and Agilent Logic Analyzers. The on board logic provides a physical (PHY) layer interface to the IEEE1394 bus and decodes transaction packets. The IEEE1394 Analysis Probe is a bus monitor that does not generate transactions on the IEEE1394 serial bus.

The configuration software sets up the format, configuration and trigger specification menu of the logic analyzer for compatibility with the IEEE1394 serial bus. When the state configuration file is loaded, an inverse assembler is also loaded which decodes IEEE1394 transactions into easy to read mnemonics.

This manual is organized to help you quickly find the information you need.

## How to Use This Manual

- **Analyzing the IEEE1394 Serial Bus** chapter introduces you to the IEEE1394 State Analysis Probe and lists the minimum equipment required and accessories supplied for IEEE1394 bus analysis.
- The **State Analysis** chapter explains how to configure the IEEE1394 State Analysis Probe to perform state analysis on your IEEE1394 serial bus.
- The **General Information** chapter provides some general information including the operating characteristics for the IEEE1394 State Analysis Probe module and the cable header pinout.

## Document Notation

This operating manual uses the terms and naming conventions of the IEEE1394 specification. In particular the term “quadlet” is used to denote a 4 byte unit of data.

# Analyzing the IEEE1394 Serial Bus

This chapter introduces you to the IEEE1394 Analysis Probe and lists the minimum equipment required and accessories supplied for IEEE1394 Serial Bus analysis.

## Accessories Supplied

The IEEE1394 Analysis Probe product consists of the following accessories:

- The State Analysis Probe interface hardware, which includes the interface circuit module.
- The inverse assembly and configuration software on a 3.5 inch diskettes for 16500 and 167xx frames
- Executable file on CD to install configuration files and inverse assembler on 169xx frames.
- One IEEE1394 cable.
- Documentation CD
- Software Entitlement certificate for 1690x or Offline Inverse Assembler software licensing.

## The FS4200 IEEE1394 Analysis Probe module



### Minimum Equipment Required

The minimum equipment required for analysis of an IEEE1394 Serial Bus consists of the following equipment:

- 1660A/C, 1661A/C, 1662A/C, 16550A, 16554A, 16555A, 16556A, 16557A, 1670A, 1671A, 1672A, 16600, 16601, 1602, 16603, 16710, 16711, 16712, 1674x, 16750-2, 1690x.
- The IEEE1394 Analysis Probe Product
- An IEEE1394 target bus
- IEEE1394 cables ( 1supplied

### Setting up Analyzers installed in the 16500 mainframe and portable logic analyzers

The logic analyzer can be configured for IEEE1394 analysis by loading the IEEE1394 configuration file. Loading this file will load the IEEE1394 Serial bus inverse assembler and configure your logic analyzer. To load the configuration and inverse assembler:

1. Insert the diskette labeled **16500 IEEE1394 Analysis Probe Software for the FS4200** into the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the appropriate configuration file (see table below).
3. Execute the load operation to load the file into the logic analyzer that the IEEE1394 Analysis Probe module is connected to. **DO NOT SELECT ALL OR SYSTEM.**

## Setting up the 16600/16700 Analyzer

The 16600/16700 requires a special install procedure to install the FS4200 software. To accomplish this, insert the diskette labeled **16600/16700 IEEE1394 Analysis Probe Software for the FS4200** into the 16600/700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. The package FS4200 will now appear. Select it and then select *INSTALL*. **This procedure does not need to be repeated. It only needs to be done the first time the IEEE1394 Analysis Probe is used.**

When this has completed restart the logic analysis session and either invoke the *Setup Assistant* from the logic analyzer screen or load the appropriate configuration file from the **configs/FuturePlus/FS4200** directory. The Setup Assistant will guide you in configuring the logic analyzer. Select *Full Measurement* and click the Next button. Now select "FuturePlus" from the *Target Manufacturer* column, "IEEE1394" from the *Target Model Number* column and "FuturePlus Systems FS4200" from the *Product No.* column. Click Next and then follow the connection instructions.

If you prefer to load the configuration files yourself please refer to the section 165xx and 167xx Logic Analyzer Configuration Files on page 14 of this manual for a list of analyzers and corresponding configuration files.

**NB:** The Logic Analysis System's Operating System must be version **A.01.20.00** to be compatible with the software provided on the installation diskette.

## Setting up the 169xx Analyzer

A CD containing the 16900 software is included in the FS4200 package. The CD contains a setup file that will automatically install the configuration files and protocol decoder onto a PC containing the 16900 operating system or onto a 16900 analyzer itself.

To install the software simply double click the .exe file on the CD containing the 16900 software. After accepting the license agreement the software should install within a couple of minutes.

### 169xx Licensing

Once the software has been successfully installed you must license the software. Please refer to the Software Entitlement Certificate for instructions on licensing the software. The software can only be installed on one machine. If you need to install the software on more than one machine you must contact the FuturePlus sales department to purchase additional licenses.

## Loading 169xx configuration files and General Purpose Probe feature

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute it. The protocol decoder automatically loads

when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

After loading the configuration file of choice, the user should see both the Probe Control application icon and the FS4200 configuration and decoder icon in the Probes column on the Overview page. Clicking on the Properties button of the FS4200 Config icon will display the General Purpose Probe Set as defined for this configuration.

## Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a \*.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may buy additional licenses, please contact FuturePlus Sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up the 169xx analyzer". Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

For data from a 16900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select "yes" when it asks if the system is ready to import 16700 data.

After clicking "Next" you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.

## Powering the IEEE1394 Analysis Probe

The active circuitry on the IEEE1394 Analysis Probe module gets its power from the logic analyzer PODs. No power is taken from the IEEE1394 cable.

**Please Note:** *If the State Analysis Probe is plugged into the IEEE1394 bus and the logic analyzer is not connected and powered up then the IEEE1394 interface on the State Analysis Probe will not be able to provide the appropriate IEEE1394 bus signal. This may cause problems with the bus configuration process.*

**The Logic analyzer must be connected and powered on before connecting to the IEEE1394 Serial Bus for the State Analysis Probe to work properly.**

## Connecting to the IEEE1394 Analysis Probe for 165xx or 167xx users

The following explains how to connect the logic analyzer to the IEEE1394 State Analysis Probe when using the 167xx or 165xx frames. 169xx users please refer to the section **Loading 169xx Configuration files and general purpose probe feature**, for probe connections:

1. Remove the probe tip assemblies from the logic analyzer cables.
2. Plug the logic analyzer cables into the IEEE1394 Analysis Probe cable headers as shown in the appropriate tables below.

### State Analysis Only

Logic Analyzer	IEEE1394 Analysis Probe	Comment
Master POD 1	POD 1	
POD 2	POD 2	
POD 3	POD 3	
POD 4	POD 4	

### State and Timing Analysis using a 6 POD Logic Analyzer card

Logic Analyzer	IEEE1394 Analysis Probe	Comment
Master POD 1	POD 1	
Master POD 2	POD 2	
Master POD 3	POD 3	
Master POD 4	POD 4	
Master POD 5	POD 5	
Master POD 6	POD 6	

**State and Timing  
Analysis using Two 4  
POD Logic Analyzer  
Cards**

Logic Analyzer	IEEE1394 Analysis Probe	Comment
Master POD 1	POD 1	
Master POD 2	POD 2	
Master POD 3	POD 3	
Master POD 4	POD 4	
Master POD 1	POD 5	2 <sup>nd</sup> 1655x card POD 1
Master POD 2	POD 6	2 <sup>nd</sup> 1655x card POD 2

**State and Timing  
Analysis using two  
Logic Analyzer Cards in  
Master & Expansion  
Configuration**

Logic Analyzer	IEEE1394 Analysis Probe	Comment
Master POD 1	POD 1	
Master POD 2	POD 2	
Expansion POD 1	POD 3	
Expansion POD 2	POD 4	
Master POD 3	POD 5	
Master POD 4	POD 6	

**Installing the  
IEEE1394 Analysis  
Probe**

The IEEE1394 Analysis Probe can be installed at any point in the IEEE1394 Serial bus. It can be placed either as a “leaf” node or between two other IEEE1394 nodes. The following steps explain how to install the State Analysis Probe into the bus.

1. Install the logic analyzer cables as described in the previous section.
2. Attach the IEEE1394 Analysis Probe to another IEEE1394 node using the cable provided. The cable may be connected to any one of the 3 IEEE1394 ports provided on the State Analysis Probe. If the State Analysis Probe is to be installed between two nodes reconnect the other node to one of the two remaining IEEE1394 ports on the State Analysis Probe using the cable providing the original connection between the two nodes.

**Please Note:** *If the State Analysis Probe is plugged into the serial bus and the logic analyzer is not powered up, the IEEE1394 interface on the State Analysis Probe will not be able to generate the appropriate IEEE1394 signals and may disrupt bus transactions.*

## 165xx and 167xx Logic Analyzer Configuration Files

Users of the 16600/16700 Logic Analysis Systems may use *the Setup Assistant* to load the correct configuration file for the logic analyzer configuration installed in the system.

Logic Analyzer	Number of PODS required/Number of Cards required	File name for State Analysis	Comment
166x	4/NA	CFW42_1	<b>State analysis only.</b> Connect Logic Analyzer PODS 1-4 to IEEE1394 Analysis Probe PODS 1-4.
166x	6/NA	CFW42_2	<b>State analysis and timing.</b> Connect Logic Analyzer PODS 1-6 to IEEE1394 Analysis Probe PODS 1-6.
16550A	4/1	CFW42_3	<b>State analysis only.</b> Connect Logic Analyzer PODS 1-4 to IEEE1394 Analysis Probe PODS 1-4.
16550A	6/1	CFW42_3	<b>State analysis and timing</b> PODS 1-4 used for State Analysis PODS 5-6 used for Timing Analysis. Connect Logic Analyzer PODS 1-4 to IEEE1394 Analysis Probe PODS 1-4 Connect Logic Analyzer PODS 5-6 to IEEE1394 Analysis Probe PODS 5-6.
1655x, 167x	4/1	CFW42_4	<b>State analysis only.</b>
16715/6/7 16750/1/2	4/1	CFW42_7	Connect Logic Analyzer PODS 1-4 to IEEE1394 Analysis Probe PODS 1-4.

Logic Analyzer	Number of PODS required/Number of Cards required	File name for State Analysis	Comment
1655x	6/2	CFW42_6	<b>State analysis and timing.</b> The two analyzer cards configured as a <b>single</b> logic analyzer (master + expansion).
16715/6/7 16750/1/2	6/2	CFW42_9	Connect IEEE1394 Analysis Probe POD 1 to the <b>master</b> logic analyzer's <b>POD1</b> . Connect IEEE1394 Analysis Probe POD 2 to the <b>master</b> logic analyzer's <b>POD2</b> . Connect IEEE1394 Analysis Probe POD 3 to the <b>expansion</b> logic analyzer's <b>POD1</b> . Connect IEEE1394 Analysis Probe POD 4 to the <b>expansion</b> logic analyzer's <b>POD2</b> . Connect IEEE1394 Analysis Probe POD 5 to the <b>master</b> logic analyzer's <b>POD3</b> . Connect IEEE1394 Analysis Probe POD 6 to the <b>master</b> logic analyzer's <b>POD4</b> .

## 169xx Configuration files

Logic Analyzer	File Name	Comments
1674x,16750-2, 1691x	CFW42_1	1 Card, state analysis
1674x,16750-2, 1691x	CFW42_2	1 Card, timing analysis
1674x,16750-2, 1691x	CFW42_3	2 Cards, 1 machine, state and timing analysis

### ***The IEEE1394 Inverse Assembler***

The Inverse Assembler is auto loaded into the logic analyzer when the configuration file is loaded.

- IFS4200 is the Inverse Assembler for the 166x, 167x and all supported logic analyzers installed into the 16500A/B/C mainframe.
- IFS4200E is the Inverse Assembler for all logic analyzers installed into the 16600 and 16700.

If the Inverse Assembler does not appear on the state listing screen select the base of the label DATA. From the menu that appears select INVASM.

## The Format Menu

The IEEE1394 Analysis Probe diskette sets up the format menu to include all of the signals that are presented to the logic analyzer. The labels STAT, DATA, ADDR and are required in order to run the Inverse Assembler. They should not be changed or deleted.

### *The STAT variable*

The IEEE1394 inverse assembler uses the STAT variable to decode IEEE1394 Serial bus transactions. *It should not be changed or deleted from the format menu.*

### *The ADDR and DATA variables*

The ADDR and DATA variables are defined in the format menu. The DATA variable is used to pass the IEEE1394 packet quadlets to the Inverse Assembler during state analysis. The ADDR variable is not used but must be defined for the Inverse Assembler to function correctly. *These variables should not be changed or deleted from the format Menu.*

### *Other Labels and Symbols*

A number of other labels and symbols are defined to assist in controlling the acquisition of data using triggers and filters. For example the label TCODE is defined with a number of associated symbols to represent the various types of primary packet. These may be used to trigger on a particular type of packet or to control acquisition of such packets. For a full list of available labels and related symbols look under the FORMAT section of the logic analyzer once the FS4200 software has been installed or see Appendix A

## Theory of Operation

The IEEE1394 Analysis Probe is an IEEE1394 node that attaches to logic analyzers. The Analysis Probe has two major parts:

1. The “PHY” interface to the IEEE1394 serial bus.
2. The interface to the logic analyzer.

### *The PHY Interface to the IEEE1394 Serial Bus.*

The “PHY” interface to the IEEE1394 Serial bus provides three IEEE1394 ports. The interface does not provide or use cable power but does pass cable power between the three ports. The PHY device converts the IEEE1394 serial information into a protocol known as the “PHY-LINK interface”. The IEEE1394 Analysis Probe interprets this protocol into a propriety format that is passed to the logic analyzer for further interpretation by the IEEE1394 Inverse Assembler.

### *Configuration Rom Implementation*

The IEEE1394 Analysis Probe implements the minimal Configuration ROM format. Therefore the “Company\_ID” entry is the only valid entry. Attempts to read other entries in the Configuration ROM address space will complete with invalid data. Note that the Analysis Probe’s response to a read of the “Company\_ID” is **not** captured in the state listing (see below for more details).

## ***Self ID and Reading the “Company\_ID”***

The IEEE1394 Analysis Probe's function is to observe the IEEE1394 serial bus and normally the Analysis Probe does not generate any IEEE1394 packets. However, there are two cases when the Analysis Probe will generate bus packet. The first is as part of the bus configuration process when the IEEE1394 Analysis Probe will generate a SELF ID packet as required by the IEEE1394 specification. **Note that this packet is not observed directly by the IEEE1394 Analysis Probe so is not reported in the state listing screen.** After sending the SELF ID packet the PHY device on the Analysis Probe will initiate the transfer of its “physical\_ID” register on its PHY-LINK interface. This transfer will be captured by the Analysis Probe and displayed as a “PHY Register Read” packet in the state listing. To determine the IEEE1394 Analysis Probe's “physical\_ID” after bus configuration observe the register read following a bus reset. The “physical\_ID” is given by the upper 6 bits of the packet data. The bottom 2 bits should be ignored.

The second case is when the IEEE1394 Analysis Probe will generate a packet on the bus in response to a read of the “Company\_ID” entry in the Configuration ROM. The Analysis Probe will initially respond to the read request with “ack\_pending” and then will arbitrate for the bus. Once the Analysis Probe is the bus owner it will generate a “Read Response for Data Quadlet” packet containing the “Company\_ID” data. **The Analysis Probe does not record the bus traffic it generates.** Therefore neither the “ack\_pending” nor the “Read Response for Data quadlet” will appear in the state listing display. This will cause the state display associated with the read request to the Analysis Probe to show only the read request packet and the “ack\_complete” from the requesting node (acknowledging the response from the Analysis Probe). The user should note that as a consequence, if there is no other bus traffic between the read request and the read response from the IEEE1394 Analysis Probe, then the display will show only the read request and an “ack\_complete” without showing any response packet.

## ***The interface to the Logic Analyzer***

The input to the logic analyzer consists of 3 parts.

1. The RC terminators (90 ohm/10pf)
2. The 40 pin headers
3. The 40 pin cables

The logic analyzer provides the power to the onboard logic. No power is obtained from the IEEE1394 Serial Bus.

## **LED Indicators**

The FS4200 has four LED indicators.

### ***+5V LED***

The +5V LED indicates that power is applied from the logic analyzer to the IEEE1394 Analysis Probe. For correct operation the +5V LED must be lit.

### ***+3.3V LED***

The +3.3V LED indicates that 3.3V is being generated by the FS4200. For correct operation the +3.3V LED must be lit.

### ***READY LED***

The READY LED indicates that IEEE1394 Analysis Probe is initialized and ready for IEEE1394 Serial bus analysis.

### ***IEEE1394 BUSY LED***

The IEEE1394 Busy LED is lit when there is activity on the IEEE1394 Serial bus. The brightness of the LED is related to the level of bus activity. If the bus activity is low then the LED may be dimly lit.

# State Analysis

This chapter explains how to configure the IEEE1394 Analysis Probe to perform state analysis on the IEEE1394 Serial Bus. The configuration software on the flexible diskette sets up the format specification menu of the logic analyzer for compatibility with the IEEE1394 Serial Bus. The next chapter explains how to configure the IEEE1394 Analysis Probe to perform timing analysis.

## Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the IEEE1394 Analysis Probe module.

1. After removing the probe tip assemblies (if present), plug the logic analyzer cables into the Analysis Probe cable headers. See page 12 of this manual for details.
2. Attach the IEEE1394 Analysis Probe to another IEEE1394 node using the cable provided. The cable may be connected to any one of the three IEEE1394 ports provided on the Analysis Probe. If the Analysis Probe is to be installed between two nodes reconnect the other node to one of the remaining two IEEE1394 ports on the Analysis Probe using the cable providing the original connection between the two nodes.

Please Note: If the Analysis Probe is plugged into the serial bus and the logic analyzer is not powered up, the IEEE1394 interface on the Analysis Probe will not be able to generate the appropriate IEEE1394 signals and may disrupt bus transactions.

Load the logic analyzer configuration file by loading the appropriate file from the appropriate FS4200 software diskette. See page 14 of this manual for details.

## Acquiring Data

Touch or click RUN on the logic analyzer and as soon as there is activity on the bus the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch or click STOP.

The logic analyzer will flash "Slow or Missing Clock" when data is not being transmitted across the bus.

## The State Listing Display

Captured data is as shown in the following figure. The figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual packet formats, commands and status conditions specified in the IEEE1394 specification. Symbols have also been defined to help aid in analysis. Packet field data is displayed in binary, decimal or hexadecimal as appropriate for the packet field. Binary data is terminated with the letter B (e.g. 0110B) and hexadecimal data with the letter H (e.g. 12AE3921H).

Packet data is presented according to the IEEE1394 specification. In particular data is displayed with the most significant bit (that is the first bit received from the IEEE1394 Serial bus) in the left most position.

State Number	Time	Relative	FUTUREPLUS SYSTEMS c 1998
Decimal	Relative		IEEE 1394 BUS TRANSACTIONS VERSION 0.3
			WR_REQ_DATA_QUADLET @5400: TLABEL= 00H; RETRY CODE= retry_1
1	40,000 ns		DST_ID:Bus= 3FFH;Node= 00H
2	40,000 ns		SRC_ID:Bus= 3FFH;Node= 02H
3	104,000 ns		DST_OFFSET= 1000000FFCOH
4	120,000 ns		DATA= 12345678H
5	10,840 us		HDR CRC: 016FBACCH
			SUBACTION Gap
6	10,504 us		ARB Reset Gap
			ARB Reset Gap
7	3,128 us		RD_RESPONSE_QUADLET @5400: TLABEL= 01H; RETRY CODE= retry_A
8	40,000 ns		DST_ID:Bus= 3FFH;Node= 00H
9	40,000 ns		SRC_ID:Bus= 3FFH;Node= 02H
10	104,000 ns		RESP CODE: Response Complete
11	120,000 ns		Reserved Quadlet: 00000000H
			DATA= 46AC55E2H
			HDR CRC: E47BC755H

## Using Symbols to Trigger in State Mode.

The labels and symbols provided may be used to trigger on the various fields of the packet. There are two types of labels. One type of label is used to define fields from IEEE1394 packets. The other type is used to qualify fields within the data passed to the analyzer. The labels used as qualifiers are :

- SID\_Q to qualify the Source ID field (used with the D/S ID Label).
- DID\_Q to qualify the Destination ID field (used with the D/S ID Label).
- TLAB\_Q to qualify the Transaction Label field (used with the TLABEL Label)

The following sections give some examples of how to use these labels.

### ***Triggering on a Packet Type***

The TCODE label may be used to define a trigger term specifying the required packet type. Symbols are defined for all packet types. The TCODE label is valid throughout a packet so may be used to qualify triggering on other fields within a particular packet type.

### ***Triggering on a Destination Address***

The DID\_Q label defines a qualifier for the D/S ID label. Together they may be used to define a trigger condition specifying a particular destination node. Define a trigger term specifying DID\_Q and D/S ID. In the value field for the D/S ID label define the required destination address in the positions marked X.

### ***Triggering on a Source Address***

The SID\_Q label defines a qualifier for the D/S ID label. Together they may be used to define a trigger condition specifying a particular source node. Define a trigger term specifying SID\_Q and D/S ID. In the value field for the D/S ID label define the required source address in the positions marked X.

### ***Triggering on a Combination of Packet Fields.***

The pre-defined symbols may be used to trigger on a combination of Packet Fields (for example a Write Request for Data Quadlet at speed S400) by defining a trigger condition for each field and then using the trigger definition menu to AND or OR the conditions together.

### **Qualifying Storage of Packets**

The labels and symbols provided may also be used to qualify the storage of data acquired from the IEEE1394 Serial bus. The End Of Packet (EOP) label may be used in conjunction with other labels to trigger on and store particular packets of interest.

For example to capture only traffic to a particular destination I.D. set the trigger condition to the required destination I.D. and store until EOP is set then loop back and re-trigger.

### **Filtering Data Payload**

To conserve acquisition memory it is possible to filter data payload information prior to capture in memory. The IEEE1394 Analysis Probe generates a separate clock for sending data payload quadlets to the analysis system. This clock is connected to the Logic Analyzer's "K" Clock and the configuration defines that both the "J" and "K" clocks are to be used to clock data to the analyzer. By changing the configuration so that the analyzer only uses the "J" clock data payload quadlets will not be clocked into memory. This can be particularly useful if bus traffic involves a number of packets with large data payloads.

### **Error Messages**

*"ERR: PHY packet check failed."*

The IEEE1394 Inverse Assembler reports the following error messages.

This error is displayed if a PHY packet is received in which the second quadlet is not the logical inverse of the first.

*"ERR: PHY packet type not recognized"*

This error is displayed if a PHY packet is received with a type code of 11<sub>2</sub>. This type code is not defined by the IEEE1394-95 or P1395A specifications.

<i>"ERR: Invalid Trans Label"</i>	This error is displayed if a Cycle Start packet is received with a Transaction Label field set to a value other than 000000 <sub>2</sub>
<i>"ERR: Invalid Retry Code"</i>	This error is displayed if a Cycle Start packet is received with a Retry Code field set to a value other than 00 <sub>2</sub>
<i>"ERR: Invalid Trans Label &amp; Retry Code"</i>	This error is displayed if a Cycle Start packet is received with a Transaction Label field set to a value other than 000000 <sub>2</sub> and a Retry Code field set to a value other than 00 <sub>2</sub>
<i>"ERR: Invalid Priority"</i>	This error is displayed if a Cycle Start packet is received with a Priority field set to a value other than 1111 <sub>2</sub> .
<i>"ERR: Invalid Trans Label &amp; Priority"</i>	This error is displayed if a Cycle Start packet is received with a Transaction Label field set to a value other than 000000 <sub>2</sub> and a Priority field set to a value other than 1111 <sub>2</sub>
<i>"ERR: Invalid Retry Code &amp; Priority"</i>	This error is displayed if a Cycle Start packet is received with a Retry Code field set to a value other than 00 <sub>2</sub> and a Priority field set to a value other than 1111 <sub>2</sub>
<i>"ERR: Invlid Trans Lbl, RT Code &amp; Priority"</i>	This error is displayed if a Cycle Start packet is received with a Transaction Label field set to a value other than 000000 <sub>2</sub> , a Retry Code field set to a value other than 00 <sub>2</sub> and a Priority field set to a value other than 1111 <sub>2</sub>
<i>"ERR: Invalid Dest ID for CYCLE START:"</i>	This error is displayed if a Cycle Start packet is received with a Destination ID field set to a value other than FFFF <sub>16</sub> .
<i>"ERR: Invalid destination offset" CYCLE START</i>	This error is displayed if a Cycle Start packet is received with a Destination Offset field set to a value other than the standard address of the CYCLE_TIME register.
<i>"ERR: INVALID Data Length"</i>	This error is displayed if a Lock Request packet or a Lock Response packet is received with a data length field set to a reserved value.
<i>"HDR CRC ERR: RCVD CRC= "</i>	This error is displayed if the IEEE1394 Analysis probe detects a CRC error when receiving the header of a primary packet.
<i>"ERR: Reserved TCODE field in a Primary Packet."</i>	This error is displayed if a Primary packet is received with the reserved Transaction Code (TCODE).
<i>"Invalid Extended TCODE= "</i>	This error is displayed if a Primary packet is received with the extended_tcode field set to a value other than 0000 <sub>16</sub> and the packet is not either a Lock Request or a Lock Response.

*"ACK Parity Error"*

This error is displayed if an Acknowledge packet is received and the Ack\_Parity field is not the ones complement of the Ack\_Code field.

*"ERR: Input data Error - Aborting"*

This error is displayed if the IEEE1394 Inverse Assembler detects that the logic analyzer has failed to initialize the inverse assembly environment correctly.

*"ERR: Expected End of Packet not found; "*

This error is displayed if an Asynchronous Primary packet with no data payload is received and the "end of packet marker" generated by the FS4200 hardware is not detected when expected.

*"ERR: EOP/CRC PROBLEM"*

This error is displayed if an Asynchronous Primary packet with no data payload is received that contains more quadlets than expected.

*"DATA CRC ERR: RCVD CRC= "*

This error is displayed if the IEEE1394 Analysis probe detects a CRC error when receiving the data payload of a primary packet.

*"ERR: Packet not an integral number of quadlets"*

This error is displayed if a packet is received that is not an integral number of quadlets (4 bytes) and the packet is not either an Acknowledge packet or a PHY status packet.

## **Post Processing Filters**

Post Processing Filters are only available with the 16600 or 16700 mainframe logic analyzers.

Filters can be invoked by selecting FILTER from the INVASM menu in the state listing display. The following selections can be suppressed or shown.

- Primary Packets.
- Acknowledge Packets.
- PHY Packets.
- PHY Status Packets.
- Data Payload.
- Isochronous Packets.
- Cycle Start Packets.
- Errors

The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the show/suppress button to the left of the list. Note that unlike the filtering of the data payload described in the section Filtering Data Payload (21) post processing filters only remove information from the display and not from the logic analyzer's acquisition memory.

The post processing filters also allow the various transaction types given in the selection list to be identified with colors in the display listing. A default color scheme has been selected for each transaction type. This can be changed by selecting the button to the right of the list.

# Timing Analysis and Viewing the IEEE1394 Serial Bus.

## Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the IEEE1394 Analysis Probe module.

1. After removing the probe tip assemblies (if present), plug the logic analyzer cables into the Analysis Probe cable headers. See page 12 of this manual for details.
2. Attach the IEEE1394 Analysis Probe to another IEEE1394 node using the cable provided. The cable may be connected to any one of the three IEEE1394 ports provided on the Analysis Probe. If the Analysis Probe is to be installed between two nodes reconnect the other node to one of the remaining two IEEE1394 ports on the Analysis Probe using the cable providing the original connection between the two nodes.

Please Note: If the Analysis Probe is plugged into the serial bus and the logic analyzer is not powered up, the IEEE1394 interface on the Analysis Probe will not be able to generate the appropriate IEEE1394 signals and may disrupt bus transactions.

Load the logic analyzer configuration file by loading the appropriate file from the appropriate FS4200 software diskette. See page 14 of this manual for details.

## Timing

It is expected that the state analysis mode of the IEEE1394 Analysis Probe will provide the necessary visibility to observe IEEE1394 Serial bus activity. However the IEEE1394 Analysis Probe does provide the means to observe timing related to the IEEE1394 Serial bus. POD 5 carries the "PHY-LINK Interface" signals from the IEEE1394 PHY interface. This interface adheres to the protocol in Annex J of the IEEE1394-95 specification. The table below shows how these signals are mapped to the logic analyzer pod.

PHY-LINK SIGNAL	LOGIC ANALYZER CHANNEL NUMBER	HEADER NUMBER AND PIN
SCLK	15	POD5-7
LINK_ON	11	POD5-15
CTL[1]	9	POD5-19
CTL[0]	8	POD5-21
D[7]	7	POD5-23
D[6]	6	POD5-25
D[5]	5	POD5-27
D[4]	4	POD5-29
D[3]	3	POD5-31
D[2]	2	POD5-33
D[1]	1	POD5-35
D[0]	0	POD5-37

The user should be aware that the default configuration of the logic analyzer displays buses with the highest labeled signal as the most significant bit. Therefore if signals such as CTL[0:1] and DATA[0:7:] are displayed as a bus the highest labeled signal (DATA[7] or CTL[1]) will be seen as the most significant bit. This will cause the values on the display to look different from those in the IEEE1394 specification.

The IEEE1394 Analysis Probe also provides four SMA connectors (50 Ohm) that are connected directly to the signal pairs TPA/TPA\* and TPB/TPB\* on one of the three ports. These connectors may be used to connect an oscilloscope to the Analysis Probe for direct observation of the serial bus signals.

**NOTE:** The IEEE1394 serial bus uses low voltage signals in an impedance controlled environment. The connection of an oscilloscope to these signals is a load over and above the load defined in the IEEE1394 specification. Care must be taken to avoid disrupting the serial bus signaling.

# General Information

This chapter provides additional reference information including the characteristics and signal connections for the IEEE1394 Analysis Probe module.

## **Characteristics**

The following operating characteristics are not specifications, but are typical operating characteristics for the IEEE1394 Analysis Probe module.

### ***Analysis Probe Interface Compatibility***

The IEEE1394 Analysis Probe is compatible with the IEEE1394-95 and PIEEE1394A 6 pin interface connector. Cable power is not used on the Analysis Probe but is routed between the three IEEE1394 ports. Power for the IEEE1394 Analysis Probe is supplied by the logic analyzer. The IEEE1394 cable ground is connected to the State Analysis 0V plane and to the ground of the logic analyzer.

### ***Standards Supported***

IEEE1394-95 (and compatible with PIEEE1394A)

### ***Power Requirements***

The IEEE1394 Analysis Probe contains several active components that process the IEEE1394 signals before they are acquired by the logic analyzer. The Analysis Probe takes no power from the IEEE1394 Serial bus but is powered by the logic analyzer. At least 4 logic analyzer pods must be connected to the IEEE1394 Analysis Probe to ensure sufficient current to support correct operation.

### ***Logic Analyzer Required***

166x, 167x, 169xx, 16550A, 16554A, 16555A, 16556A, 16557A, 16600, 16601, 16602, 16603, 16711-7, 1674x, 16750-2

### ***Number of Probes Used***

State Only - 4 cable headers.

State and PHY-LINK interface – 6 cable headers.

### ***Maximum Speed***

The IEEE1394 Analysis Probe supports transfers up to S400 (393.216 Mbits/sec)

### ***Operations***

All IEEE1394-95 operations are supported. Operations compatible with PIEEE1394A are also supported.

### ***Environmental Temperature***

Operating: 0 to 55 degrees C (+32 to +131 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

### ***Altitude***

Operating: 4,600m (15,000 ft)

Non operating: 15,300m (50,000 ft)

### ***Humidity***

Up to 90% non condensing. Avoid sudden, extreme, temperature changes, which would cause condensation on the Analysis Probe module.

***Testing and  
Troubleshooting***

There are no automatic performance tests or adjustments for the IEEE1394 Analysis Probe module. If a failure is suspected in the IEEE1394 Analysis Probe module contact the factory or your FuturePlus Systems authorized distributor.

***Servicing***

The repair strategy for the IEEE1394 Analysis Probe is module replacement. However, if parts of the IEEE1394 Analysis Probe module are damaged or lost contact the factory for replacement parts.

# Appendix A: Format Definitions

The format menu contains a number of label and symbol definitions that are useful for setting up triggers and data acquisition filters. These definitions are shown in the following tables.

## State Formats

Label	Pod 4	Pod 3	Pod 2	Pod 1
PRIMARY				15
TCODE				15:11
SPEED				10:8
EOP				7
CRC				6
NOTQD				4
ERROR				3
HDRCNT				2:0
REGVLD			2:0	
ACKMIS			3	
SID_Q				15, 2:0
DID_Q				15, 2:0
TLAB_Q				15, 2:0
RT		9:8		15, 2:0
RCODE		15:12		15, 2:0
ETCODE		15:0		15:11, 2:0
D/S ID	15:0			
TLABEL		15:10		
PHYPKT	15:14			15:11,2:0
EXPHYPKT	15:14,7:2			15:11,2:0
EVENTS				15:11
ACKS	15:12			15:11
DATA	15:0	15:0		
STAT			15:0	15:0
ADDR	15:0	15:0		

<b>TCODE Symbol</b>	<b>Definition</b>
WR REQ DATA QUAD	10000
WR REQ DATA BLK	10001
WR RESPONSE	10010
RD REQ DATA QUAD	10100
RD REQ DATA BLK	10101
RD RSP DATA QUAD	10110
RD RSP DATA BLK	10111
CYCLE START	11000
LOCK REQUEST	11001
ISOCHRONOUS	11010
STREAM DATA BLK	11010
LOCK RESPONSE	11011

<b>SPEED Symbol</b>	<b>Definition</b>
S100	001
S200	010
S400	011

<b>RT Symbol (Retry Code)</b>	<b>Definition</b>
RETRY_1	001001
RETRY_X	011001
RETRY_A	101001
RETRY_B	111001

<b>RCODE Symbol</b>	<b>Definition</b>
resp_complete	00001010
resp_conflict_err	01001010
resp_data_err	01011010
resp_type_err	01101010
resp_address_err	01111010

<b>ETCODE Symbol (extended TCODE)</b>	<b>Definition</b>
mask_swap	0000000000000001110X1100
compare_swap	0000000000000010110X1100
fetch_add	0000000000000011110X1100
little_add	0000000000000100110X1100
bounded_add	0000000000000101110X1100
wrap_add	0000000000000110110X1100
vendor_dependent	0000000000000111110X1100

<b>ACKS Symbol (Acknowledge Codes)</b>	<b>Definition</b>
Ack_complete	0001
Ack_pending	0010
Ack_busy_x	0100
Ack_busy_a	0101
Ack_busy_b	0110
Ack_data_error	1101
Ack_type_error	1110

<b>PHYPKT Symbol (PHY Packets)</b>	<b>Definition</b>
Phy_config	00
Link_on	01
Phy_id	10

<b>EXPHYPKT</b>	<b>Definition</b>
Ping	000000001000001
Remote Access	00000X0101000001
Remote Reply	00000X1101000001
Remote CMD	0000100001000001
Remote Confirm	0000101001000001
Resume	0000111101000001

<b>EVENTS Symbol</b>	<b>Definition</b>
Arb_Reset	0001
Sub_Action_Gap	0010
Bus_Reset	0011
State_Time_out	0100
Null_event_pkt	0101

### Timing Format

<b>LABEL</b>	<b>POD 5</b>
SCLK	15
LNK_ON	11
CTL	9:8
DATA	7:0