

FuturePlus Systems Corporation



Premier Solution Partner

FS3100 – VME64/VXI Bus Analysis Probe

User's Guide

for use with Agilent Technologies Logic Analyzers

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HOW TO CONTACT US	5
PRODUCT WARRANTY	6
LIMITATION OF WARRANTY	6
EXCLUSIVE REMEDIES	6
ASSISTANCE	6
INTRODUCTION	7
LOGIC ANALYZERS SUPPORTED	7
HOW TO USE THIS MANUAL	7
CHAPTER 1 - ANALYZING THE VME/VXI BUS	8
Introduction	8
Duplicating the Master Disk	8
Equipment Supplied	8
Minimum Equipment Required	8
Caution	8
Daisy-Chaining	9
Bus Grant and IACKIN/OUT Lines	9
Connecting the Jumpers	10
LED Indicators	12
CHAPTER 2 STATE ANALYSIS	13
Introduction	13
Installation Quick Reference	13
Connecting to the FS3100	14
Using the FS3100 with an Agilent 1690x Analyzer	16
1680/90/900 Licensing	16

Loading 1680/90/900 configuration files	16
Connecting the 1680/90/9xx Agilent logic analyzer to the FS3100	16
Timing Analysis with the 1680/90/9xx	16
Offline Analysis	17
Installing the FS3100	19
Setting Up the Analyzer from the Disk	20
State Format Specification	20
Acquiring Data	21
Listing Menu	22
Bus Grant Interpretation	24
Address Interpretation	24
VXI Bus Translation	25
Error Messages	26
CHAPTER 3 TIMING ANALYSIS	27
Introduction	27
Installation Quick Reference	27
Connecting to the FS3100	27
Installing the FS3100	29
Setting Up the Analyzer from the Disk	29
Timing Format Specification	29
Acquiring Data	30
Symbols	30
Waveforms Menu	31
CHAPTER 4 GENERAL INFORMATION	32
Introduction	32
Characteristics	32
Analysis Probe Interface Compatibility:	32
Standard Supported:	32
Accessories Required:	32
Power Requirements:	32

Number of Probes Used:	32
Signal Line Loading	32
Sampling Time	33
Timing Measurement Skew:	33
Analysis Probe Interface Description	33
State/Timing Switch	33
Pod 6 (for 16/32 bit analysis only)	34
Master Clock	34
Slave Clock	34
Signal Connections	34
Servicing	37
Troubleshooting	37
Target Board Will Not Boot	37
“Slow or Missing Clock”	38
Slow Clock	38
“No Configuration File Loaded”	38
“Selected File is Incompatible”	38
“. . . Inverse Assembler Not Found”	38
Incorrect Inverse Assembly	39
No Activity on Activity Indicators	39
“State Clock Violates Overdrive Specification”	39
Intermittent Data Errors	40

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Introduction

The FS3100 VME/VXI Bus Analysis Probe Interface provides a complete interface between any VME/VXI Bus target system using “B” or “C” size cards and the logic analyzers listed below. The Analysis Probe interface connects the signals from the VME/VXI Bus target system to the logic analyzer inputs. For “B” sized systems, the Analysis Probe interface board may also be used as an extender board.

The configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with your VME/VXI bus system. When the state configuration file is loaded, an inverse assembler is also loaded which decodes VME/VXI transactions into mnemonics.

Logic Analyzers Supported

The following logic analyzers are supported by the FS3100 Analysis Probe Interface:

- 1650A, 1650B, 16510A, 16510B, and 1652B
- 1660A/61A
- 16511B
- 16550A, 16710
- 1655x, 16717/8/9, 16750/1/2
- 167x
- 1690x, 16910/11

How to Use This Manual

This manual is organized into four chapters and one appendix:

- **Chapter 1** introduces you to the FS3100 VME/VXI Bus Analysis Probe Interface and lists the minimum equipment required and accessories supplied for VME/VXI bus analysis. This chapter also contains information that is common to both state and timing analysis of the VME/VXI bus.
- **Chapter 2** explains how to configure the FS3100 VME/VXI Bus Analysis Probe Interface to perform state analysis on your target system.
- **Chapter 3** explains how to configure the FS3100 to perform timing analysis on your target system.
- **Chapter 4** provides some general information including the operating characteristics for the FS3100 Analysis Probe Interface.
- **Appendix A** contains information on troubleshooting problems or difficulties which may occur with the Analysis Probe interface.

Chapter 1 - Analyzing the VME/VXI Bus

Introduction

This chapter introduces you to the FS3100 VME/VXI Bus Analysis Probe Interface and lists the minimum equipment required and accessories supplied for VME/VXI bus analysis. This chapter also contains information that is common to both state and timing analysis of the VME/VXI bus.

Duplicating the Master Disk

Before you use the FS3100 software, make a duplicate copy of the FS3100 master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The FS3100 Bus Analysis Probe Interface consists of the following equipment:

- The Analysis Probe interface hardware, which includes the interface circuit board (FuturePlus Systems part number FS3100). Six jumpers which come installed on the circuit board.
- The 16700 protocol decode software on a 3.5-inch disk.
- The 1690x Windows-based FS1135 protocol decode software on CD.
- A SW Entitlement certificate for the FS1135 protocol decode software.
- This operating manual and Quicksheet on CD. A hardcopy of the Quicksheet.

Minimum Equipment Required

The minimum equipment required for analysis of a VME/VXI bus target system consists of the following equipment:

VME32/VXI systems:

- A 1650A, 1650B, 1652B, 1660A/61A, 16510A, 16510B, 16511B, 16550A Logic Analyzer or 1655x, 167x, or 1690x.
- The VME/VXI Bus Analysis Probe Interface Configuration files and Protocol Decoder.

VME64/VXI systems:

- 1690x, 1660, 167x, 16550 and 1655x Logic analyzers
- The VME/VXI Bus Analysis Probe Interface Configuration files and Protocol Decoder.

Caution

To prevent equipment damage, remove power from both the logic analyzer and the target system whenever the Analysis Probe interface is being connected or disconnected.

Use of the Asterisk

To help define usage, the VME/VXI specification (IEEE STD P1014) assigns an asterisk (*) suffix to signal mnemonics for the following conditions:

- An asterisk (*) follows the signal name of signals which are level-significant to denote that the signal is true or valid when the signal is low.
- An asterisk (*) follows the signal name of signals which are edge-significant to denote that the actions initiated by that signal occur on a high to low transition.
- In the symbol tables, the labels for signals or groups of signals which are asserted low are designated with a prefix “/”, such as “/BGIN”.

Daisy-Chaining

The daisy-chains are used to propagate signal levels from board to board, starting with the first slot and ending with the last slot. Each board in a VME/VXI bus backplane slot can control whether the Bus Grant and IACKIN/OUT signals are passed to the next highest slot. The FS3100 Analysis Probe Interface board allows you to properly jumper the four Bus Grant daisy-chains and the Interrupt Acknowledge daisy-chain on the VME/VXI bus.

Bus Grant and IACKIN/OUT Lines

The Bus Request lines are used to request the use of the Data Transfer Bus (DTB). The Bus Grant lines allow the ARBITER to award use of the bus to one REQUESTER at a time. The ARBITER does this by driving a Bus Grant daisy-chain line low. This low level propagates down the daisy-chain, typically passing through several boards in the process. If a board never uses a particular request/grant level, the signal is passed through that board. If the board uses a request/grant level low, the corresponding signal BGxIN* is stopped on the board. If this board's on-board REQUESTER is currently requesting the DTB on that level, the board does not pass the low level on to its BGxOUT*. Otherwise, the board passes the low level on to the next board.

If the Bus Grant information is required, you must place the Analysis Probe interface board in a lower number slot than any VME/VXI board in which BGxIN* is occurring. If the Analysis Probe interface board is in a higher number slot than a VME/VXI board which is requesting the bus, the daisy chain will not pass the necessary information for the Analysis Probe interface to properly decode the bus arbitration. When this happens, a 3 (hexadecimal) is displayed on the state display listing, instead of the proper bus grant number.

Each of the seven Interrupt Request lines can be shared by two or more INTERRUPTER modules. The Interrupt Acknowledge daisy chain assures that only one INTERRUPTER responds to the Interrupt Acknowledge cycle. This daisy-chain line passes through each board on the VME/VXI bus. Each INTERRUPTER that is driving an interrupt line low waits for a falling edge to arrive at its IACKIN* daisy-chain input. Only upon receiving this falling edge does an INTERRUPTER respond to an Interrupt Acknowledge cycle. The INTERRUPTER does not pass the falling edge on down the daisy chain. This prevents other INTERRUPTERS from responding to the Interrupt Acknowledge cycle.

Jumper J2 provides the daisy chain for the IACKIN/OUT signal. Jumpers J3 through J6 provide the daisy chain for the Bus Grant signals. If either of the following conditions are true, jumpers must be installed across pins 1 and 2 on J2 through J6 at an empty mainframe slot to pass the Bus Grant and IACKIN/OUT signals:

- If a VME/VXI bus backplane slot is not occupied by a board, and there are boards farther down the daisy chain.

If no VME/VXI board is installed in the FS3100 Analysis Probe Interface board that resides in that slot, and there are boards farther down the daisy chain.

Note

If the Analysis Probe interface is used as an extender card, with another VME/VXI Bus card attached to the front of it, the jumpers must be placed across pins 2 and 3, or else removed, to avoid shorting the daisy chain. The VME/VXI Bus card will provide the necessary circuitry for the daisy chain.

S_DX Signal

The signal S_DX will go high on the second and subsequent DTACK's after the first one with out a reset of AS. This signal is present on the product so that the Inverse Assembler can detect RMW and BLK transfers.

Connecting the Jumpers

Figure 1-1 shows the location of the jumpers and the appropriate pin locations. There are six jumpers, J1 - J6. Five of the jumpers (J2 - J6) are for configuring the Analysis Probe interface according to how it is used in the VME/VXI bus daisy chain. The sixth jumper (J1) selects the signal BERR or IRQ1 for timing measurements.

Jumpers J2 - J6 have the same function as the Bus Grant and IACKIN/OUT jumpers on any VME or VXI card. These jumpers make or break the daisy chain for the Bus Grant lines and the IACKIN/OUT line. J2 is for IACKIN/OUT, and J3 through J6 are BG3 through BG0. The five configuration jumpers must be connected across the pins as shown in the table 1-1. Table 1-2 shows the jumpers for BERR/IRQ1.

Table 1-1. Jumper Connections (J2 - J6)

Jumpers	Condition
Across pins 1 and 2	If there is not a VME/VXI board installed in the FS3100 Analysis Probe Interface board that is installed in a VME/VXI backplane slot, AND there are boards farther down the daisy-chain.
Across pins 2 and 3	If the FS3100 Analysis Probe Interface board is used as an extender, and there is a VME/VXI board installed in the front of the board.
Across pins 2 and 3	If there are not boards installed farther down the daisy-chain from the FS3100 Analysis Probe Interface board.

Note

The FS3100 Analysis Probe Interface board is shipped from the factory with jumpers connected across pins 2 and 3 of J2 through J6.

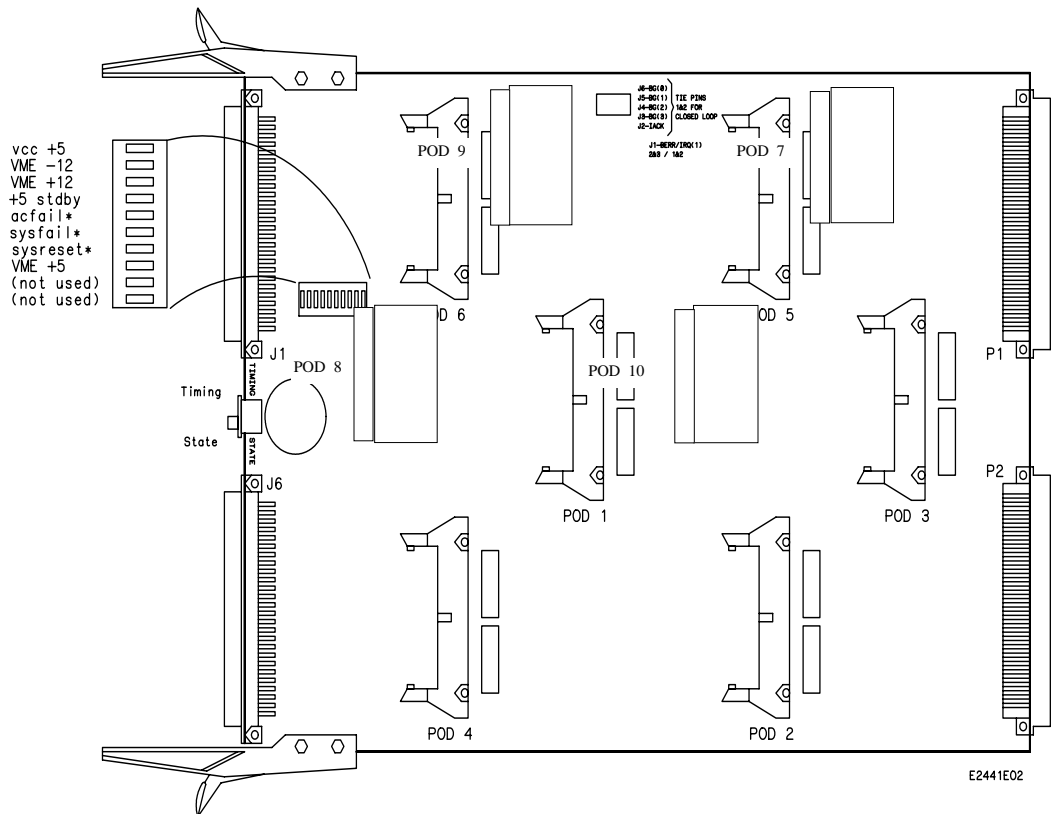
LED Indicators

An LED light bar containing 10 LED's (see figure 1-2) is used to inform you of the status of the following signals:

- VME_+5.
- VME_-12.
- VME_+12.
- VME_+5STDBY.
- ACFAIL.
- SYSFAIL.
- SYSRESET.
- VCC (+5 V).

The power indicator LEDs will be illuminated if power is applied to the target system. In order for the Analysis Probe interface to be operating, the logic analyzer must be supplying power. If ACFAIL, SYSFAIL, or SYSRESET become true (active low), the corresponding LED will be turned on. The first two LED's are not used.

Figure 1-2 LED Display



Chapter 2 State Analysis

Introduction

This chapter explains how to configure the FS3100 VME/VXI Bus Analysis Probe Interface to perform state analysis on a VME/VXI bus system using “B” or “C” size cards. The state configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the VME/VXI bus target system. The two inverse assemblers interpret both VME and VXI bus transactions for obtaining displays of VME/VXI bus data. The IAVXID64 inverse assembler decodes memory transactions in the A16 address range C000H to FFFFH in terms of VXI version 1.3 protocols and definition. The IAVMED64 inverse assembler decodes these addresses as pure VME references.

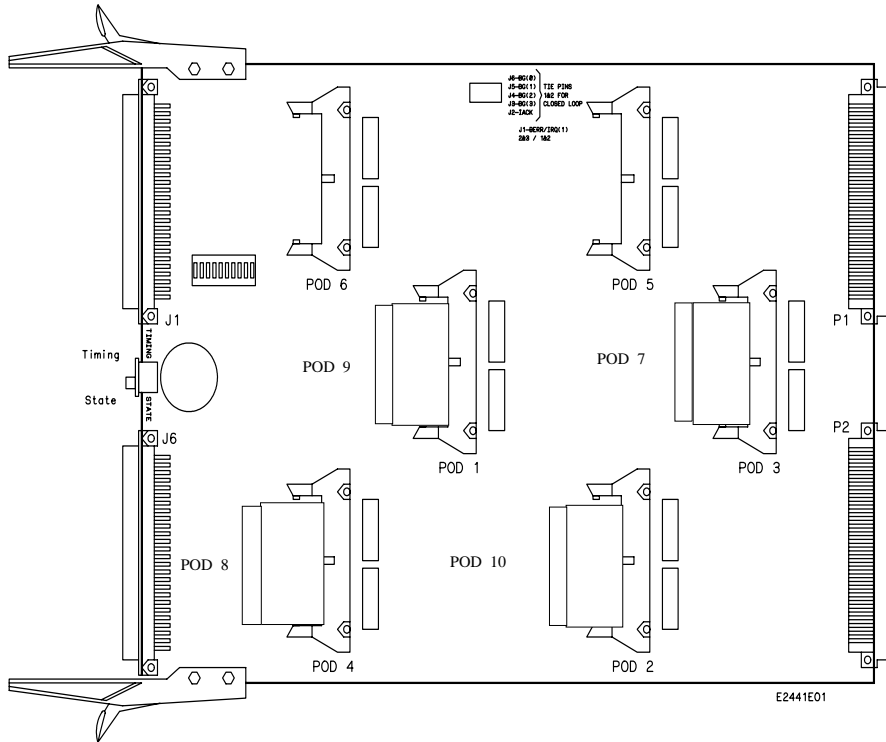
Chapter 3 explains how to configure the FS3100 VME/VXI Bus Analysis Probe Interface to perform timing analysis on a VME/VXI bus system using “B” or “C” size cards.

Installation Quick Reference

The following procedure describes the major steps required to perform state measurements with the FS3100 Bus Analysis Probe Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

1. Set the State/Timing switch to the down (State) position for state analysis (see figure 2-1).
2. Set jumpers across pins 1 and 2 of jumpers J2 through J6 if the daisy chain on signals BG3IN* through BG0IN* and IACK* need to continue to the next slot (see page 6). Otherwise, set jumpers across pins 2 and 3. Note that if the Analysis Probe interface board is used as an extender, the jumpers must be set across pins 2 and 3.
3. Plug the logic analyzer cables into the Analysis Probe interface board (see table 2-1 thru table 2-3).
4. If you are installing the Analysis Probe interface board into a “C” size target system, remove the two board supports on the Analysis Probe interface board (see figure 2-3).
5. Install the Analysis Probe interface board in the target system and, if necessary, plug the VME/VXI board into the Analysis Probe interface board (see page 13).
6. Load the logic analyzer configuration and Protocol Decoder by loading the appropriate file from the diskette or CD (1690x only) (see page 14).
7. For use with the 1670x frame only, load the appropriate Protocol Decoder:
 - IAVMED64 for VME64 or VXI inverse assembly without decoding VXI registers.
 - IAVXID64 for VME64 or VXI inverse assembly including decoding VXI registers.

Figure 2-1



Connecting to the FS3100

Connect the logic analyzer cable pods to the FS3100 Analysis Probe Interface headers as shown in the following tables.

Table 2-1. Connections and Configuration Files (State Analysis) for VME32/VXI systems

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
1650A, 1650B, 16510A, 1652B and 16510B	F510_0S		P5	P4	P3	P2	P1
16550A, 16710	F550_02	P6**	P5	P4	P3	P2	P1
16554/5/6/7 Master Card 167x, 167XX Pods 1-4	F555_02			P4	P3	P2	P1
16554/5/6/7 Expander Card Pods 1-2 167x, 167XX Pods 5-6	F555_02	P6**	P5				
1660A/61A	F550_02	P6**	P5	P4	P3	P2	P1

Table 2-2. Connections and Configuration Files (State Analysis) for VME/VXI A32/D64 systems

Logic Analyzer	File	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
1650A, 1650B, 16510A, 1652B and 16510B, 16511B	not supported	--	--	--	--	--	--	--	--
1660	F660_00	P8	P7	P6**	P5	P4	P3	P2	P1
16550A, 16710 Master Card	F550_00			P6**	P5	P4	P3	P2	P1
16550A, 16710 Expander Card		P2	P1						
16554/5/6/7 Master Card 167X, 167XX Pods 1-4	F555_00					P4	P3	P2	P1
16554/5/6/7 Expander Card 167X, 167XX PODS 5-8		P4	P3	P2**	P1				
1661A	not supported								

Table 2-3. Connections and Configuration Files (State Analysis) for VME/VXI A64/D64 systems

Logic Analyzer	File	Pod 10	Pod 9	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
1650A, 1650B, 16510A, 1652B and 16510B, 16511B	not supported	--	--	--	--	--	--	--	--	--	--
1660	not supported	--	--	--	--	--	--	--	--	--	--
16550A, 16710 Master Card	F550_01					P6**	P5	P4	P3	P2	P1
16550A, 16710 Expander Card		P4	P3	P2	P1						
16554/5/6/7, 167XX Master Card	F555_01							P4	P3	P2	P1
16554/5/6/7, 167XX Expander Card 1				P4	P3	P2**	P1				
16554/5/6/7, 167XX Expander Card 2		P2	P1								
1661A, 167x	not supported										

** not required for inverse assembly. It is only used for timing analysis.

POD 9 and 10 are only used for A64 systems

Using the FS3100 with an Agilent 1690x Analyzer

The 1680/90/900 Analyzer is a PC based application that requires a PC running Windows OS with the Agilent logic analyzer software installed or a 16900 frame.

Before installing the protocol decoder for the VME/VXI protocol on a PC you **must** install the Agilent logic analyzer software. Once the Agilent logic analyzer software is installed, you can install the FS1135 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the .exe file on the CD-ROM disk and then double click the .exe file name from within the File Explorer navigation panel.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe Adapter is used.

1680/90/900 Licensing

The FS1135 Protocol Decode software is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the 16900 SW Entitlement certificate provided with this product.

Loading 1680/90/900 configuration files

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list. All of this configuration files have the VME Protocol Decoder load as the default. If VXI protocol is being used, then from the 1690x Overview screen delete the VME Decoder and replace it with the VXI Protocol Decoder found under the Tools drop-down menu.

Refer to the table for a list 1690x configuration files.

Target systems	State and Timing	File	Default Protocol
32 bit	Yes	VM310_3	VME
32 bit D/ 64 bit A	Yes	VM310_1	VME
64 bit A and D	Yes	VM310_2	VME

Connecting the 1680/90/9xx Agilent logic analyzer to the FS3100

For a diagram on logic analyzer cable attachments to the probe click the Properties button on the General Purpose Probe icon from the overview tab. When you click the Properties button another window will open showing what probe pods are attached to each logic analyzer module cable pods. If you select one of the entries from the list in the window another window will open up showing the signal name on each pin of the connector the cables are attached to.

Timing Analysis with the 1680/90/9xx

Changing between State and Timing analysis only requires that the FS3100 probe switch position is changed and the selection on the 1690x analyzer is changed.

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

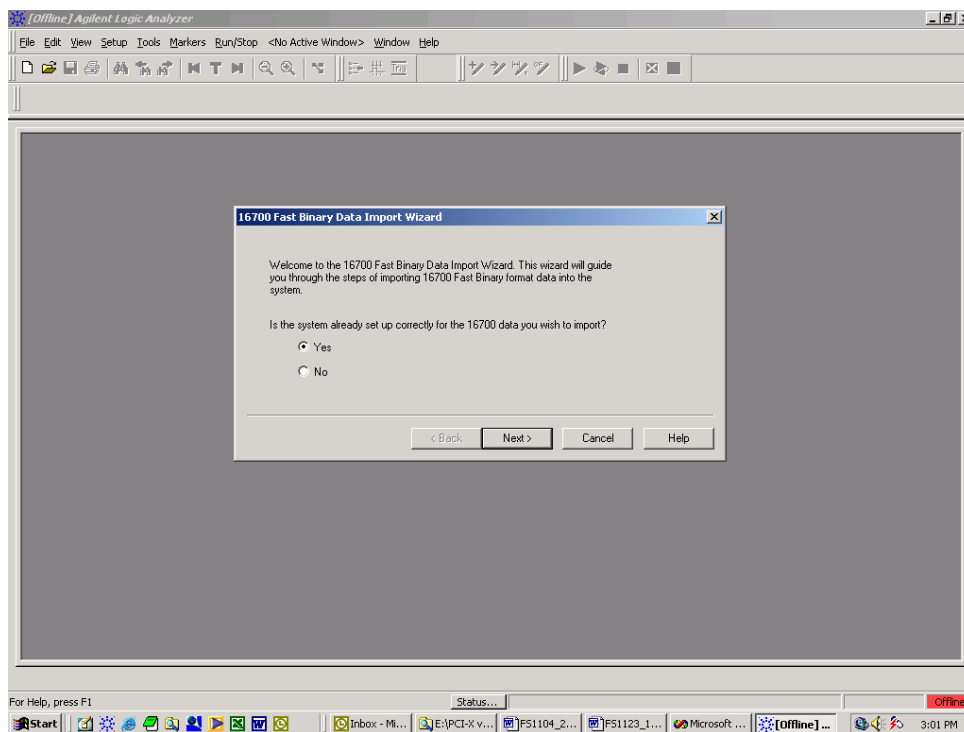
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may receive additional licenses, please contact the FuturePlus Sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up 1680/90/900 analyzer". Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select Cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select "yes" when it asks if the system is ready to import 16700 data.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product.

Installing the FS3100

The FS3100 Analysis Probe Interface board can be installed in any slot of the VME/VXI bus system. It can be installed as a separate board or as an extender board in "B" size systems. The following steps explain how to install the FS3100 Analysis Probe Interface board in a "B" or "C" size target system:

Note

If there are boards in higher number slots than the Analysis Probe interface board, refer to the section "Daisy-Chaining" on page 6 for information on setting the jumpers.

1. If the FS3100 Analysis Probe Interface board will be used as an extender board, remove the current VME/VXI board from its socket on the target system and store it in a protected environment.
2. If you are installing the Analysis Probe interface board into a "C" size target system, remove the two board supports from the Analysis Probe interface board (see figure 2-3).
3. Align the FS3100 Analysis Probe Interface board with the appropriate slot on the target system, and plug the board into the connectors (see figure 2-3).

Note

Do not use the FS3100 Analysis Probe Interface as an extender board for VME/VXI "C" size systems.

4. If the FS3100 Analysis Probe Interface board is being used as an extender board in a "B" size target system, align the appropriate VME/VXI board with the slot on the end of the FS3100 Analysis Probe Interface board. Then plug the VME/VXI board into the connectors on the FS3100 Analysis Probe Interface board (see figure 2-3).

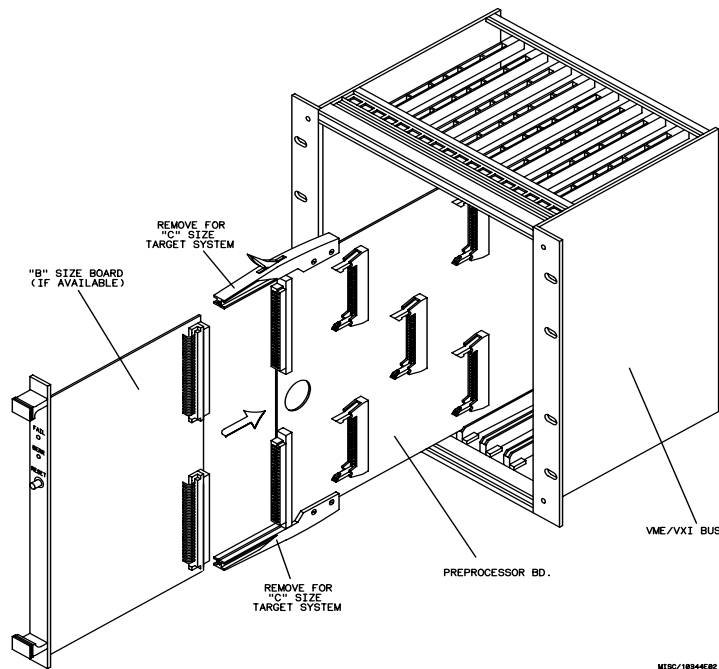


Figure 2-3 Installing the FS3100 Board

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for VME64/VXI or VME32/VXI bus analysis by loading the appropriate bus configuration file. Loading this file will also load the appropriate protocol decoder. Both protocol decoders interpret VME and VXI bus transactions. The IAVXID64 protocol decoder decodes memory transactions in the A16 address range C000H to FFFFH in terms of VXI protocols and definition. The IAVMED64 file decodes these addresses as pure VME references. To load the configuration and protocol decoder:

1. Install the FS3100 flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
 - For the 1650 series logic analyzers, select the I/O Disk Operations menu;
 - For the 16500 series logic analyzers, select the System Front Disk menu.
 - For the 16700/702 frames, open file manager and select flexible drive.
 - For the 1690x frames, the configuration files will be in a desktop folder named "FS1135"
3. Configure the menu to "Load" the analyzer with the appropriate configuration file from table 2-1/2-2.
4. For the 1660A/61A, 167x and 16500 series logic analyzers, select the configuration file with the knob, then touch "All" and select the correct module.
5. Execute the load operation to load the file into the logic analyzer.

The VME Inverse Assemblers are loaded by default. For VXI use, configure the menu to "Load" one of the following inverse assemblers, using steps three through five above:

- IAVMED64 for VME or VXI inverse assembly without decoding VXI registers.
- IAVXID64 for VME or VXI inverse assembly including decoding VXI registers.

State Format Specification

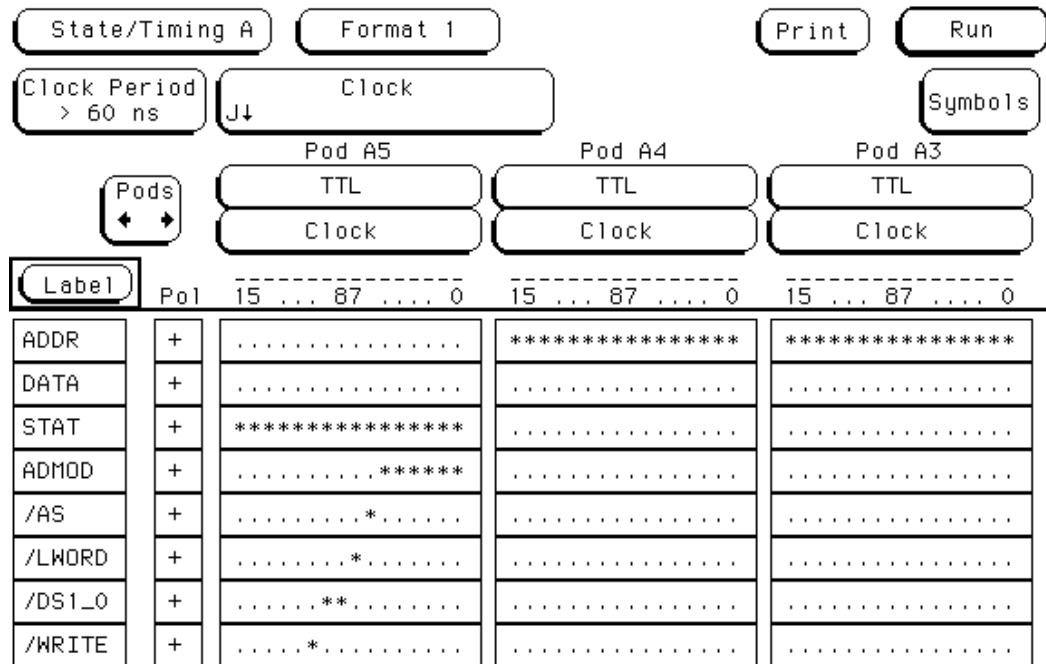
When you use the FS3100 VME/VXI Bus Analysis Probe Interface for state analysis, the format specification will be set up by the software as shown in figures 2-4 and 2-5.

Note

For those logic analyzers which have a Clock Period field (1650A, 1650B, 1652B, 16510A, 16510B, and 16511B), the Clock Period field in figures 2-4 and 2-5 should remain in the current selection (> 60 ns) for proper Analysis Probe interface operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

Note

In figures 2-4 and 2-5, additional labels are listed offscreen. To view these signals, select the Label field and rotate the knob on the front panel clockwise.



Note

In figures 2-4 and 2-5, additional labels are listed offscreen. To view these signals, select the Label field and rotate the knob on the front panel clockwise.

Figure 2-4 State Format Specification

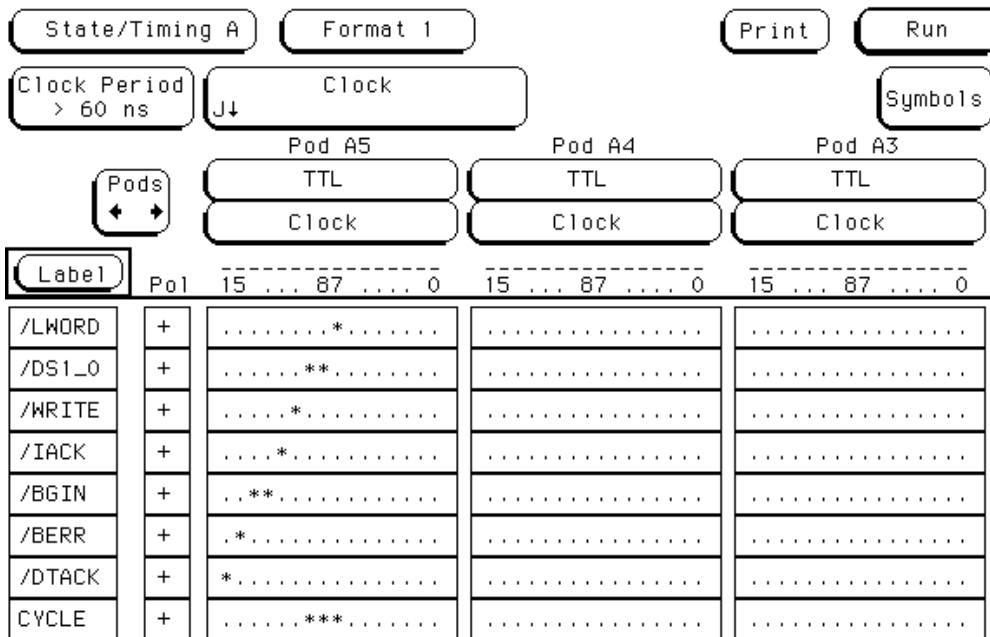


Figure 2-5 State Format Specification

Acquiring Data

To acquire data, touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full or when you touch STOP.

Note

The logic analyzer will flash "Slow or Missing Clock" when data is not being transmitted across the bus.

Listing Menu

Captured data is displayed as shown in figure 2-6. This figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages, and phases of the VME/VXI bus.

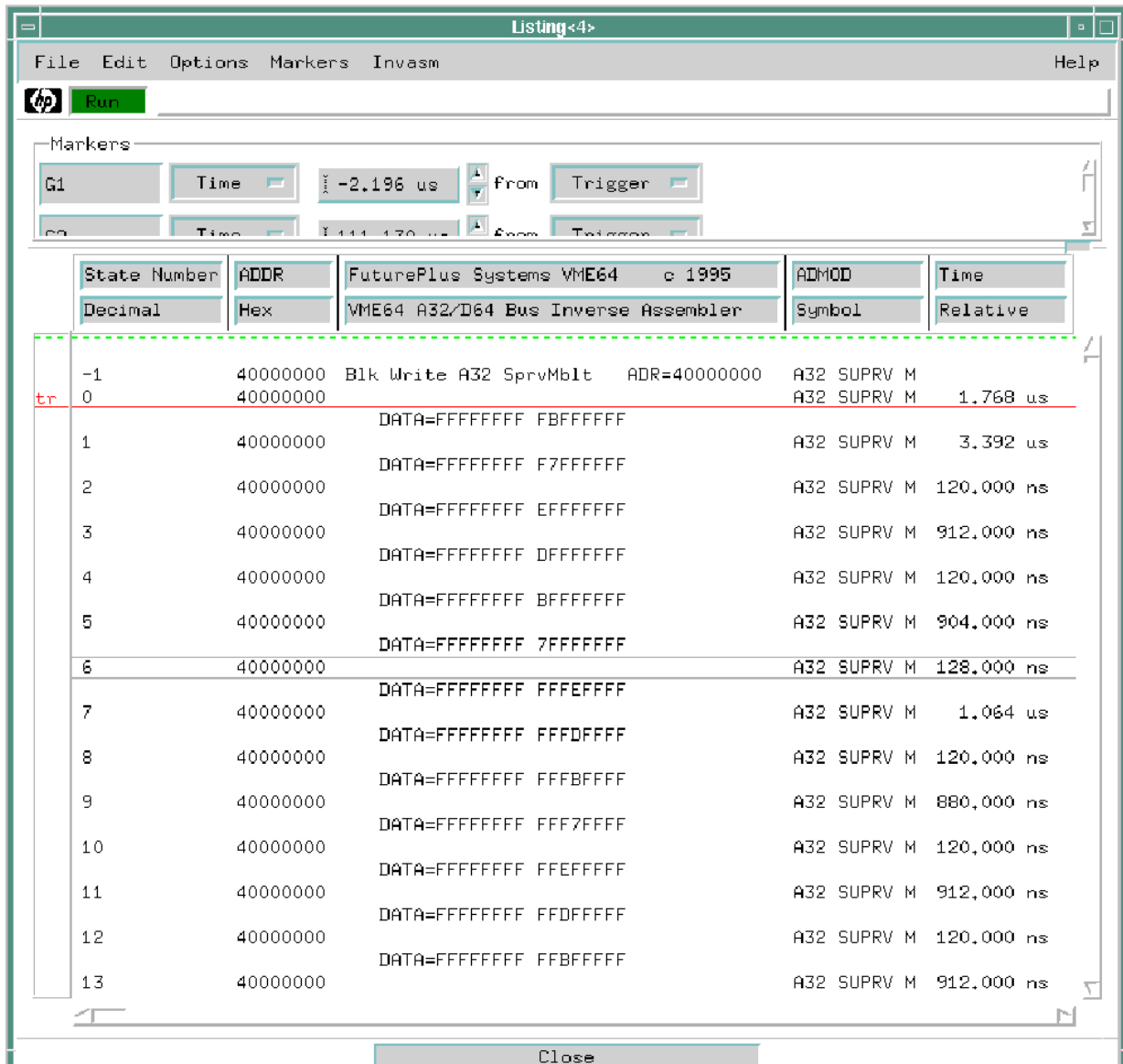


Figure 2-6 VME State Listing display (picture taken from the 16505A Prototype analyzer)

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 2-4 lists the symbols for the ADMOD label. Table 2-5 lists the symbols for the ADDR, /DS1_0, /BGIN, CYCLE, and /WRITE labels. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve display space.

Table 2-4. ADMOD Label Symbols

Label	Symbol	Pattern					
ADMOD	A24 SUPRV BLK	1	1	1	1	1	1
	A24 SUPRV PGM	1	1	1	1	1	0
	A24 SUPRV DATA	1	1	1	1	0	1
	A24 SUPRV MBLT	1	1	1	1	0	0
	A24 NONPRIV BLK	1	1	1	0	1	1
	A24 NONPRIV PGM	1	1	1	0	1	0
	A24 NONPRIV DATA	1	1	1	0	0	1
	A24 NONPRIV MBLT	1	1	1	0	0	0
	A40 BLT	1	1	0	1	1	1
	A40 LCK	1	1	0	1	0	1
	A40 ACCESS	1	1	0	1	0	0
	A24 LCK	1	1	0	0	1	0
	A16 SUPRV	1	0	1	1	0	1
	A16 NONPRIV	1	0	1	0	0	1
	A16 LCK	0	1	1	1	0	0
	USER DEFINED	0	1	x	x	x	x
	A32 SUPRV BLK	0	0	1	1	1	1
	A32 SUPRV PGM	0	0	1	1	1	0
	A32 SUPRV DATA	0	0	1	1	0	1
	A32 SUPRV MBLT	0	0	1	1	0	0
	A32 NONPRIV BLK	0	0	1	0	1	1
	A32 NONPRIV PGM	0	0	1	0	1	0
	A32 NONPRIV DATA	0	0	1	0	0	1
	A32 NONPRIV MBLT	0	0	1	0	0	0
	A32 LCK	0	0	0	1	0	1
	A64 LCK	0	0	0	1	0	0
A64 BLK	0	0	0	0	1	1	
A64 SINGLE TRANS	0	0	0	0	0	1	
A64 MBLT	0	0	0	0	0	0	

Table 2-5. ADDR, /DS1_0, /BGIN, CYCLE, and /WRITE Symbols

Label	Symbol	Pattern	
ADDR	DEV0	C000 to C03F	
	DEV1	C040 to C07F	
	DEV2	C080 to C0BF	
	DEV3	C0C0 to C0FF	
/DS1_0	MULTI	0	0
	EVEN	0	1
	ODD	1	0
	ADDR	1	1
/BGIN	BG0	0	0

	BG1	0	1		
	BG2	1	0		
	BG3	1	1		
CYCLE	ADDR ONLY	1	1	x	x
	QUAD 0-3	0	0	0	0
	UNALIGN 1-2	0	0	0	1
	DOUBLE 0-1	0	0	1	0
	DOUBLE 2-3	0	0	1	1
	UNALIGN 0-2	0	1	0	0
	ILLEGAL	0	1	0	1
	SINGLE 0	0	1	1	0
	SINGLE 2	0	1	1	1
	UNALIGN 1-3	1	0	0	0
	ILLEGAL	1	0	0	1
	SINGLE 1	1	0	1	0
	SINGLE 3	1	0	1	1
/WRITE	READ	1			
	/WRITE	0			

Bus Grant Interpretation

In the State mode, the four Bus Grant signals are combined logically in the FS3100 Analysis Probe Interface and sent to the logic analyzer as two signals. Figure 2-7 shows the schematic and truth table for the Bus Grant signals.

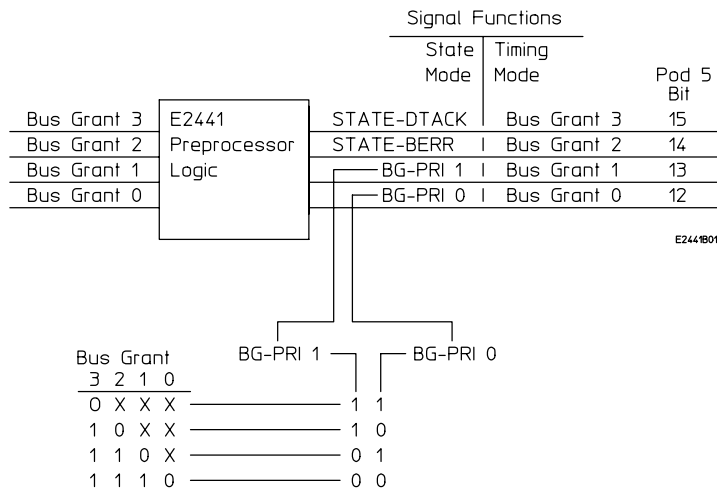


Figure 2-7 Bus Grant Signals

Address Interpretation

If a symbol is defined for the address, or for the range in which the address lies, the symbol (and offset) is displayed by the inverse assembler. For example, the address C000H could be translated as SYMBOL+00H. This format is particularly helpful for VXI cards where certain address ranges are associated with a particular card. For A16 addresses in the range of C000H to FFFFH, which are the VXI configuration registers, the default symbol LA# is supplied. The # sign represents the logical address of the VXI device. Other symbols can be defined in the Symbols menu of the Format menu. For more information, refer to the reference manual for your logic analyzer.

VXI Bus Translation

The ADDRESS, DATA, Modifier, and Transfer Type are decoded for all VME and VXI bus transactions. If a bus transaction address lies in the A16 range C000H to FFFFH, then the transaction is decoded as a read or write to a VXI configuration register. A maximum of 256 VXI devices can have configuration registers in this range, on 64 byte offsets. The VME/VXI Analysis Probe interface treats memory transactions to configuration registers as shown in the following table:

Table 2-6. VXI Bus Translation

Offset	Transaction Type	Interpretation
00	Read	ID Register
00	Write	Assign Logical Address
02	Read	Type Register
02	Write	Reserved
04	Read	Status Register
04	Write	Control Register
06	R/W	Offset Register
08	Read	Message Protocol Register
08	Write	Message Signal Register
0A	Read	Message Response Register
0A	Write	Message Data Extended Register
0C	R/W	Message Data High Register
0E	Read	Message Data Low
0E	Write	Message Word Serial
10	R/W	Message A24 Pointer High
12	R/W	Message A24 Pointer Low
14	R/W	Message A32 Pointer High
16	R/W	Message A32 Pointer Low
18 - 1C	R/W	Undefined

Note

The decoding may be incorrect if the device is a memory device or a register based device that uses the register offsets 08H to 16H.

When a bus transaction lies within the range of the VXI configuration register, the address is decoded in two parts: a logical address and a register offset. The register offset is used by the VXI inverse assembler to interpret the DATA bit pattern. For example, if the data DEFFH were written to the offset 0EH, it would be interpreted as a Word Serial Byte Request command.

For some registers, such as the Response Register, offset 0AH, the DATA pattern indicates whether particular flags are active. When decoding these registers, the inverse assembler interprets the pattern and shows any flags that are active (TRUE). For example, if LOCKED* = 0, the flag <LOCK> is shown. If no flags are currently active, the message "No Flags Set" is displayed.

Error Messages

The following list identifies the types of errors that are detected by the inverse assembler:

**** ERROR: MUST BE READ FOR IACK* SEQUENCE ****

This message means that the IACK* bit was 0 (indicating that the bus cycle was an interrupt acknowledge), and that the WRITE* line was also 0. This violates the VME/VXI interrupt handler definition.

**** BUS ERROR: Data NOT Transferred ****

This message indicates that the BERR* bit was 0. This bit can be driven low by either the bus timer (when it detects the absence of data acknowledge (DTACK*) during a data bus cycle), or by a card which implements the fast handshake protocol.

**** BAD COMBINATION OF DS1*, DS0*, LWORD*, A01**

This message indicates that an illegal combination of DS1*, DS0*, LWORD*, and A01 was present on the bus. VME defines the illegal cycle types as shown in table 2-7.

Table 2-7. Illegal Cycle Types

DS1*	DS0*	LWORD*	A01	CYCLE
high	low	low	high	DTB
low	high	low	high	DTB

Chapter 3 Timing Analysis

Introduction

The FS3100 Bus Analysis Probe Interface board can also be used for timing analysis. This chapter explains how to configure the FS3100 Bus Analysis Probe Interface for timing analysis of a VME/VXI bus system using “B” or “C” size cards.

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the FS3100 VME/VXI Bus Analysis Probe Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

1. Set the State/Timing switch to the top (Timing) position for timing analysis (see figure 1-1).
2. Set jumpers across pins 1 and 2 of jumpers J2 through J6 if the daisy chain on signals BG3IN* through BG0IN* and IACK* need to continue to the next slot (see page 6). Otherwise, set jumpers across pins 2 and 3. Note that if the Analysis Probe interface board is used as an extender, the jumpers must be set across pins 2 and 3.
3. Set jumper J1 to select BERR or IRQ1. The factory settings, and the configuration file, are set for BERR. If you select IRQ1, reassign the bit (see page 7).
4. Plug the logic analyzer cables into the Analysis Probe interface board (see table 3-1).
5. If you are installing the Analysis Probe interface board into a “C” size target system, remove the two board supports on the Analysis Probe interface board (see figure 2-3).
6. Install the Analysis Probe interface board in the target system and, if necessary, plug the VME/VXI board into the Analysis Probe interface board (see page 13).
7. Load the logic analyzer configuration by loading the appropriate file from the Analysis Probe interface disk (see page 24).

Connecting to the FS3100

Connect the logic analyzer cables to the FS3100 Analysis Probe Interface pods as shown in the following tables.

Table 3-1. Connections and Configuration Files (Timing Analysis) for VME32/VXI systems

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
1650A, 1650B, 16510A, 1652B and 16510B	F510_0T	P4	P5	**	P3	P2	P1
16550A	F550_02	P6**	P5	P4	P3	P2	P1
16554/5/6/7 Master Card 167x Pods 1-4	F555_02			P4	P3	P2	P1
16554/5/6/7 Expander Card Pods 1-2 167x Pods 5-6	F555_02	P6**	P5				
1660A/61A	F660_00	P6**	P5	P4	P3	P2	P1

**To see timing for the signals on the Analysis Probe interface P4, remove the logic analyzer cable from P2 and connect to P4.

Table 3-2. Connections and Configuration Files (Timing Analysis) for VME/VXI A32/D64 systems

Logic Analyzer	File	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
1650A, 1650B, 16510A, 1652B and 16510B, 16511B	not supported	--	--	--	--	--	--	--	--
1660	F660_00	P8	P7	P6**	P5	P4	P3	P2	P1
16550A Master Card	F550_00			P6**	P5	P4	P3	P2	P1
16550A Expander Card		P2	P1						
1655x Master Card 1670 PODS 1-4	F555_00					P4	P3	P2	P1
1655x Expander Card 1670 PODS 5-8		P4	P3	P2**	P1				
1661A	not supported								

Table 3-3. Connections and Configuration Files (Timing Analysis) for VME/VXI A64/D64 systems

Logic Analyzer	File	Pod 10	Pod 9	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
1650A, 1650B, 16510A, 1652B and 16510B, 16511B	not supported	--	--	--	--	--	--	--	--	--	--
1660	not supported	--	--	--	--	--	--	--	--	--	--
16550A Master Card	F550_01					P6	P5	P4	P3	P2	P1
16550A Expander Card		P4	P3	P2	P1						
1655x Master Card	F555_01							P4	P3	P2	P1
1655x Expander Card 1				P4	P3	P2	P1				
1655x Expander Card 2		P2	P1								
1661A, 167x	not supported										

Installing the FS3100

The FS3100 Analysis Probe Interface board can be installed in any slot of the VME/VXI bus system. It can be installed as a separate board or as an extender board in “B” size systems. The following steps explain how to install the FS3100 Analysis Probe Interface board in a “B” or “C” size target system:

Note

If there are boards in higher number slots than the Analysis Probe interface board, refer to the section “Daisy-Chaining” on page 6 for information on setting the jumpers.

1. If the FS3100 Analysis Probe Interface board will be used as an extender board, remove the current VME/VXI board from its socket on the target system and store it in a protected environment.
2. If you are installing the Analysis Probe interface board into a “C” size target system, remove the two board supports from the Analysis Probe interface board (see figure 2-3).
3. Align the FS3100 Analysis Probe Interface board with the appropriate slot on the target system and plug the board into the connectors (see figure 2-3).

Note

Do not use the FS3100 Analysis Probe Interface board as an extender board for VME/VXI “C” size systems.

4. If the FS3100 Analysis Probe Interface board is being used as an extender board in a “B” size target system, align the appropriate VME/VXI board with the slot on the end of the FS3100 Analysis Probe Interface board. Then plug the VME/VXI board into the connectors on the FS3100 Analysis Probe Interface board (see figure 2-3).

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for VME/VXI bus timing analysis by loading the appropriate VME/VXI bus configuration file. To load the configuration file:

1. Install the FS3100 flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
 - For the 1650 series logic analyzers, select the I/O Disk Operations menu;
 - For the 16500 series logic analyzers, select the System Front Disk menu.
3. Configure the menu to “Load” the analyzer with the appropriate configuration file from table 3-1 thru 3-3.
4. For the 1660A/61A, 167x and 16500 series logic analyzers, select the configuration file with the knob, then touch “All” and select the correct module.
5. Execute the load operation to load the file into the logic analyzer.
6. For the 1660A/61A, 167x and 16550A Logic Analyzers, go to the “System Configuration” menu and select “Timing”.

Timing Format Specification

When you use the VME/VXI Bus Analysis Probe Interface for timing analysis, the format specification will be set up by the software as shown in figure 3-1.

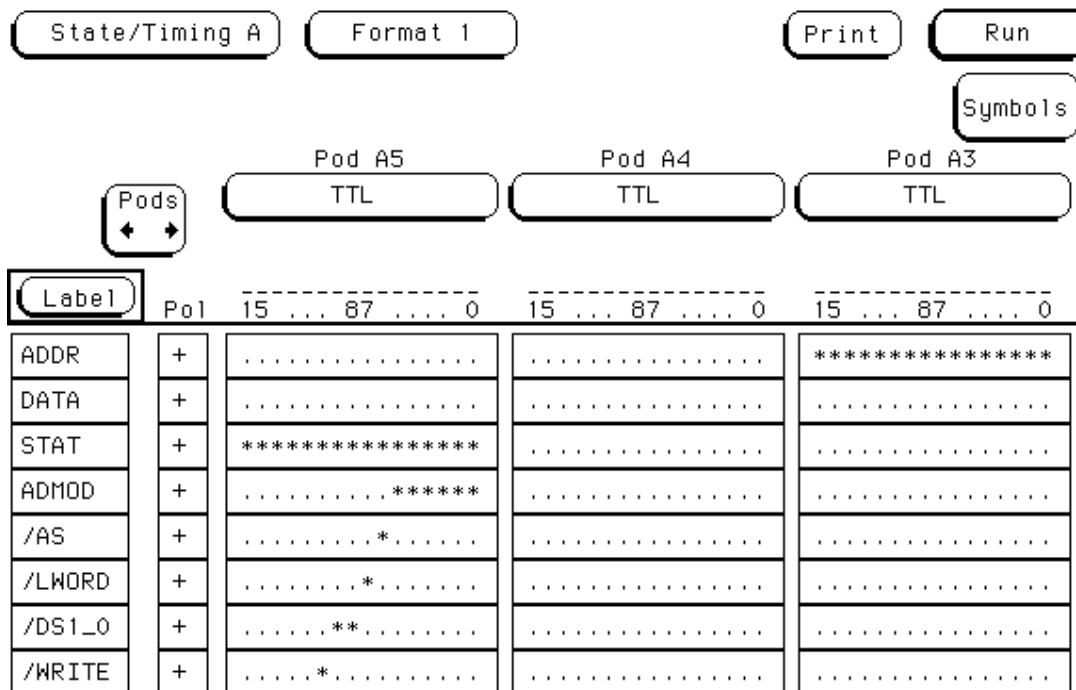


Figure 3-1 Timing Format Specification

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer meets its trigger condition or when you touch STOP. The logic analyzer will flash "Waiting for Trigger" when data is not being transmitted across the bus.

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 3-4 lists the symbols for the /WRITE, /BREQ, AND IRQ2_7 labels. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve display space.

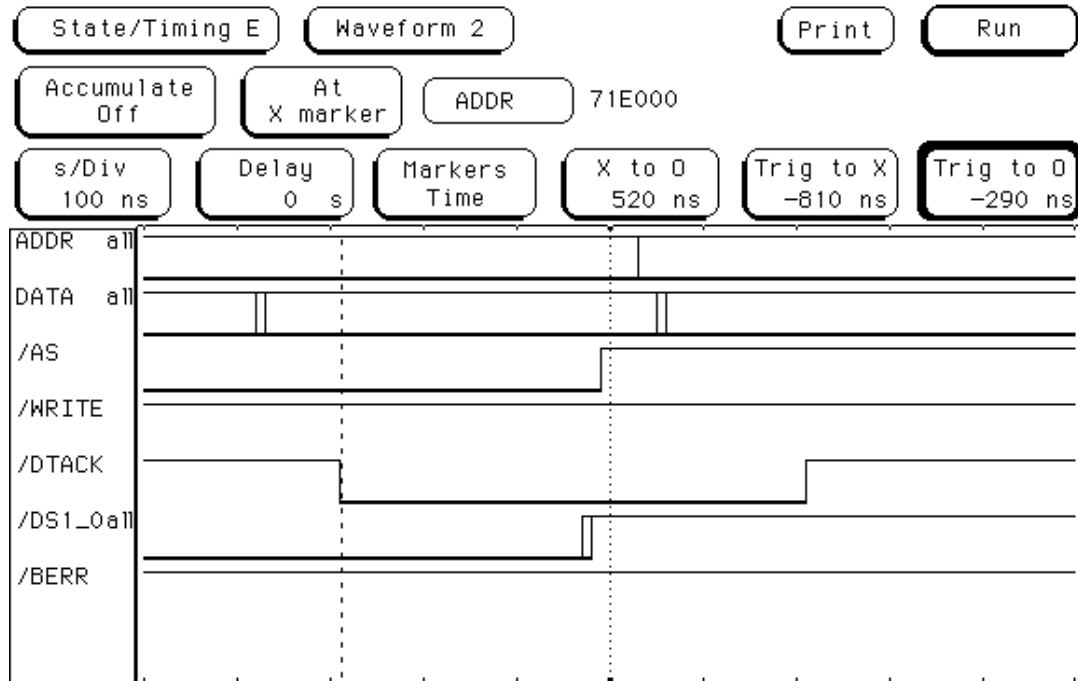
Table 3-4. Timing Symbols

Label	Symbol	Pattern
/WRITE	READ	1
	/WRITE	0
/BREQ	BRQ3	0 x x x
	BRQ2	1 0 x x
	BRQ1	1 1 0 x
	BRQ0	1 1 1 0
IRQ2_7	IRQ7	0 x x x x x
	IRQ6	1 0 x x x x
	IRQ5	1 1 0 x x x
	IRQ4	1 1 1 0 x x
	IRQ3	1 1 1 1 0 x
	IRQ2	1 1 1 1 1 0

Waveforms Menu

Captured data is displayed as shown in figure 3-2.

Figure 3-2. Waveform Display



Chapter 4 General Information

Introduction

This chapter provides additional reference information including the characteristics and signal connections for the FS3100 VME/VXI Bus Analysis Probe Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS3100 VME/VXI Bus Analysis Probe Interface. These characteristics are included as additional information for the user.

Analysis Probe Interface Compatibility:

16/32/64-bit VME/VXI bus systems using "B" or "C" size cards.

Standard Supported:

VME Rev. C.1 (except for capacitive loading).
Standard VXI Revision 1.3 (except for capacitive loading).
VME64 rev 1.9 (except for capacitive loading)

Accessories Required:

None.

Power Requirements:

Maximum 600 mA at +5 volts from the logic analyzer.

Number of Probes Used:

For 32 bit analysis: Five or six 16-channel probes.
For A32/D64: Eight PODS
For A64/D64: Ten PODS

Signal Line Loading

VIL = -150 uA, plus 30 pF (maximum) on the following lines:

DTACK*, BERR*, DS0*, DS1*, WRITE*, AS*, BBSY*, BGIN(3:0)*

VIL = -150 uA, plus 25 pF (maximum) on all other lines.

Note

If the FS3100 Analysis Probe Interface board is used as an extender board, you must take into account any additional loading from the board that is installed in the FS3100 Analysis Probe Interface board.

Sampling Time

The following signals are sampled approximately 18 ns after AS goes low true: ADDRESS, ADDRESS MODIFIERS, LWORD and IACK.

The following signals are sampled approximately 18 ns after DS_A goes low true in a WRITE cycle or approximately 18 ns after DTACK goes low in a READ cycle: DATA, DS(1:0) and WRITE.

Timing Measurement Skew:

All signals are passed through 74ACT573 buffers in the timing mode. The worst case published skew is 8 ns for these parts (typical skew is less than 4 ns).

Environmental Temperature:

- Operating: 0 to +55° C (+32 to +131° F)
- Nonoperating: 40 to +75° C (-40 to +167° F)

Altitude:

- Operating: 4,600 m (15,000 ft)
- Nonoperating: 15,300 m (50,000 ft)

Humidity:

Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the Analysis Probe interface.

Analysis Probe Interface Description

The FS3100 VME/VXI Bus Analysis Probe Interface provides an interface between a VME/VXI bus system and the supported logic analyzers. Figure 4-1 shows the block diagram for the clocking circuitry and switches on the FS3100 Analysis Probe Interface.

The FS3100 has two Programmed Logic Arrays that generate a latching strobe for the signal lines of the VME/VXI bus. The signals are latched into 74ACT573 transparent latches. When the STATE/TIMING switch is in the TIMING position, these latches are in the buffer mode and all signals flow straight through to the logic analyzer.

The on-board logic is an asynchronous state machine for the purpose of decoding address broadcast cycles, pipelined cycles, block transfers or single transfer cycles. This state machine also generates the Master Clock to the logic analyzer.

State/Timing Switch

There are four signals that change between the State and Timing modes. These are the BG_IN(3:0) lines on Pod 5, bits 12 through 15. These four lines are coded for the inverse assembler software in the State mode. In Timing mode, the BG_IN(3:0) lines are buffered straight through for timing analyses. The State/Timing switch selects the appropriate mode. Note that the switch must be in the correct position for proper operation.

The State/Timing switch changes four of the inputs to pod 5. In the State mode, the four most significant inputs to pod 5 are latched values of the Bus Grant lines, BERR, and DTACK. The four Bus Grant lines are priority encoded into two lines, to free up more state lines (see Chapter 2).

In the timing mode, the inputs to pod 5 are the actual BGxIN(3:0)* lines from the VME/VXI bus. These four lines are necessary in order to see the timing during a bus request operation.

Pod 6 (for 16/32 bit analysis only)

Five-pod logic analyzers do not use P6 in the state mode. For timing measurements, P4 can be moved up to P6 to capture the signals available on P6 at the sacrifice of the upper 16 address lines A16 thru A31. In reality the user may sacrifice any of the pods for use in P6, but the pod assignments in the Format menu must match the connections.

Master Clock

The Master Clock is the falling edge of the J clock on pin 3 of Pod 1. In an address broadcast cycle, the Master Clock is generated when AS goes from low to high. In a Data Transfer cycle the Master Clock is generated when DTACK or BERR goes from low to high.

Slave Clock

The slave clock is based on the falling edge of AS and is found on POD 3 pin 17 (L Clock).

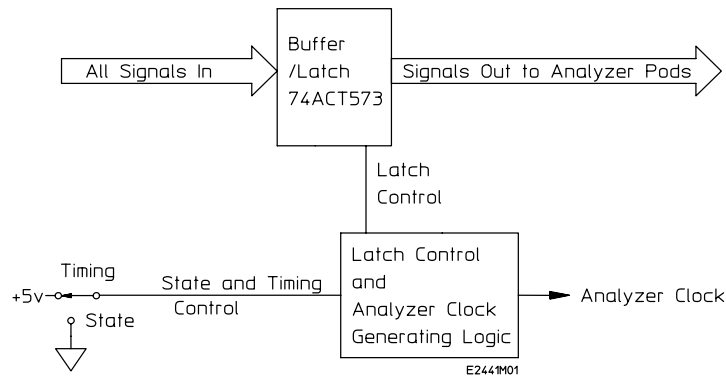


Figure 4-1 FS3100 block diagram

Signal Connections

The FS3100 VME/VXI Bus Analysis Probe Interface monitors 83 lines for state information and 97 lines for timing information. Table 4-1 lists the VME/VXI bus signals and connections for the logic analyzers.

Table 4-1. FS3100 Signal Connections

Logic Analyzer POD	Logic Analyzer Channel	VME/VXI Pin	Signal Name	Format Menu Label
P1	0	J4-A1	D0	DATA
P1	1	J4-A2	D1	DATA
P1	2	J4-A3	D2	DATA
P1	3	J4-A4	D3	DATA
P1	4	J4-A5	D4	DATA
P1	5	J4-A6	D5	DATA
P1	6	J4-A7	D6	DATA

P1	7	J4-A8	D7	DATA
P1	8	J4-C1	D8	DATA
P1	9	J4-C2	D9	DATA
P1	10	J4-C3	D10	DATA
P1	11	J4-C4	D11	DATA
P1	12	J4-C5	D12	DATA
P1	13	J4-C6	D13	DATA
P1	14	J4-C7	D14	DATA
P1	15	J4-C8	D15	DATA
P2	0	J10-B14	D16	DATA
P2	1	J10-B15	D17	DATA
P2	2	J10-B16	D18	DATA
P2	3	J10-B17	D19	DATA
P2	4	J10-B18	D20	DATA
P2	5	J10-B19	D21	DATA
P2	6	J10-B20	D22	DATA
P2	7	J10-B21	D23	DATA
P2	8	J10-B23	D24	DATA
P2	9	J10-B24	D25	DATA
P2	10	J10-B25	D26	DATA
P2	11	J10-B26	D27	DATA
P2	12	J10-B27	D28	DATA
P2	13	J10-B28	D29	DATA
P2	14	J10-B29	D30	DATA
P2	15	J10-B30	D31	DATA
P2	17	*		S_DX
P3	0	*	A0	ADDR
P3	1	J4-A30	A1	ADDR
P3	2	J4-A29	A2	ADDR
P3	3	J4-A28	A3	ADDR
P3	4	J4-A27	A4	ADDR
P3	5	J4-A26	A5	ADDR
P3	6	J4-A25	A6	ADDR
P3	7	J4-A24	A7	ADDR
P3	8	J4-C30	A8	ADDR
P3	9	J4-C29	A9	ADDR
P3	10	J4-C28	A10	ADDR
P3	11	J4-C27	A11	ADDR
P3	12	J4-C26	A12	ADDR
P3	13	J4-C25	A13	ADDR
P3	14	J4-C24	A14	ADDR
P3	15	J4-C23	A15	ADDR
P3	17	*		SL_CLK
P4	0	J4-C22	A16	ADDR
P4	1	J4-C21	A17	ADDR
P4	2	J4-C20	A18	ADDR
P4	3	J4-C19	A19	ADDR
P4	4	J4-C18	A20	ADDR
P4	5	J4-C17	A21	ADDR
P4	6	J4-C16	A22	ADDR
P4	7	J4-C15	A23	ADDR
P4	8	J10-B4	A24	ADDR

P4	9	J10-B5	A25	ADDR
P4	10	J10-B6	A26	ADDR
P4	11	J10-B7	A27	ADDR
P4	12	J10-B8	A28	ADDR
P4	13	J10-B9	A29	ADDR
P4	14	J10-B10	A30	ADDR
P4	15	J10-B11	A31	ADDR
P5	0	J4-B16	AM0	STAT
P5	1	J4-B17	AM1	STAT
P5	2	J4-B18	AM2	STAT
P5	3	J4-B19	AM3	STAT
P5	4	J4-A23	AM4	STAT
P5	5	J4-C14	AM5	STAT
P5	6	J4-A18	AS	STAT
P5	7	J4-C13	LWORD	STAT
P5	8	J4-A13	DS0	STAT
P5	9	J4-A12	DS1	STAT
P5	10	J4-A14	WRITE	STAT
P5	11	J4-A20	IACK	STAT
P5	12	* / J4-B4	BG_PRI0 / BG0IN	STAT
P5	13	* / J4-B6	BG_PRI1 / BG1IN	STAT
P5	14	* / J4-B8	BERR_STATE / BG2IN	STAT
P5	15	* / J4-B10	DTACK_STATE / BG3IN	STAT
P6	0	J4-B12	BR0	(timing)
P6	1	J4-B13	BR1	(timing)
P6	2	J4-B14	BR2	(timing)
P6	3	J4-B15	BR3	(timing)
P6	4	J4-B1	BBSY	(timing)
P6	5	J4-B2	BCLR	(timing)
P6	6	J4-C11/B30 **	BERR/IRQ1 **	(timing)
P6	7	J4-B29	IRQ2	(timing)
P6	8	J4-B28	IRQ3	(timing)
P6	9	J4-B27	IRQ4	(timing)
P6	10	J4-B26	IRQ5	(timing)
P6	11	J4-B25	IRQ6	(timing)
P6	12	J4-B24	IRQ7	(timing)
P6	13	J4-A21	IACKIN	(timing)
P6	14	J4-A22	IACKOUT	(timing)
P6	15	J4-A16	DTACK	(timing)
P6	17	J2-B3	RETRY	Timing/State
P7	0	J4-C13	LWORD	DATA_B
P7	1	J4-A30	A1	DATA_B
P7	2	J4-A29	A2	DATA_B
P7	3	J4-A28	A3	DATA_B
P7	4	J4-A27	A4	DATA_B
P7	5	J4-A26	A5	DATA_B
P7	6	J4-A25	A6	DATA_B
P7	7	J4-A24	A7	DATA_B

P7	8	J4-C30	A8	DATA_B
P7	9	J4-C29	A9	DATA_B
P7	10	J4-C28	A10	DATA_B
P7	11	J4-C27	A11	DATA_B
P7	12	J4-C26	A12	DATA_B
P7	13	J4-C25	A13	DATA_B
P7	14	J4-C24	A14	DATA_B
P7	15	J4-C23	A15	DATA_B
P7	17			
P8	0	J4-C22	A16	DATA_B
P8	1	J4-C21	A17	DATA_B
P8	2	J4-C20	A18	DATA_B
P8	3	J4-C19	A19	DATA_B
P8	4	J4-C18	A20	DATA_B
P8	5	J4-C17	A21	DATA_B
P8	6	J4-C16	A22	DATA_B
P8	7	J4-C15	A23	DATA_B
P8	8	J10-B4	A24	DATA_B
P8	9	J10-B5	A25	DATA_B
P8	10	J10-B6	A26	DATA_B
P8	11	J10-B7	A27	DATA_B
P8	12	J10-B8	A28	DATA_B
P8	13	J10-B9	A29	DATA_B
P8	14	J10-B10	A30	DATA_B
P8	15	J10-B11	A31	DATA_B

- When the State/Timing Switch is in the State position, the signals listed to the left are generated by the Analysis Probe interface and displayed on the logic analyzer; when the switch is in the Timing position, the signals listed to the right are captured by the logic analyzer.
 - ** This signal is determined by jumper J1 location (see Chapter 1).
 - * This signal is generated on the Analysis Probe interface.

Servicing

The repair strategy for the FS3100 is board replacement. Contact FuturePlus Systems Technical Support for further information on servicing the board.

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes “ “. Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact FuturePlus Systems Technical Support for additional assistance.

Target Board Will Not Boot

If the target board will not boot after connecting the Analysis Probe interface, the microprocessor or the Analysis Probe interface may not be installed properly, or they may not be making electrical contact. Verify that the logic analyzer cables are in the proper sockets of the Analysis Probe interface and firmly inserted.

“Slow or Missing Clock”

This error message might occur if the logic analyzer cards are not firmly seated in the 16500 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly, **if there is no activity on the bus**, or if the FS3100 asynchronous circuitry is not recognizing valid bus activity. Ensure that the target system is on and operating properly.

If the error message persists, check that the logic analyzer pods are connected to the proper connectors, as listed in tables 2-2 or 3-2.

Slow Clock

If you have the Analysis Probe interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the FS3100 and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1).

If +5 V isn't observed across these pins, check the internal Analysis Probe fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.

If +5 V is observed across these pins and you feel confident that the +5 V is getting to the Analysis Probe interface, contact your nearest FuturePlus Systems Sales/Service Office for information on servicing the board.

“No Configuration File Loaded”

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the 16500 disk operation menu. **Selecting Load {All} will cause incorrect operation when loading most Analysis Probe interface configuration files.**

“Selected File is Incompatible”

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

“... Inverse Assembler Not Found”

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

Check the activity indicators for status lines locked in a high or low state.

Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.

Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the 1650A, 1651A, and 16510A Logic Analyzers if there is no activity the fuse which allows power to the Analysis Probe interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or Analysis Probe interface connections are probably loose. Check all connections.

“State Clock Violates Overdrive Specification”

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note

The error message “State Clock Violates Overdrive Specification” should only occur for 1650A,B, 1652B, 16510A,B, and

16511B Logic Analyzers with the Clock Period field set to <60 ns. If this error message is observed with the Clock Period set to >60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest FuturePlus Systems Sales/Service Office for information on servicing the instrument.

“Waiting for Trigger”

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a “don’t care” trigger condition is set, this message indicates:

For an 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to “Slow or Missing Clock.”

For an 1650A,B, 1652B, or 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a “don’t care” pattern is always true, the “less than” condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

“Time from Arm Greater Than 41.93 ms.”

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.