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# **FS3030 Users Manual**

## **EIO PCI Analysis Probe**

**For use with Agilent Technologies Logic Analyzers**

**Revision 1.3**

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# Introduction

The FS3030 PCI Analysis Probe provides a complete interface between an EIO PCI add-in slot and the Logic Analyzer. The EIO probe also acts as an extender card, extending the EIO card under test beyond the EIO chassis.

The Analysis Probe interface is a passive bus monitor which does not assert any signals on the PCI bus. The PCI bus signals are terminated with 90k ohm/10pf terminators via the E5346A high density adapter cables at the near maximum allowed stub length so that they are matched to the logic analyzer and provide, at the same time, the worst case PCI load.

The configuration software on the diskette sets up the format specification menu of the logic analyzer for compatibility with your PCI bus. When the logic analyzer configuration file is loaded, an inverse assembler is also loaded which decodes PCI transactions into easy to read mnemonics.

The extender card functionality and logic analysis functionality of the EIO PCI Probe may be used independently of each other. That is, the logic analyzer does not need to be connected in order for the extender card connector to work. Conversely, an add-in card does not need to be installed in the add-in card connector for the logic analysis function to work.

## How to Use This Manual

This manual is organized to help you quickly find the information you need.

- **Analyzing the PCI Local Bus** chapter introduces you to the FS3030 and lists the minimum equipment required and accessories supplied for PCI bus analysis.
- The **State Analysis** chapter explains how to configure the FS3030 to perform state analysis on your PCI bus.
- The **Timing Analysis** chapter explains how to configure the FS3030 to perform timing analysis on your PCI bus.
- The **General Information** chapter provides information on the operating characteristics, the test point and cable header pinout and the mechanical drawing for the FS3030 module.

# Analyzing the PCI Local Bus

This chapter introduces you to the FS3030 and lists the minimum equipment required and accessories supplied for PCI Local Bus analysis. This chapter also contains information that is common to both state and timing analysis.

## Duplicating the Master Diskette

Before you use the FS3030 software, make a duplicate copy of the master diskette. Then store the master diskette and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the diskette wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate diskette operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

## Accessories Supplied

The FS3030 product consists of the following accessories:

- The FS3030 hardware, which includes the interface circuit module.
- The inverse assembly and configuration software on 3.5 inch diskettes.
- This operating manual

## Minimum Equipment Required

The minimum equipment required for analysis of a PCI Local Bus consists of the following equipment:

- An 16500B based logic analyzer
- The FS3030 Product
- 2 E5346A high density termination adapter cables
- A PCI target bus

## Signal Naming Conventions

This operating manual uses the same signal notation as the PCI LOCAL BUS SPECIFICATION - REVISION 2.1. That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

## Connecting the logic analyzer to the FS3030

The following explains how to connect the logic analyzer to the FS3030 for either state or timing analysis:

1. Remove the probe tip assemblies from the logic analyzer cables.
2. Plug the logic analyzer cables into the FS3030 cable headers as shown in the appropriate table.

Logic Analyzer	FS3030	Comment
Master Pod 1	Header 1	
Pod 2	Header 2	
Pod 3	Header 3	L Clock
Pod 4	Header 4	

## User Pins

The FS3030 contains 17 *User Defined* pins. These pins are available to the user to connect whatever additional signals the users wishes to view along with the PCI bus. These pins are located along the side of the FS3030 and are clearly marked.

These pins may be used to connect the individual GNT, REQ or IDSEL signals from the other slots on the PCI bus.

## How to install a PCI add-in card into the FS3030

The card edge connector of the FS3030 module can accommodate one EIO add in card. Simply align the module with the connector and gently push the module in until it is seated in the connector. There is sufficient clearance for the add-in card front plate. The FS3030/EIO add-in card combination can then be installed in any slot of the PCI Local bus.

When removing the PCI add-in card from the card edge extender connector grasp the FS3030 with one hand and the PCI add-in card with the other. Gently pry the PCI add-in card until it is free from the connector.

## Operation of the PCI add-in card

The nature of an extender card is that it extends the etch length of the bus. Due to the sensitivity of most PCI designs, extending the etch length can interfere with the PCI add-in card operation. Operation of the PCI add-in card when installed in the card edge extender connector is not guaranteed. Please check your system design if you experience failures due to poor signal fidelity.

### 66 MHz Operation

The FS3030 Analysis Probe contains series zero ohm resistors in case the system will not work with the extender card attached. Removal of these resistors may be necessary to eliminate the stub etch to the extender card connector.

## Installing the EIO PCI Analysis Probe

The FS3030 Analysis Probe can be installed in any slot of the EIO PCI Local bus that has enough mechanical clearance. The following steps explain how to install the EIO PCI Probe into the PCI Local bus.

1. Install the logic analyzer cables as described in the previous section.
2. Install the EIO add-in card into the EIO PCI Probe extender card connector.
3. Align the EIO PCI Probe with the appropriate slot on the target system and plug the probe into the PCI connector.

### Setting up the Analyzer from the diskette

The EIO Analysis Probe software includes the configuration files and inverse assembler for the logic analyzer.

The logic analyzer can be configured for PCI analysis by loading the PCI configuration file. Loading this file will load the PCI Local bus inverse assembler and configure your logic analyzer. To load the configuration and inverse assembler:

1. Install the FS3030 software flexible diskette in the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the appropriate configuration file (see table below).

Logic Analyzer	File name for State Analysis	File name for Timing Analysis
16555, 167x	F555PE	F555PE
166x	F660PE	F660PE
16550	F550PE	F550PE

3. Execute the load operation to load the file into the logic analyzer. *Please note: The target of the LOAD operation must be the logic analyzer that is connected to the EIO PCI Probe. Do not select ALL or SYSTEM as the target of the LOAD operation.*

Please note that 1655x and 16550 users do not need to reload any files from the diskette when switching between state and timing analysis.

## Setting up the 16600/16700 Analyzer

The 16600/16700 requires a special install procedure to install the PCI Inverse Assembler. To accomplish this, insert the diskette labeled PCI INVERSE ASSEMBLER INSTALLATION DISK FOR THE 16600/16700 into the 16600/700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INTALL screen select the *FLEXIBLE DISK* and *APPLY* once the title appears select it and then *DOUBLE CLICK* on the + sign and then select *INSTALL* .

**This procedure does not need to be repeated. It only needs to be done the first time the EIO PCI Analysis Probe is used.**

## Setting up the 16505A Prototype Analyzer for State and Timing Analysis

To configure the 16505A prototype analyzer insert the diskette labeled PCI INVERSE ASSEMBLER INSTALLATION DISK FOR THE 16505A into the 16505A diskette drive. From the session manager select update and follow the prompts until the prompts indicate a successful install. **This procedure does not need to be repeated. It only needs to be done the first time the PCI Analysis Probe is used.**

To load the configuration and inverse assembler:

1. Install the FS3030 software flexible diskette in the disk drive of the 16500B mainframe.
2. Go to the main 16505A window and select FILE. Configure this file menu to "Load 16500 file". After selecting diskette, load the appropriate configuration file (see table below).

Logic Analyzer	File name for State Analysis	File name for Timing Analysis
16555, 167x	F555PE	F555PE
166x	F660PE	F660PE
16550	F550PE	F550PE

3. Execute the load operation to load the file into the logic analyzer that is connected to the EIO PCI Probe.

## The Format Menu

The FS3030 diskette sets up the format menu as shown in the following table (1655x, 167x, and 166x). This format is the same for both Timing and State Analysis.

Label	Clk Inputs	Pod 4	Pod 3	Pod 2	Pod 1
STAT		9-0	14-0		
ADDR				15-0	15-0
USER17_15	M, K, J				
USER14_9		15-10			
USER8_5		6,5,1,0			
USER4_1		15-12			
C/B3_0			9-6		
INTA			11		
RESET			10		
DATA				15-0	15-0
DEVSEL			5		
STOP			4		
VDD			3		
PERR			2		
SERR			1		
PAR			0		
IDSEL		2			
GNT		3			
REQ		4			
IRDY		7			
FRAME		8			
TRDY		9			
PCICLK	L				
CYCLE		9-7	9-4		

### **The STAT variable**

The STAT variable is used by the PCI inverse assembler to decode PCI bus transactions. *It should not be changed or deleted from the format menu.* The signals that make up the STAT variable are listed in the following table. The STAT variable can be useful to set up SYMBOLS since it contains all of the key PCI control and status signals.

<b>STAT Variable</b>	<b>PCI Bus Signal Name</b>
Bit 24	TRDY#
Bit 23	FRAME#
Bit 22	IRDY#
Bit 21	UNUSED
Bit 20	UNUSED
Bit 19	REQ#
Bit 18	GNT#
Bit 17	IDSEL
Bit 16	UNUSED
Bit 15	UNUSED
Bit 14	UNUSED
Bit 13	UNUSED
Bit 12	UNUSED
Bit 11	INTA#
Bit 10	RESET#
Bit 9	C/BE3#
Bit 8	C/BE2#
Bit 7	C/BE1#
Bit 6	C/BE0#
Bit 5	DEVSEL#
Bit 4	STOP#
Bit 3	VDD
Bit 2	PERR#
Bit 1	SERR#
Bit 0	PAR

**The ADDR, ADDR\_B and DATA variables**

The ADDR variable is AD[31-0] bits of the PCI bus. The DATA variable is a dummy variable that needs to be defined for the PCI inverse assembler. *These variables should not be changed or deleted from the format Menu.*

**The CYCLE variable**

The CYCLE variable is made up of the following PCI signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL# and STOP#. This variable has 30 symbols defined that can be used to help make triggering, timing analysis and pattern filtering (16505A) easier. The following lists the bit pattern and the corresponding symbol.

Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP#
INTACK	1	0	1	0000	1	1
SPEC_CYC	1	0	1	0001	1	1
I/O_RD	1	0	1	0010	1	1
I/O_WR	1	0	1	0011	1	1
RESVRD	1	0	1	0100	1	1
RESVRD	1	0	1	0101	1	1
MEM_RD	1	0	1	0110	1	1
MEM_WR	1	0	1	0111	1	1
RESRVD	1	0	1	1000	1	1
RESRVD	1	0	1	1001	1	1
CON_RD	1	0	1	1010	1	1
CON_WR	1	0	1	1011	1	1
MEMRDM	1	0	1	1100	1	1
DAD_CY	1	0	1	1101	1	1
MEMRDL	1	0	1	1110	1	1
MEMWRI	1	0	1	1111	1	1
IO_XACTION	1	0	1	001X	1	1
MEM_XACTION	1	0	1	011X	1	1
CONFIG_XACTION	1	0	1	101X	1	1
ADD_CYCLE	1	0	1	XXXX	1	1
DATA_XFER	0	0	0	XXXX	0	1
WAIT_TARGET	1	X	0	XXXX	0	1
WAIT_INITIATOR	0	X	1	XXXX	0	1

DATA_FINALXFER	0	1	0	XXXX	0	1
STOP_NOXFER	X	0	1	XXXX	0	0
STOP_DATAXFER	0	X	0	XXXX	0	0
STOP_RETRY	1	1	0	XXXX	0	0
TARGET_ABORT	1	0	1	XXXX	1	0
IDLE	X	1	1	XXXX	X	X
WAIT_NODEVSEL	X	X	0	XXXX	1	1

# State Analysis

## Installation Quick Reference

This chapter explains how to configure the FS3030 to perform state analysis on the PCI Local Bus. The configuration software on the flexible diskette sets up the format specification menu of the logic analyzer for compatibility with the PCI Local Bus.

The following procedure describes the major steps required to perform measurements with the FS3030 module.

1. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe interface cable headers.
2. Install the FS3030 module into a slot in the target PCI Local bus.
3. Load the logic analyzer configuration file by loading the appropriate file from the Analysis Probe interface diskette.

## Acquiring Data

Touch RUN and, as soon as the PCI clock is active, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Slow or Missing Clock" when the PCI clock is not active.

## The State Display

Captured data is as shown in the following figure. The below figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

100/500MHz LA E

Listing 1

Print

Run

Markers  
Time

Trig to X  
0 s

Trig to 0  
0 s

X to 0  
0 s

Label>	PCI BUS TRANSACTIONS	Time	C/B3_0
Base>	REV 2.2	Relative	Hex
242	D32=xxxxxxx08	296 ns	E
243	I/O READ ADR=00000073	9.072 us	2
244	D32=23xxxxxxx	1.096 us	7
245	I/O WRITE ADR=00000020	10.97 us	3
246	D32=xxxxxxx20	168 ns	E
247	INTERRUPT ACK CYCLE	54.90 ms	0
248	D32=xxxxxxx08	296 ns	E
249	I/O READ ADR=00000073	9.904 us	2
250	D32=23xxxxxxx	1.128 us	7
251	I/O WRITE ADR=00000020	10.97 us	3
252	D32=xxxxxxx20	168 ns	E

## Error Messages

The following error messages are reported by the PCI inverse assembler.

### ERROR-NO DEVICE SELECTED

This error is displayed during a non special cycle data phase when IRDY and TRDY are asserted and DEVSEL is not asserted.

### ERROR DEVSEL ASSERTED

This error is displayed during a special cycle data phase if DEVSEL is asserted.

### SYSTEM ERROR

This error is displayed anytime SERR# is asserted.

## INVASM OPTIONS

**INVASM OPTIONS** is available with the following logic analyzers.

- 16505A Prototype Analyzer
- 16550A in an 16500B main frame
- 16540/541 in a 16500B main frame

INVASM OPTIONS can be invoked by selecting INVASM OPTIONS from the state listing display. The following selection will be displayed.

- I/O Reads
- I/O Writes
- Configuration Reads
- Configuration Writes
- Memory transactions (all memory transactions)
- IDLE cycles
- WAIT cycles
- All other transactions (this includes Interrupt Acknowledge and Special Cycle transactions)

The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the show/suppress button to the right of the transaction list.

## Loading the PC Mapper Software

The EIO PCI Analysis Probe PC Mapper software is an enhanced version of the EIO PCI Analysis Probe inverse assembler and is for use only with the EIO PCI Analysis Probe from FuturePlus Systems Corporation. The enhancement includes PCI I/O and memory address decode to indicate common PC access.

After the configuration file is loaded the PCI PC Mapper software can be loaded:

1. Install the PCI Analysis Probe software flexible diskette in the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the file IAPCIMPE.
3. Execute the load operation to load the file into the logic analyzer.

## The State Display with the PCI PC Mapper

Captured data is as shown in the following figure. The first figure displays the state listing after disassembly. The PCI PC Mapper is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

100/500MHz LA E	Listing 1	Invasm Options	Print	Run
Markers Time	Trig to X 0 s	Trig to 0 0 s	X to 0 0 s	

Label>	PCI BUS TRANSACTIONS	Time	C/B3_0
Base>	PC MAPPER PRE-RELEASE VERSION	Relative	Hex
39	RTC/CMOS RAM DATA PORT I/O WRITE ADR=00000071 REQ64 D32=xxxx00xx	2.960 us	3
40		1.168 us	D
41	VIDEO MEMORY MEM WRITE ADR=000B81E0 REQ64 D32=xxxxxx30	41.55 us	7
42		72 ns	E
43	VGA CRT CNTRLR ADDR REG I/O WRITE ADR=000003D4 REQ64 D32=xxxx000E	4.832 us	3
44		264 ns	C
45	VGA CRT CNTRLR ADDR REG I/O WRITE ADR=000003D4 REQ64 D32=xxxxF10F	440 ns	3
46		264 ns	C

The above display data using the PCI Inverse Assembly software without the PCI PC Mapper functionality. The display below is without the PC Mapper software.

100/500MHz LA E    Listing 1    Invasm Options    Print    Run

Markers Time    Trig to X 0 s    **Trig to 0 0 s**    X to 0 0 s

Label> Base>	PCI BUS TRANSACTIONS REV 2.2	Time	C/B3_0
		Relative	Hex
37	I/O WRITE ADR=00000070 REQ64#	1.200 us	3
38	D32=xxxxxx8F	1.072 us	E
39	I/O WRITE ADR=00000071 REQ64#	2.960 us	3
40	D32=xxxx00xx	1.168 us	D
41	MEM WRITE ADR=000B81E0 REQ64#	41.55 us	7
42	D32=xxxxxx30	72 ns	E
43	I/O WRITE ADR=000003D4 REQ64#	4.832 us	3
44	D32=xxxx000E	264 ns	C
45	I/O WRITE ADR=000003D4 REQ64#	440 ns	3
46	D32=xxxxF10F	264 ns	C
47	I/O WRITE ADR=00000070 REQ64#	4.064 us	3

## PC Mapper Error Messages

The error messages reported by the PCI PC Mapper are the same as those reported with the standard non mapper version of the PCI Inverse Assembler.

## PC Mapper INVASM OPTIONS

INVASM OPTIONS is available with the following logic analyzers.

- 16505A
- 1655x, 167x in a 16500B main frame
- 16540/541 in a 16500B main frame
- 166x series with 2.0 system software

INVASM OPTIONS can be invoked by selecting INVASM OPTIONS from the state listing display. The following selection will be displayed.

- I/O Reads
- I/O Writes
- Configuration Reads
- Configuration Writes
- Memory transactions (all memory transactions)
- IDLE cycles
- WAIT cycles
- All other transactions (this includes Interrupt Acknowledge and Special Cycle transactions)

## PCI PC Mapping for memory transactions

The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the show/suppress button to the right of the transaction cycle list.

This section lists the addresses, the commands and the corresponding mapping done by the PCI PC Mapper software. For information on the standard PCI configuration register mapping please refer to the PCI Local Bus Specification Rev 2.0.

Address bits 23-0	PC Mapper output
greater than 0FFFFFFH	System Memory
0FFFFFF-0E0000H	System BIOS
0DFFFF-0C0000H	ROM Scan
0BFFFF-0A0000H	Video Memory
09FFFF-000400H	System Memory
0003FF-000000H	See Interrupt Vector Table

## Interrupt Vector Table

Address bits 23-0	PC Mapper output
0003C4H	INT #F1-FF USER PROGRAMS
000200H	INT #80-F0 BASIC
0001E0H	INT #78-7F USER PROGRAMS
0001DCH	INT #77 IRQ15
0001D8H	INT #76 IRQ14
0001D4H	INT #75 IRQ13
0001D0H	INT #74 IRQ12
0001CCH	INT #73 IRQ11
0001C8H	INT #72 IRQ10
0001C4H	INT #71 IRQ9
0001C0H	INT #70 IRQ8
0001A0H	INT #68-6F RESERVED
00019CH	INT #67 EXP MEM MANG
000180H	INT #60-66 USER PROGRAMS
00012CH	INT #4B-5F RESERVED
000128H	INT #4A USER RTC ALARM
00011CH	INT #47-49 RESERVED
000118H	INT #46 HD DISK #1 PARAM
000110H	INT #44-45 RESERVED
00010CH	INT #43 VIDEO CHAR TABLE
000108H	INT #42 EGA BIOS
000104H	INT #41 HD DISK #0 PARAM
000100H	INT #40 FLOPPY DISK ISR
000080H	INT #20-3F RESERVED DOS
00007CH	INT #1F VIDEO CHAR TABLE
000078H	INT #1E FLOPPY PARAMS
000074H	INT #1D AVAILABLE
000070H	INT #1C AVAILABLE
00006CH	INT #1B KEYBOARD BREAK
000068H	INT #1A RTC ISR
000064H	INT #19 BOOSTRAP LOADER
000060H	INT #18 ROM BASIC
00005CH	INT #17 LPT PRINTER BIOS
000058H	INT #16 KEYBOARD BIOS
000054H	INT #15 SYS SERVICE BIOS
000050H	INT #14 SERIAL PORT BIOS
00004CH	INT #13 FLOPPY DISK BIOS
000048H	INT #12 MEM SIZE INT
000044H	INT #11 EQUIP LIST
000040H	INT #10 VIDEO BIOS
00003CH	INT #0F IRQ7 LPT1
000038H	INT #0E IRQ6 FLOPPY DISK
000034H	INT #0D IRQ5 LPT2
000030H	INT #0C IRQ4 SERIAL #1
00002CH	INT #0B IRQ3 SERIAL #2
000028H	INT #0A IRQ2 SLAVE INT
000024H	INT #09 KEYBOARD
000020H	INT #08 IRQ0 SYS TIMER
00001CH	INT #07 NUM COPROCESSOR
000018H	INT #06 INVALID OPCODE
000014H	INT #05 PRINT SCREEN
000010H	INT #04 OVERFLOW DETECT
00000CH	INT #03 BREAKPOINT TRACE

<b>Address bits 23-0</b>	<b>PC Mapper output</b>
000008H	INT #02 NMI
000004H	INT #01 SINGLE STEP
000000H	INT #00 DIVIDE BY ZERO

## PCI PC Mapping - I/O Transactions

Address bits 23-0	PC Mapper output
0000H	MSTR DMA CH 0
0001H	MSTR DMA CH 0
0002H	MSTR DMA CH 1
0003H	MSTR DMA CH 1
0004H	MSTR DMA CH 2
0005H	MSTR DMA CH 2
0006H	MSTR DMA CH 3
0007H	MSTR DMA CH 3
0008H	MSTR DMA STAT REG
0009H	UNKNOWN IO DEVICE
000AH	MSTR DMA MASK REG
000BH	MSTR DMA MODE REG
000CH	MSTR DMA CLR BYTE PTR
000DH	MSTR DMA MSTR CLEAR
000EH	MSTR DMA CLEAR MASK
000FH	MSTR DMA WRT MASK
0018H	MSTR DMA CH EXT FUNCT REG
001AH	MSTR DMA EXT FUNCT
0020H	MSTR INT REQ REG
0021H	MSTR INT REQ REG2
0040H	INTERVAL TIMER TIMER 0
0042H	INTERVAL TIMER SPKR TIMER
0043H	INTRVAL TIMER #1 CNTRL
0044H	INTERVL TIMER #2 WATCHDOG
0047H	INTERVAL TIMER #2 CNTRL
0060H	KEYBOARD/MOUSE DATA PORT
0061H	SYSTEM CONTOL PORT B
0064H	KEYBOARD/MOUSE CMD PORT
0070H	RTC/CMOS RAM ADDR PORT
0071H	RTC/CMOS RAM DATA PORT
0074H	EXT CMOS RAM ADDR PORT
0075H	EXT CMOS RAM ADDR PORT
0076H	EXT CMOS RAM DATA PORT
0081H	CH 2 DMA PAGE REGISTER
0082H	CH 3 DMA PAGE REGISTER
0083H	CH 1 DMA PAGE REGISTER
0087H	CH 0 DMA PAGE REGISTER
0089H	CH 6 DMA PAGE REGISTER
008AH	CH 7 DMA PAGE REGISTER
008BH	CH 5 DMA PAGE REGISTER
008FH	CH 4 DMA PAGE REGISTER
0090H	ARB CNTRL POINT REG
0091H	FEEDBACK REG
0092H	SYSTEM CONTROL PORT A
0094H	SYS SETUP/CARD ENABLE REG
0096H	ADAPTOR SETUP/ENABLE REG
00A0H	SLAVE INTERRUPT CNTRLR
00A1H	SLAVE INTERRUPT CNTRLR
00C0H	SLAVE DMA CH4 MEM ADDR
00C2H	SLAVE DMA CH4 TRANS COUNT
00C4H	SLAVE DMA CH5 MEM ADDR
00C6H	SLAVE DMA CH5 TRANS COUNT
00C8H	SLAVE DMA CH6 MEM ADDR

<b>Address bits 23-0</b>	<b>PC Mapper output</b>
00CAH	SLV DMA CH6 TRANS COUNT
00CCH	SLAVE DMA CH7 MEM ADDR
00CEH	SLAVE DMA CH7 TRANS COUNT
00D0H	SLV DMA STATUS REG CH 4-7
00D4H	SLV DMA MASK REG CH 4-7
00D6H	SLAVE DMA MODE REG CH 4-7
00D8H	SLAVE DMA CLEAR BYTE PNTR
00DAH	SLAVE DMA MASTER CLEAR
00DCH	SLV DMA CLR MASK CH 4-7
00DEH	SLAVE DMA WRITE MASK REG
00E0H	IBM MODELS - ENCODE REG
00E1H	IBM MODELS - ENCODE REG
00F1H	NUMERIC COPROCESSOR RESET
00F8H	NUMERIC COPROCESSOR PORT
00F9H	NUMERIC COPROCESSOR PORT
00FAH	NUMERIC COPROCESSOR PORT
00FBH	NUMERIC COPROCESSOR PORT
00FCH	NUMERIC COPROCESSOR PORT
0100H	ADAPTER CARD POS REG 0
0101H	ADAPTER CARD POS REG 1
0102H	SYS BD/ADP CD POS REG 2
0103H	SYS BD/ADP CD POS REG 3
0104H	ADAPTER CARD POS REG 4
0105H	ADAPTER CARD POS REG 5
0106H	ADAPTER CARD POS REG 6
0107H	ADAPTER CARD POS REG 6
0278H	PARALLEL PORT 3 DATA PORT
0279H	PARALLEL PORT 3 STAT PORT
027AH	PARALLEL PORT 3 CMD PORT
02F8H	SERIAL PORT 2 XMIT/REC
02F9H	SER PORT 2 DIV LATCH/INT
02FAH	SERIAL PORT 2 INT ID REG
02FBH	SERIAL PORT 2 CNTRL REG
02FDH	SERIAL PORT 2 MODEM CNTRL
02FEH	SERIAL PORT 2 MODEM STAT
02FFH	SERIAL PORT 2 SCRTCH REG
0378H	PARALLEL PORT 2 DATA PORT
0379H	PARALLEL PORT 2 STAT PORT
037AH	PARALLEL PORT 2 CMD PORT
03B4H	VGA CRT CNTRLR ADDR REG
03B5H	VGA CRT CNTRLR DATA REG
03BAH	VGA STAT 1/FEATURE CNTRL
03BCH	PARALLEL PORT 1 DATA PORT
03BDH	PARALLEL PORT 1 STAT PORT
03BEH	PARALLEL PORT 1 CMD PORT
03C0H	VGA ATTRIBUTE CNTRLR ADDR
03C1H	VGA ATTRIBUTE CNTRLR DATA
03C2H	VGA OUTPUT/STAT REG
03C3H	VGA VIDEO SUBSYSTEM ENABLE
03C4H	VGA SEQUENCER ADDR REG
03C5H	VGA SEQUENCER DATA REG
03C6H	VIDEO DAC PEL MASK
03C7H	VIDEO DAC PAL ADDR/STAT

<b>Address bits 23-0</b>	<b>PC Mapper output</b>
03C8H	VIDEO DAC PAL ADDR/WRITE
03C9H	VIDEO DAC PALETTE DATA
03CAH	VGA FEATURE CONTROL REG
03CCH	VGA MISC OUTPUT REG
03CEH	VGA GRAPHICS CNTRLR ADDR
03CFH	VGA GRAPHICS CNTRLR ADDR
03D4H	VGA CRT CNTRLR ADDR REG
03D5H	VGA GRAPHICS CNTRLR DATA
03DAH	VGA COLOR STAT 1/FEATURE
03F0H	FLOPPY STATUS REG A
03F1H	FLOPPY STATUS REG B
03F2H	FLOPPY DIGITAL OUTPUT REG
03F4H	FLOPPY DISK CNTRLR STAT
03F5H	FLOPPY DISK CNTRLR DATA
03F7H	FLOPPY CONFIG CONTROL REG
03F8H	SERIAL PORT 1 XMIT/RCV BUF
03F9H	SER PORT 1 DIV LATCH/INT
03FAH	SERIAL PORT 1 INT ID/FIFO
03FBH	SERIAL PORT 1 LINE CNTRL
03FCH	SERIAL PORT 1 MODEM CNTRL
03FDH	SERIAL PORT 1 STAT REG
03FEH	SERIAL PORT 1 MODEM STAT
03FFH	SERIAL PORT 1 SCRATCH REG
0680H	MANUFACTURING CHECKPOINT PORT

# Timing Analysis

## Installation Quick Reference

Since the FS3030 EIO interface contains no active logic, it introduces negligible skew to the PCI Local Bus signals.

The following procedure describes the major steps required to perform timing analysis measurements with the FS3030 module.

1. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe cable headers
2. Install the FS3030 module into a slot in the target PCI Local bus.
3. Load the logic analyzer configuration file by loading the appropriate file from the Analysis Probe interface diskette.

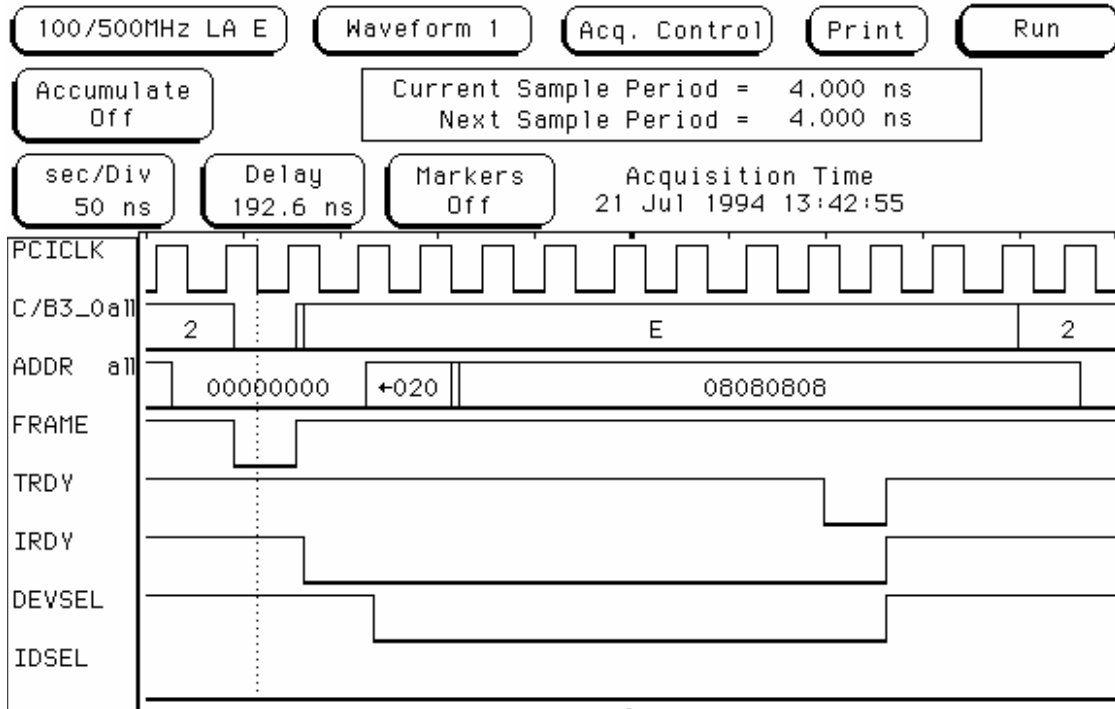
## Acquiring Data

Touch RUN and the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Waiting for Trigger" if the trigger specification has not been met.

# The Waveform Display

Captured data is displayed as shown in the following figure.



# General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS3030 module.

## Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS3030 module.

### ***Analysis Probe Interface Compatibility***

32 bit EIO PCI card per the EIO Specification rev. 1.42.

### ***JTAG Boundary Scan***

The FS3030 does not implement JTAG Boundary SCAN.

### ***Standards Supported***

The EIO Specification Revision 1.42.

### ***Power Requirements***

The FS3030 Analysis Probe logic contains no active components and therefore requires no power.

### ***Logic Analyzer Required***

1655x, 166x, 167x.

### ***Number of Probes Used***

32 bit PCI Local Bus - 4 cable headers.

### ***Minimum Clock Period (State)***

Not limited by the Analysis Probe interface logic. Clocking is specified by the logic analyzer. Therefore both 33Mhz and 66Mhz are supported.

### ***Signal loading***

When attached the logic analyzer presents approximately a 10pf load. The add-in card presents an additional load.

### ***Etch length***

The etch length from the gold finger card edge to the pad of the extender card edge connector is approximately 4 inches on all signals. The signals are all daisy chained from the connector to the mictor connectors and then up to the extender card connector.

### ***Environmental Temperature***

Operating: 0 to 55 degrees C (+32 to +131 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

### ***Altitude***

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

***Humidity***

Up to 90% non condensing. Avoid sudden, extreme temperature changes which would cause condensation on the FS3030 module.

***Testing and Troubleshooting***

There are no automatic performance tests or adjustments for the FS3030 module. If a failure is suspected in the FS3030 module contact the factory or your FuturePlus Systems authorized distributor.

***Servicing***

The repair strategy for the FS3030 is module replacement. However, if parts of the FS3030 module are damaged or lost contact the factory for a list of replacement parts.

## Signal Connections

The FS3030 module monitors signals for both state and timing analysis. The below figure displays how the cable headers are numbered. The following tables list the FS3030 cable headers and the corresponding PCI Local Bus signals after these signals have been terminated by the 90K ohm/10pf terminators.

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 1 pin 3	CLK/16	User15
5	no connect	
7	15	AD15
9	14	AD14
11	13	AD13
13	12	AD12
15	11	AD11
17	10	AD10
19	9	AD09
21	8	AD08
23	7	AD07
25	6	AD06
27	5	AD05
29	4	AD04
31	3	AD03
33	2	AD02
35	1	AD01
37	0	AD00

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 2 pin 3	CLK/16	User16
5	no connect	
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 3 pin 3	CLK/16	PCI Clock
5	no connect	
7	15	USER4
9	14	USER3
11	13	USER2
13	12	USER1
15	11	INTA#
17	10	RST#
19	9	C/BE3#
21	8	C/BE2#
23	7	C/BE1#
25	6	C/BE0#
27	5	DEVSEL#
29	4	STOP#
31	3	VDD (note: this is done for software compatibility purposes)
33	2	PERR#
35	1	SERR#
37	0	PAR

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 4 pin 3	CLK/16	USER17
5	no connect	
7	15	USER14
9	14	USER13
11	13	USER12
13	12	USER11
15	11	USER10
17	10	USER9
19	9	TRDY#
21	8	FRAME#
23	7	IRDY#
25	6	USER8
27	5	USER7
29	4	REQ#
31	3	GNT#
33	2	IDSEL
35	1	USER6
37	0	USER5