



CompactPCI[®]

CompactPCI Analysis Probe FS3020

Users Manual

For Agilent Logic Analyzers

Revision 2.2

FuturePlus is a registered trademark of FuturePlus Systems Corporation

Copyright 2004 FuturePlus Systems Corporation

HOW TO REACH US	5
PRODUCT WARRANTY	6
Limitation of warranty	6
Exclusive Remedies	6
Assistance	6
INTRODUCTION	7
How to Use This Manual	7
ANALYZING THE COMPACTPCI LOCAL BUS	8
Duplicating the 167xx Logic Analyzer Master Diskette	8
Accessories Supplied	8
Minimum Equipment Required	9
Signal Naming Conventions	9
The Jumpers- JMP2-JMP5	9
Connecting the Jumpers	9
Connecting to the CompactPCI Analysis Probe	9
Installing the CompactPCI Analysis Probe	10
How to install a CompactPCI add-in card into the FS3020	11
Operation of the CompactPCI card in the extender card connector	11
System Slot Operation	11
Setting up the Analyzers installed in the 16500 mainframes and the portables	11
Setting up the Analyzers installed in the 167xx mainframe	12
Setting up the 1680/90/900 Analyzer	12
1680/90/900 Licensing	13
Loading 1680/90/900 configuration files and the General Purpose Probe feature	13
Configuration Files	14
Offline Analysis	14
The Format Menu	17
POD 7 Signals	18

Location of POD 7 jumpers	19
Optional signals for POD 7 (<i>wire wrap</i>)	20
Location of optional signals	21
The STAT variable	21
The ADDR, ADDR_B and DATA variables	22
The CYCLE variable	22
STATE ANALYSIS	25
Installation Quick Reference	25
Acquiring Data	25
The State Display	28
Error Messages	31
INVASM OPTIONS	33
Using the PC Mapper Inverse Assembler	35
Setting up the Analyzer from the diskette	35
Acquiring Data	36
The State Display with the CompactPCI PC Mapper	36
PCI PC Mapping for memory transactions	38
Interrupt Vector Table	39
CompactPCI PC Mapping - I/O Transactions	41
TIMING ANALYSIS	44
Installation Quick Reference	44
Acquiring Data	44
The Waveform Display	45
GENERAL INFORMATION	46
Characteristics	46
3.3V and 5.0V Analysis Probe Interface Compatibility	46
JTAG Boundary Scan	46
Standards Supported	46
Power Requirements	46
Logic Analyzer Required	46
Number of Probes Used	46
Minimum Clock Period (State)	46
Signal loading	46
Etch length	47
Operations	47
Environmental Temperature	47

Altitude	47
Humidity	47
Testing and Troubleshooting	47
Servicing	47
Signal Connections	48
Test Points	56

How to reach us

For Technical Support:

FuturePlus Systems Corporation

36 Olde English Road

Bedford NH 03110

TEL: 603-471-2734

FAX: 603-471-2738

On the web <http://www.futureplus.com>

For Sales and Marketing Support:

FuturePlus Systems Corporation

TEL: 719-278-3540

FAX: 719-278-9586

On the web <http://www.futureplus.com>

FuturePlus Systems has technical sales representatives in several major countries. For an up to date listing please see <http://www.futureplus.com/contact.html>.

Agilent Technologies is also an authorized reseller of many FuturePlus products. Contact any Agilent Technologies sales office for details.

Product Warranty

This FuturePlus Systems product has a warranty against defects in material and workmanship for a period of 1 year from the date of shipment. During the warranty period, FuturePlus Systems will, at its option, either replace or repair products proven to be defective. For warranty service or repair, this product must be returned to the factory.

For products returned to FuturePlus Systems for warranty service, the Buyer shall prepay shipping charges to FuturePlus Systems and FuturePlus Systems shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to FuturePlus Systems from another country.

FuturePlus Systems warrants that its software and hardware designated by FuturePlus Systems for use with an instrument will execute its programming instructions when properly installed on that instrument. FuturePlus Systems does not warrant that the operation of the hardware or software will be uninterrupted or error-free.

Limitation of warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. FUTUREPLUS SYSTEMS SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Exclusive Remedies

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. FUTUREPLUS SYSTEMS SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

Assistance

Product maintenance agreements and other customer assistance agreements are available for FuturePlus Systems products. For assistance, contact the factory.

Introduction

The CompactPCI Analysis Probe module provides a complete interface between any CompactPCI add-in slot and Agilent Logic Analyzers. The Analysis Probe interface connects the signals from the CompactPCI Local bus to the logic analyzer inputs.

The CompactPCI Analysis Probe is a passive bus monitor which does not assert any signals on the CompactPCI bus. The CompactPCI bus signals are terminated with 90k ohm/10pf terminators so that they are matched to the logic analyzer.

The configuration software on the diskette sets up the format specification menu of the logic analyzer for compatibility with your CompactPCI bus. When the state configuration file is loaded, an inverse assembler is also loaded which decodes CompactPCI transactions into easy to read mnemonics.

This manual is organized to help you quickly find the information you need.

How to Use This Manual

- **Analyzing the CompactPCI Local Bus** chapter introduces you to the CompactPCI Analysis Probe and lists the minimum equipment required and accessories supplied for CompactPCI bus analysis.
- The **State Analysis** chapter explains how to configure the CompactPCI Analysis Probe to perform state analysis on your CompactPCI bus.
- The **Timing Analysis** chapter explains how to configure the CompactPCI Analysis Probe to perform timing analysis on your CompactPCI bus.
- The **General Information** chapter provides some general information including the operating characteristics for the CompactPCI Analysis Probe module and the cable header pinout.

Analyzing the CompactPCI Local Bus

This chapter introduces you to the CompactPCI Analysis Probe and lists the minimum equipment required and accessories supplied for CompactPCI Local Bus analysis. This chapter also contains information that is common to both state and timing analysis.

Duplicating the 167xx Logic Analyzer Master Diskette

Before you use the CompactPCI Analysis Probe software, make a duplicate copy of the master diskette. Then store the master diskette and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the diskette wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate diskette operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Accessories Supplied

The CompactPCI Analysis Probe product consists of the following accessories:

- The Analysis Probe interface hardware, which includes the interface circuit module.
- Several jumpers which come installed on the circuit module.
 - Four that control the logic analyzer clocking
 - One for passing the TDO/TDI JTAG signals
 - 16 for jumpering directly to POD 7
- The inverse assembly and configuration software on two 3.5 inch diskettes.

- This operating manual on CD.
- CD containing setup file to install configuration files and decoder on a 1680/90/900 analyzer or for use as an offline viewer.

Minimum Equipment Required

The minimum equipment required for analysis of a CompactPCI Local Bus consists of the following equipment:

- An 1650B, 166x, 167x, 16550A, 16555, 16510B Logic Analyzer. The diskette labeled “CompactPCI Analysis Probe Software for the FS3020” supports the above listed analyzers.
- 16600/167xx Analyzers. The diskette labeled “16600/16700 Analysis Probe Install Disk for the FS3020” supports the 16600/167xx analyzers.
- 1680/90 Analyzers. The diskette labeled “1680/1690 Analysis Probe Install Disk for the FS3020” supports the 1680/90 analyzers.
- The CompactPCI Analysis Probe Product
- A CompactPCI target bus

Signal Naming Conventions

This operating manual uses the same signal notation as the PCI LOCAL BUS SPECIFICATION - REVISION 2.1. That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

Connecting the Jumpers

There are four jumpers JP2, JP3, JP4 and JP5 that are configured on the CompactPCI Analysis Probe for clocking purposes. These jumpers are used to configure the master clock used for state analysis and for compatibility for use with older logic analyzers.

The Jumpers- JMP2- JMP5

For 166x, 167x, 16550A, 167xx, 1680/90 logic analyzers jumpers JMP2, 3, 4 and 5 must be connected between pins 2 and 3. For 1650B and 16510B logic analyzers JMP2, 3, 4 and 5 must be connected between pins 1 and 2.

Logic Analyzer	JMP 2, 3, 4 and 5
166x, 167x, 1655x, 167xx, 1680/90 State OR Timing analysis	Connect pins 2 and 3
1650B, 16510B Timing analysis	Connect pins 1 and 2
1650B, 16510B State analysis	Connect pins 2 and 3

Connecting to the CompactPCI Analysis Probe

The following explains how to connect the logic analyzer to the CompactPCI Analysis Probe for either state or timing analysis:

1. Remove the probe tip assemblies from the logic analyzer cables.

2. Plug the logic analyzer cables into the CompactPCI Analysis Probe cable headers as shown in the appropriate following tables.

For logic analyzers : 16510, 165x, 166x, 167x, 1680/90 series and the 16550.

Logic Analyzer	CompactPCI Analysis Probe	Comment
Master POD 1	Header 1	
POD 2	Header 2	
POD 3	Header 3	L clock
POD 4	Header 4	
POD 5	Header 5	64 bit
POD 6	Header 6	64 bit
POD 7	Header 7	optional signals

For logic analyzers 16554/5/6/7, 16715/7/9, 16750/51/52

Logic Analyzer	CompactPCI Analysis Probe	Comment
Master POD 1	Header 1	
Master POD 2	Header 2	
Master POD 3	Header 3	L clock
Master POD 4	Header 4	
Expander POD 1	Header 1	64 bit
Expander POD 2	Header 2	64 bit
Expander POD 3		optional signals

Installing the CompactPCI Analysis Probe

The CompactPCI Analysis Probe can be installed in any slot of the CompactPCI Local bus. The following steps explain how to install the CompactPCI Analysis Probe into the CompactPCI Local bus.

1. Install the logic analyzer cables as described in the previous section.
2. Align the CompactPCI module with the appropriate slot on the target system and plug the module into the CompactPCI connector.

How to install a CompactPCI add-in card into the FS3020

The extender card connector of the FS3020 module can accommodate one CompactPCI add in card. Simply align the module with the connector and gently push the module in until it is seated in the connector. The FS3020/PCI add-in card combination can then be installed in any slot of the CompactPCI Local bus. For mechanical stability the add-in card in the extender card connector should be mechanically supported.

When removing the CompactPCI add-in card from the card edge extender connector grasp the FS3020 with one hand and the PCI add-in card with the other. Gently rock the CompactPCI add-in card until it is free from the connector.

Operation of the CompactPCI card in the extender card connector

The nature of an extender card is that it extends the etch length of the bus. Due to the sensitivity of most PCI designs, extending the etch length can interfere with the PCI add-in card operation. Operation of the PCI add-in card when installed in the extender card connector is not guaranteed. Please check your system design if you experience failures due to poor signal fidelity.

System Slot Operation

The FS3020 was designed to operate in the system slot with the CPU board in the extender card connector. In this configuration all the clocks, request and grant signals can be observed.

Setting up the Analyzers installed in the 16500 mainframes and the portables

The logic analyzer can be configured for CompactPCI analysis by loading the CompactPCI configuration file. Loading this file will load the CompactPCI Local bus inverse assembler and configure your logic analyzer. To load the configuration and inverse assembler:

1. Install the CompactPCI Analysis Probe software flexible diskette in the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the appropriate configuration file (see table below).
3. Execute the load operation to load the file into the logic analyzer.

Logic Analyzer	No. of PODS	File name for state Analysis	File name for Timing Analysis	Comment
16555/6/7, 167x	4	F555CPCI	F555CPCI	32 bit analysis
16555/6/7 (requires 2 16555 cards), 167x	7	F555CP64	F555CP64	64 bit analysis with system slot signals
16555/6/7 (requires 2 16555 cards), 167x	5	F555C32S	F555C32S	32 bit analysis with system slot signals
166x	7	F660CPCI	F660CPCI	64 bit analysis with system slot signals
166x	5	F660C32S	F660C32S	32 bit analysis with system slot signals

Logic Analyzer	No. of PODS	File name for state Analysis	File name for Timing Analysis	Comment
16550A	7	F550CPCI	F550CPCI	64 bit analysis with system slot signals
16550A	5	F550C32S	F550C32S	32 bit analysis with system slot signals
1650B and 1651B	4	F510CPCIS	F510CPCIT	32 bit analysis no system slot

Setting up the Analyzers installed in the 167xx mainframe

Please note that 166x, 167x and 1655x users do not need to reload any files from the diskette when switching between state and timing analysis.

For 16500B mainframe users 1655x and 166x, 167x REV 2.0 (system software) users an enhanced inverse assembler is included on the Analysis Probe software diskette. After loading the above file. Load the file IAPCIE . This will configure the STATE Listing menu to include INVASM OPTIONS.

The 16700 requires a special install procedure to install the PCI Inverse Assembler. To accomplish this, insert the diskette labeled 16600/16700 Analysis Probe Install Disk for the FS3020 into the 16600/700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL* .

This procedure does not need to be repeated. It only needs to be done the first time the CompactPCI Probe Adapter is used.

When this has completed, load the appropriate configuration file from the /configs/FuturePlus/FS3020 directory. Refer to the table on the following pages for a list of analyzers and corresponding configuration files.

Setting up the 1680/90/900 Analyzer

The 1680/90/900 Analyzer is a PC based application that requires a PC running the Windows OS with the Agilent logic analyzer software installed or a 16900 frame.

Before installing the protocol decoder for the PCI protocol on a PC you **must** install the Agilent logic analyzer software. Once the Agilent logic analyzer software is installed, you can install the FS3020 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the .exe file on the CD-ROM disk and then double click the .exe file name from within the File Explorer navigation panel.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe Adapter is used.

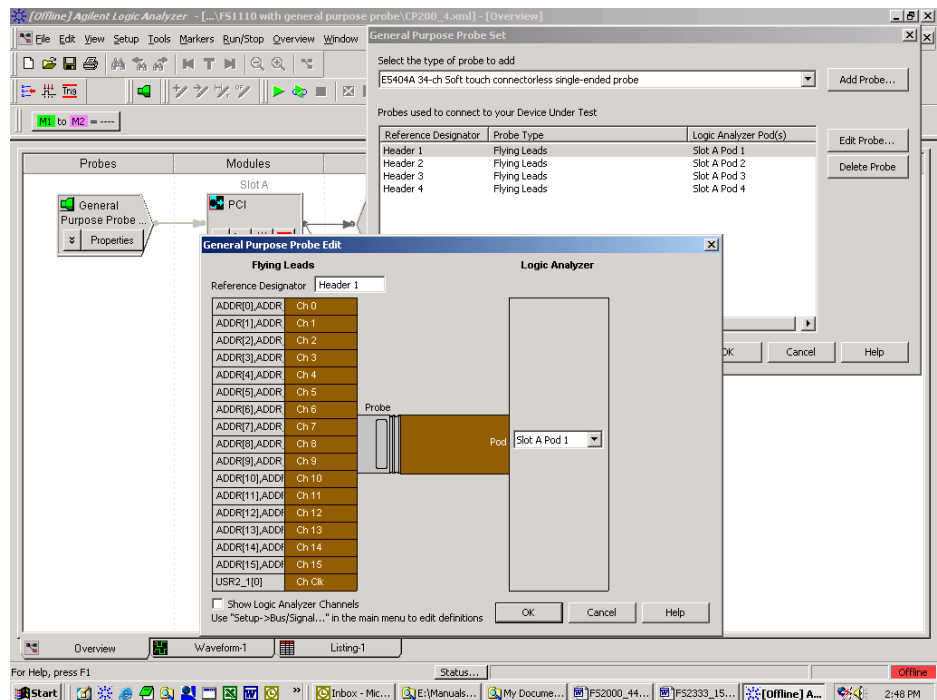
1680/90/900 Licensing

The PCI Inverse Assembler is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

Loading 1680/90/900 configuration files and the General Purpose Probe feature

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

Once you have loaded a configuration file on the 169xx machine you can find out how to attach the logic analyzer cables to the probe by going to the workspace and selecting Properties on the General Purpose Probe tool icon that appears before the logic analyzer icon. Once you click on the Properties box a new window will appear showing which analyzer pod attaches to each probe cable.



Refer to the table below for a list of analyzers and corresponding configuration files.

Configuration Files

167xx Analyzer	169xx Analyzer	No. of PODS	File name for state/timing analysis	Comment
16715/6/7/9 16750/1/2		7	CP302_1	64 bit analysis with system slot signals
16715/6/7/9 16750/1/2		5	CP302_2	32 bit analysis with system slot signals
16715/6/7/9 16750/1/2		4	CP302_3	32 bit analysis w/out system slot signals
16550A		5	CP302_4	32 bit analysis with system slot signals
16555, 167x		4	CP302_5	32 bit analysis w/out system slot signals
16555/6/7 (requires 2 16555 cards), 167x		5	CP302_6	32 bit analysis with system slot signals
16555/6/7 (requires 2 16555 cards), 167x		7	CP302_7	64 bit analysis with system slot signals
16550A		7	CP302_8	64 bit analysis with system slot signals
	1680/90, 16750/1/2, 1691x	7	CP302_9	64 bit analysis with system slot signals
	1680/90, 16750/1/2, 1691x	5	CP302_10	32 bit analysis with system slot signals

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

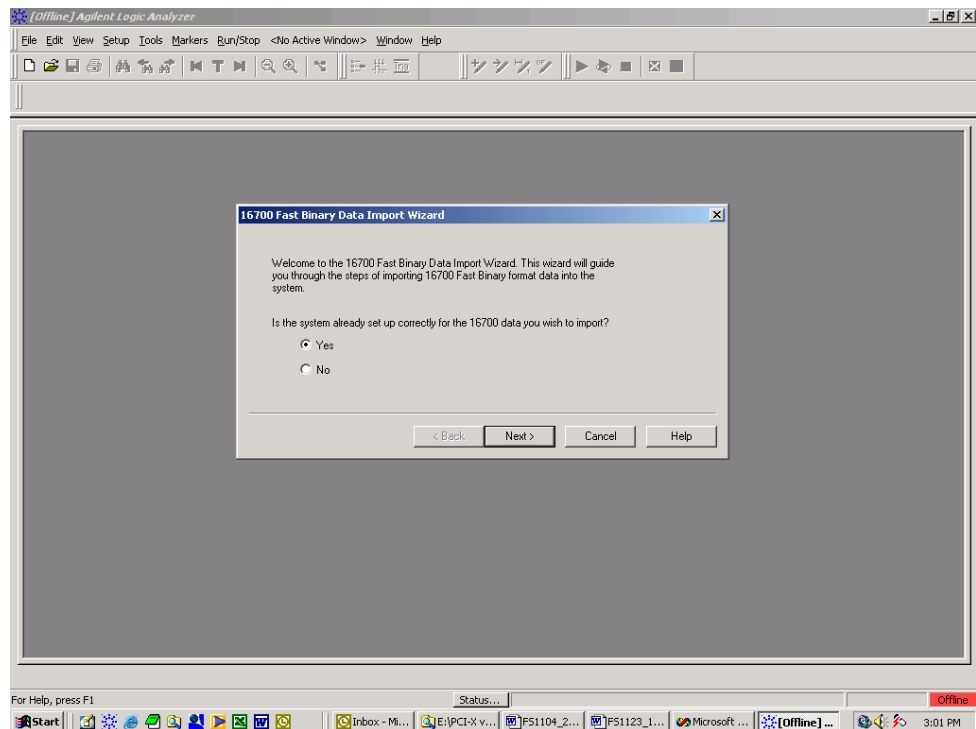
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may buy additional licenses, please contact FuturePlus sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for “Setting up 1680/90/900 analyzer”. Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

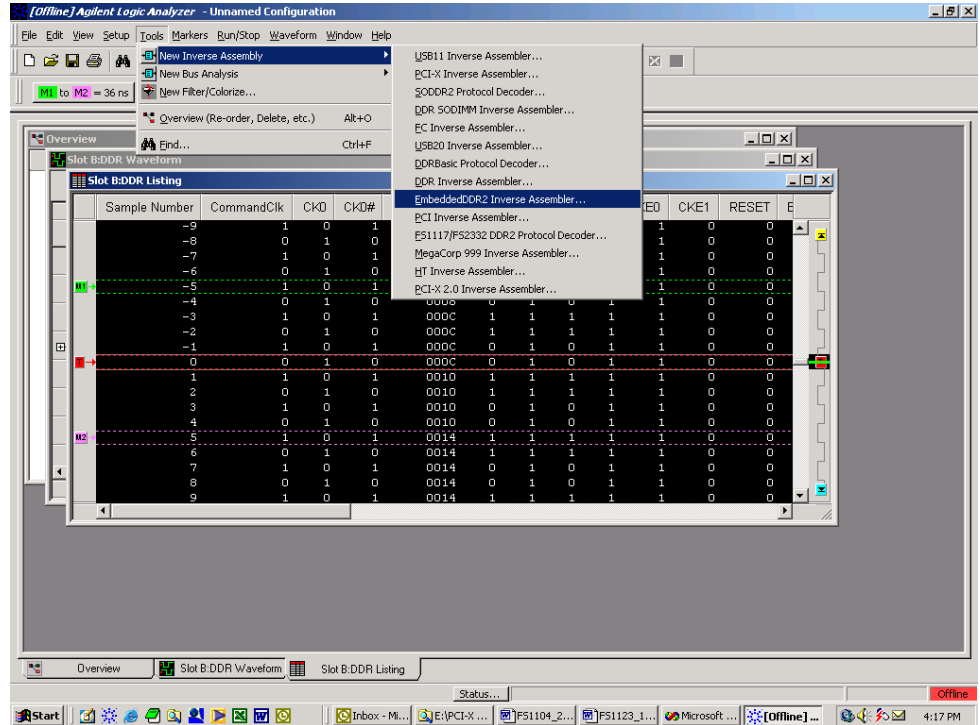
For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select “yes” when it asks if the system is ready to import 16700 data.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.



After the decoder has loaded, select Preferences if required, from the overview screen and set the preferences to their correct value in order to decode the trace properly. This is a general requirement, some decoders do not have preferences, if this is the case then no preference setting is necessary.

The Format Menu

The CompactPCI Analysis Probe diskette sets up the format menu as shown in the following table. This format is the same for both Timing and State Analysis.

The 16510 Format will differ slightly. The STAT variable will be channels 11-0 on POD 4 and channels 14-0 on POD 3. In addition, the 16510 is only capable of 32 bit analysis due to having less than 6 PODS.

Label	Clk Inputs	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
STAT	M,K,J				8-0	14-0		
ADDR							15-0	15-0
ADDR_B			15-0	15-0				
USER7_1					15-9			
INTD_A						14-11		
RESET						10		
C/B7_0						9-6		
DATA							15-0	15-0
DEVSEL						5		
STOP						4		
LOCK						3		
PERR						2		
SERR						1		
PAR						0		
SD/SB0					8-7			
PAR64					2			
ACK/RQ					1-0			
IRDY	J				9			
FRAME	K				10			
TRDY	M				11			
PCICLK	L							
CLK3	N							
Optional POD 7 signals		15-0						

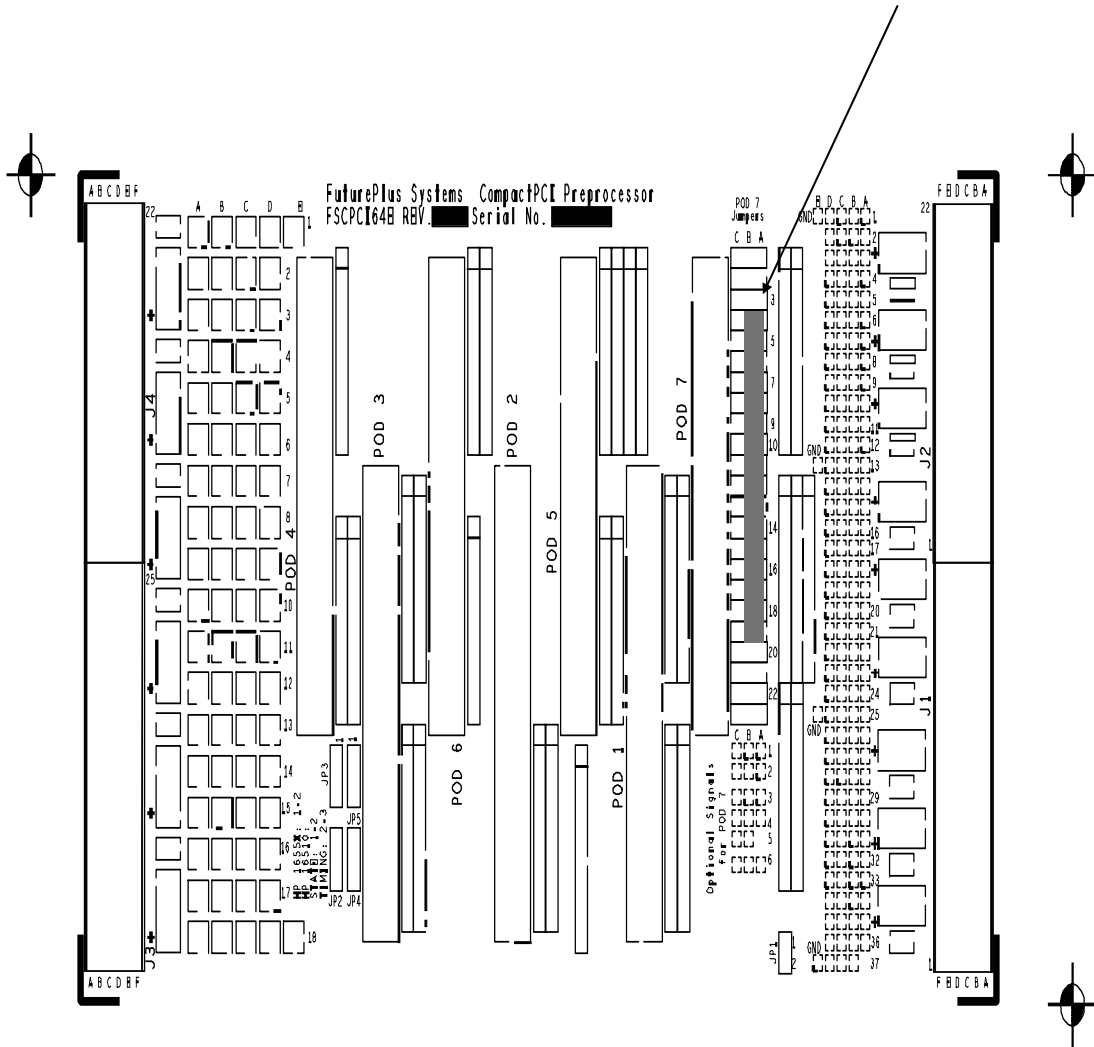
POD 7 Signals

POD 7 can be used to view the reserved, request, grant, clock and other miscellaneous signals that are only available on the system slot. A list of the signals that can be directly jumpered to POD 7 are listed below.

Logic Analyzer channel number	POD 7 jumper	CompactPCI Signal name jumper selectable position 1(C-B)/ position 2(B-A)
CLK/16		CLK3
no connect		
15	19	CLK4/FAL#
14	18	PRST#/DEG#
13	17	INTP/ BRSVJ1A4
12	16	INTS/ BRSVJ1A5
11	15	REQ1#/ BRSVJ1B5
10	14	GNT1#/ BRSVJ1C25
9	13	REQ2#/ BRSVJ2B4
8	12	GNT2#/ BRSVJ2A15
7	11	REQ3#/ BRSVJ2A16
6	10	GNT3#/ BRSVJ2A17
5	9	REQ4#/ BRSVJ2B16
4	8	GNT4#/ BRSVJ2E16
3	7	REQ5#/ BRSVJ2A18
2	6	GNT5#/ BRSVJ2B18
1	5	REQ6#/ BRSVJ2C18
0	4	GNT6#/ BRSVJ2E18

Location of POD 7 jumpers

These jumpers start at location 4 and go to location 19 as shown in the drawing below



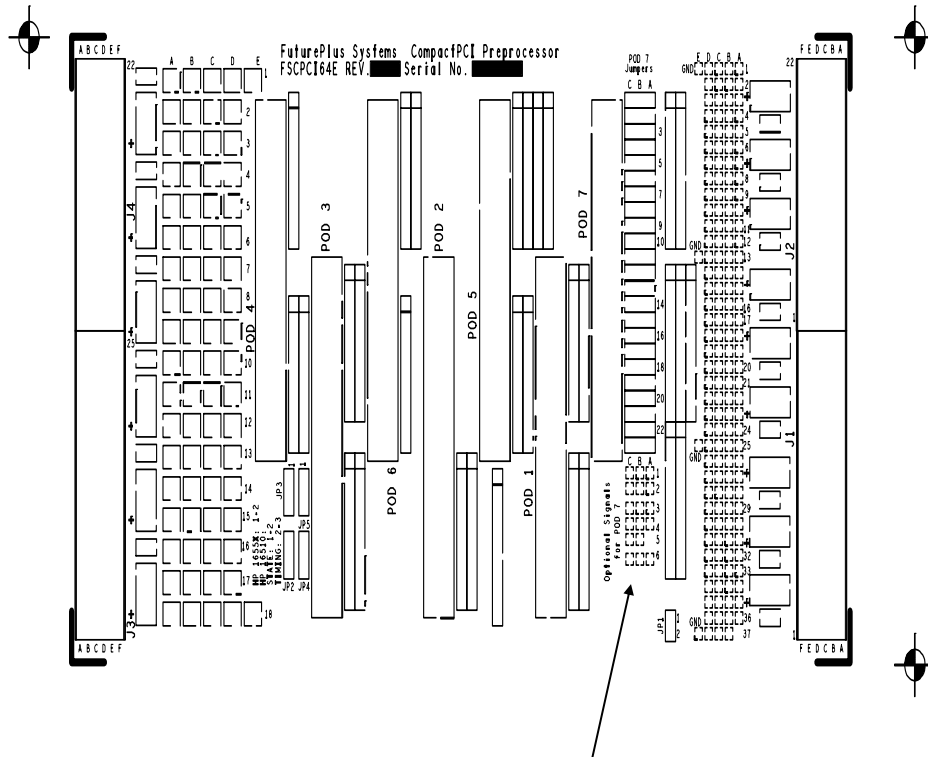
Optional signals for POD 7 (*wire wrap*)

The below listed signals are terminated for compatibility to the logic analyzer but must be connected via wire wrap to pin 2 of the POD 7 connectors 4-19.

Optional signals for POD 7 Location	CompactPCI Signal name
C5	RSVJ2A19
C3	RSVJ2A20
C3	RSVJ2A21
C4	RSVJ2A22
A3	RSVJ2B20
B5	RSVJ2B22
POD7.C1*	RSVJ2C19
POD7.C21*	RSVJ2C20
POD7.A1*	RSVJ2C21
POD7.A2*	RSVJ2C22
POD7.C23*	RSVJ2D19
POD7.C20*	RSVJ2D21
POD7.C22*	RSVJ2D22
A1	RSVJ2E19
A2	RSVJ2E20
B2	RSVJ2E21
C1	RSVJ2E22
C2	SYSEN
B1	CLK1
A4	CLK2

*These signals are located in the POD 7 jumpers area

Location of optional signals



The STAT variable

The STAT variable is used by the CompactPCI inverse assembler to decode CompactPCI bus transactions. *It should not be changed or deleted from the format menu.* The signals that make up the STAT variable are listed in the following table.

STAT Variable	CompactPCI Bus Signal Name
Bit 26	TRDY#
Bit 25	FRAME#
Bit 24	IRDY#
Bit 23	SDONE
Bit 22	SB0#

STAT Variable	CompactPCI Bus Signal Name
Bit 21	C/BE7#
Bit 20	C/BE6#
Bit 19	C/BE5#
Bit 18	C/BE4#
Bit 17	PAR64#
Bit 16	ACK64#
Bit 15	REQ64#
Bit 14	INTD#
Bit 13	INTC#
Bit 12	INTB#
Bit 11	INTA#
Bit 10	RESET#
Bit 9	C/BE3#
Bit 8	C/BE2#
Bit 7	C/BE1#
Bit 6	C/BE0#
Bit 5	DEVSE#L
Bit 4	STOP#
Bit 3	LOCK#
Bit 2	PERR#
Bit 1	SERR#
Bit 0	PAR

The ADDR, ADDR_B and DATA variables

The ADDR variable is the lower 32 bits of the CompactPCI AD bus. The ADDR_B is the upper 32 bits of the CompactPCI AD bus. The DATA variable is a dummy variable that needs to be defined for the CompactPCI inverse assembler. *These variables should not be changed or deleted from the format Menu.*

The CYCLE variable

The CYCLE variable is made up of the following CompactPCI signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL# and STOP#. This variable has 30 symbols defined that can be used to help make triggering, timing analysis and pattern filtering easier. The following lists the bit pattern and the corresponding symbol.

Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP
INTACK	1	0	1	0000	1	1
SPEC_CYC	1	0	1	0001	1	1
I/O_RD	1	0	1	0010	1	1
I/O_WR	1	0	1	0011	1	1
RESVRD	1	0	1	0100	1	1
RESVRD	1	0	1	0101	1	1
MEM_RD	1	0	1	0110	1	1
MEM_WR	1	0	1	0111	1	1
RESRVD	1	0	1	1000	1	1
RESRVD	1	0	1	1001	1	1
CON_RD	1	0	1	1010	1	1
CON_WR	1	0	1	1011	1	1
MEMRDM	1	0	1	1100	1	1
DAD_CY	1	0	1	1101	1	1
MEMRDL	1	0	1	1110	1	1
MEMWRI	1	0	1	1111	1	1
IO_XACTION	1	0	1	001X	1	1
MEM_XACTION	1	0	1	011X	1	1
CONFIG_XACTION	1	0	1	101X	1	1
ADD_CYCLE	1	0	1	XXXX	1	1
DATA_XFER	0	0	0	XXXX	0	1
WAIT_TARGET	1	X	0	XXXX	0	1
WAIT_INITIATOR	0	X	1	XXXX	0	1
DATA_FINALXFER	0	1	0	XXXX	0	1
STOP_NOXFER	X	0	1	XXXX	0	0
STOP_DATAXFER	0	X	0	XXXX	0	0
STOP_RETRY	1	1	0	XXXX	0	0

Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP
TARGET_ABORT	1	0	1	XXXX	1	0
IDLE	X	1	1	XXXX	X	X
WAIT_NODEVSL/F_0	X	0	0	XXXX	1	1
WAIT_NODEVSEL	X	X	0	XXXX	1	1

State Analysis

This chapter explains how to configure the CompactPCI Analysis Probe to perform state analysis on the CompactPCI Local Bus. The configuration software on the flexible diskette sets up the format specification menu of the logic analyzer for compatibility with the CompactPCI Local Bus. The next chapter explains how to configure the CompactPCI Analysis Probe to perform timing analysis.

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the CompactPCI Analysis Probe module.

1. Set jumpers JMP2-JMP5 to the appropriate position on the CompactPCI Analysis Probe module. See page 9 of this manual for details.
2. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe cable headers. See page 9 of this manual for details.
3. Install the CompactPCI Analysis Probe module into a slot in the target CompactPCI Local bus.
4. Load the logic analyzer configuration file by loading the appropriate file from the Analysis Probe interface diskette. See page 11 of this manual for details.

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Slow or Missing Clock" if the PCI clock is not transitioning.

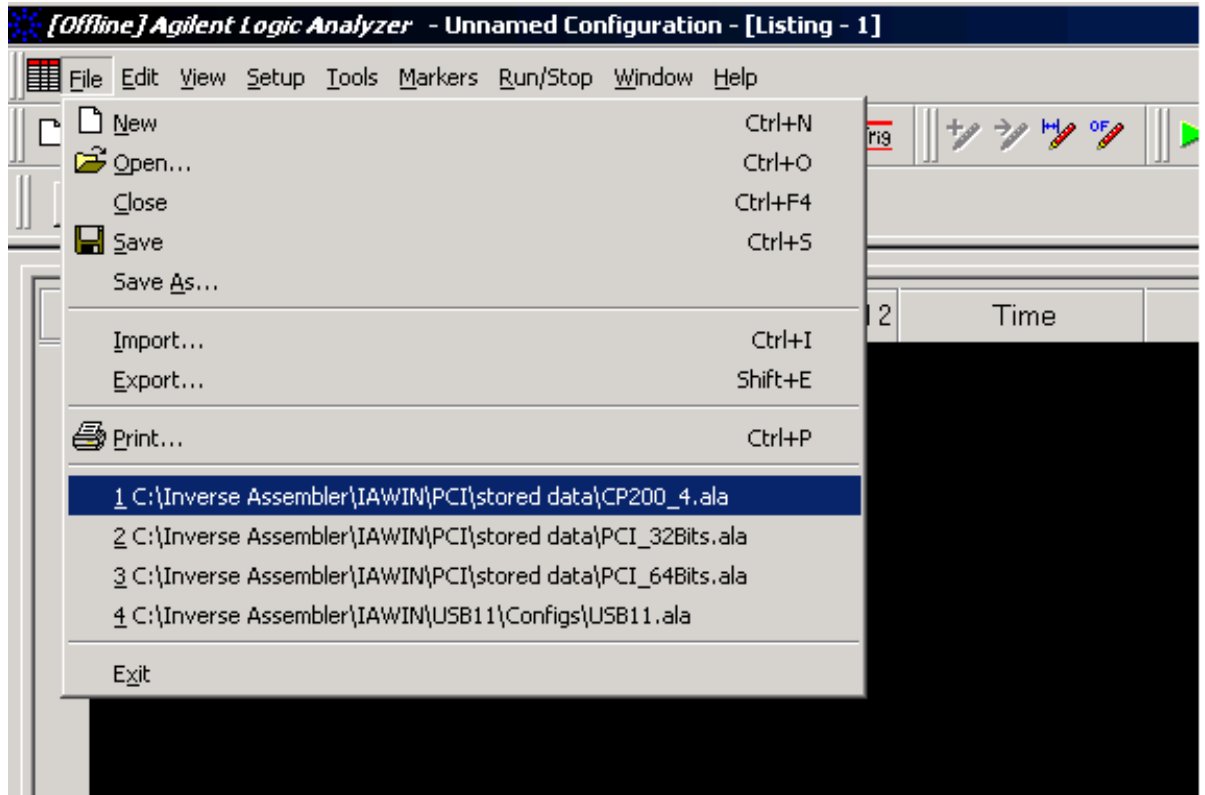
Acquiring data on the 1680/90

Execute the Agilent Logic Analyzer software on the PC and then load the appropriate configuration file.

There are two methods of loading the configuration file. The first method is to pull down the File->Open menu and navigate to the ..\Program Files\Agilent Technologies\Logic Analyzer\AddIns\FuturePlus\configs\FS3020 folder and select the appropriate configuration file e.g. CP302_9.ala or CP302_10.ala.

Alternatively, if the configuration file has been loaded during a prior execution of the logic analyzer, the configuration file can be

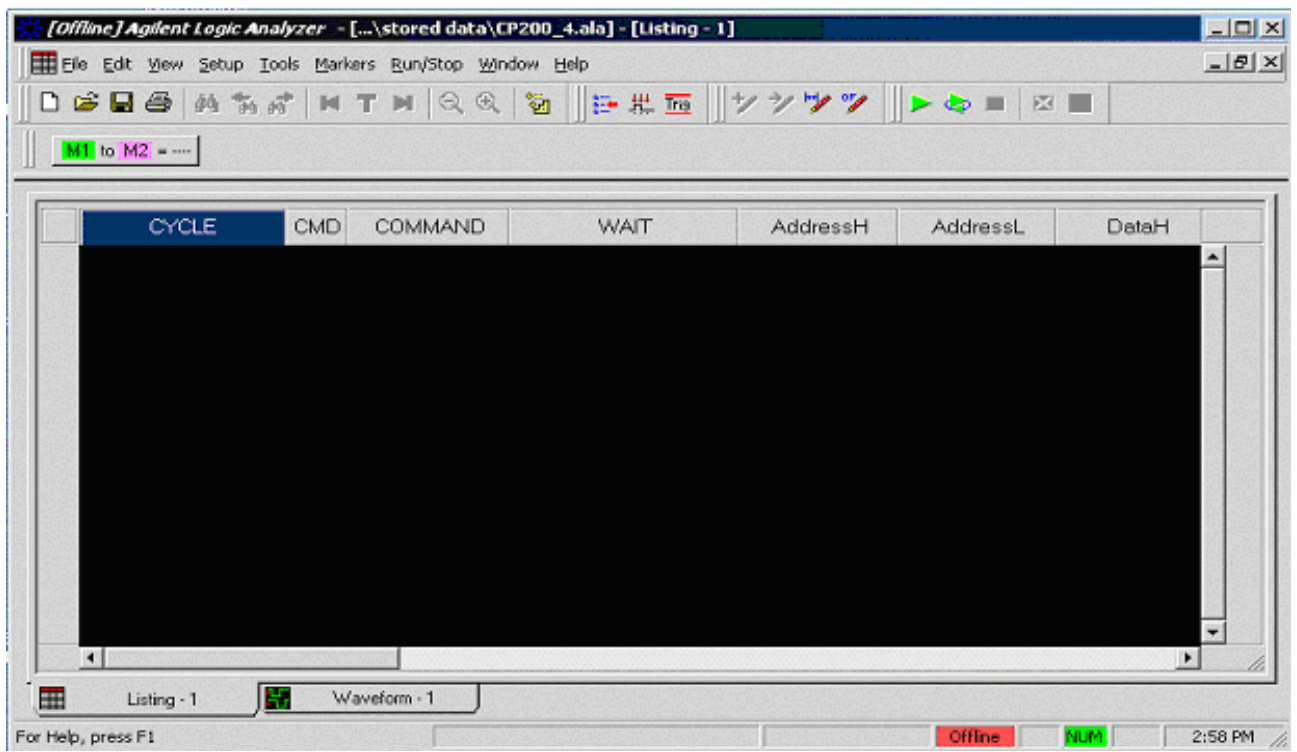
selected from the recently loaded configuration files that are listed at the bottom of the File pull-down menu as shown in the following figure.



Load Configuration File Figure

To capture PCI data, depress the F5 key or click the green arrow (run) button that is located on the tool bar at the top of the screen.

Alternatively, hit the Alt-F5 key or click the other green button that is located just to the right of the run button in order to acquire repetitive runs of data after the configuration file has been loaded as seen in the following figure.



The State Display

Captured data is as shown in the following figure. The below figures displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the CompactPCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays CompactPCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

16500 Display

100/500MHz LA E

Listing 1

Print

Run

Markers
Time

Trig to X
0 s

Trig to 0
0 s

X to 0
0 s

Label>	PCI BUS TRANSACTIONS	Time	C/B3_0
Base>	REV 2.2	Relative	Hex
242	D32=xxxxxxx08	296 ns	E
243	I/O READ ADR=00000073	9.072 us	2
244	D32=23xxxxxxx	1.096 us	7
245	I/O WRITE ADR=00000020	10.97 us	3
246	D32=xxxxxxx20	168 ns	E
247	INTERRUPT ACK CYCLE	54.90 ms	0
248	D32=xxxxxxx08	296 ns	E
249	I/O READ ADR=00000073	9.904 us	2
250	D32=23xxxxxxx	1.128 us	7
251	I/O WRITE ADR=00000020	10.97 us	3
252	D32=xxxxxxx20	168 ns	E

16700 Display

Listing<2>

File Window Edit Options Invasm Source Help

Goto Markers Search Comments Analysis Mixed Signal

Label ACK/RQ Hex when Present Next Prev

Advanced searching Set G1 Set G2

State Number	Time	FUTUREPLUS SYSTEMS c 1998	CYCLE	STAT	U
Decimal	Relative	PCI BUS TRANSACTIONS REV 1.1	Symbols	Hex	H
640	16,000 ns	FUNC=1 REG OFFSET=4 TYPE=00			
		WAIT-NO DEVICE SELECT	WAIT_NODVSEL	7DF3C	0
641	76,000 ns	COMMAND=0000	STOP_DATAxFE	7C33C	0
642	4,292 us	CONFG READ ADR=00010000	CON_RD	73FBA	0
		FUNC=0 REG OFFSET=0 TYPE=00			
643	12,000 ns	WAIT-NO DEVICE SELECT	WAIT_NODVSEL	65F30	0
644	76,000 ns	VENDOR ID=8086	STOP_DATAxFE	64330	0
645	24,764 us	CONFG WR ADR=00010004	CON_WR	73FFB	0
		FUNC=0 REG OFFSET=4 TYPE=00			
646	16,000 ns	WAIT-NO DEVICE SELECT	WAIT_NODVSEL	7DF3C	0
647	76,000 ns	COMMAND=0000	STOP_DATAxFE	7C33C	0
648	28,072 ms	CONFG READ ADR=00000000	CON_RD	73FBA	0
		FUNC=0 REG OFFSET=0 TYPE=00			
649	12,000 ns	WAIT-NO DEVICE SELECT	WAIT_NODVSEL	65F30	0
650	16,000 ns	WAIT-NO DEVICE SELECT	WAIT_NODVSEL	65F30	0

16700 Display

[Offline] Agilent Logic Analyzer - [...\stored data\CP200_4.ala] - [Listing - 1]

File Edit View Setup Tools Markers Run/Stop Window Help

M1 to M2 = 4.95 ns

LE	CMD	COMMAND	WAIT	AddressH	AddressL	DataH	DataL	Termination	Term_Code	
				Created by PCI Inverse Assembler - 1						
4B 0002	I/O Read		Wait-No DEVSEL				xxxxxx36	Initiator	0	
B9 0002										
4B 0002	I/O Read		Wait-No DEVSEL		00000040					
B8 0002								STOP Retry	3	
4B 0002	I/O Read		Wait-No DEVSEL		00000040					
B8 0002										
B9 0002							xxxxxx17	Initiator	0	
4F 0003	I/O Write		Wait-No DEVSEL		00000021					
B7 0003										
B5 0003							xxxxFCxx	Initiator	0	
4F 0003	I/O Write		Wait-No DEVSEL		000000A1					
B7 0003										
M1	B5 0003						xxxxFDxx	Initiator	0	
M2	47 0001	Spec Cyc								
	83 0001	Cmd=Halt, M...			00000001					
	83 0001		Wait-No DEVSEL							
	83 0001		Wait-No DEVSEL					Mstr Abort	4	
	43 0000	Int Ack			00000000					
	9B 0000		Wait-No DEVSEL				50xxxx50	Initiator	0	
	99 0000									
	4F 0003	I/O Write			00000021					
	B7 0003		Wait-No DEVSEL							
	B5 0003						xxxxFDxx	Initiator	0	
	4F 0003	I/O Write			00000020					
	B8 0003		Wait-No DEVSEL							
	B9 0003						xxxxxx60	Initiator	0	
	4F 0003	I/O Write			00000021					
	B7 0003		Wait-No DEVSEL							

Listing - 1 Waveform - 1

For Help, press F1 Offline NUM 3:11 PM

Error Messages

The following error messages are reported by the CompactPCI inverse assembler.

ERROR-NO DEVICE SELECTED

This error is displayed during a non special cycle data phase when IRDY and TRDY are asserted and DEVSEL is not asserted.

ERROR DEVSEL ASSERTED

This error is displayed during a special cycle data phase if DEVSEL is asserted.

SYSTEM ERROR

This error is displayed anytime SERR# is asserted.

1680/90 Errors:

XXX input label could not be attached to.

This error is displayed when the 1680/90 IA is being started and a failure occurs during the creation of an input label/column.

XXX: input label invalid Min/Max parameters.

This error is displayed during the creation of a label/column. The IA expects the label/column to fall within a min/max number of bits which has been violated.

XXX: Failed to unattach from label

This error is displayed when the 1680/90 IA is being exited and a failure occurs during the label/column destruction

XXX: output label could not be created.

This error is displayed when the 1680/90 IA is being started and a failure occurs when an output label/column is being constructed

XXX: symbol could not be created.

This error is displayed when the 1680/90 IA is being started and a failure occurs when an output or input label/column symbol could not be created

XXX: Could not save Label

This error is displayed when the 1680/90 IA configuration file is being created and/or updated. The configuration data for the specified label could not be written to the file and thus will be lost.

XXX: Could not load Label

This error is displayed when the 1680/90 IA configuration file is being read. The configuration data for the specified label could not be read to the file and thus will be lost.

INVASM OPTIONS

INVASM OPTIONS is available with the following logic analyzers.

- 1655xA in a 16500B main frame
- 166x, series with 2.0 system software
- 16700 series

1680/90 does not implement an INVASM Options menu

INVASM OPTIONS for the 165xx can be invoked by selecting INVASM OPTIONS from the state listing display. The following selection will be displayed.

- I/O Reads
- I/O Writes
- Configuration Reads
- Configuration Writes
- Memory transactions (all memory transactions)
- IDLE cycles
- WAIT cycles
- All other transactions (this includes Interrupt Acknowledge and Special Cycle transactions)

Filtering

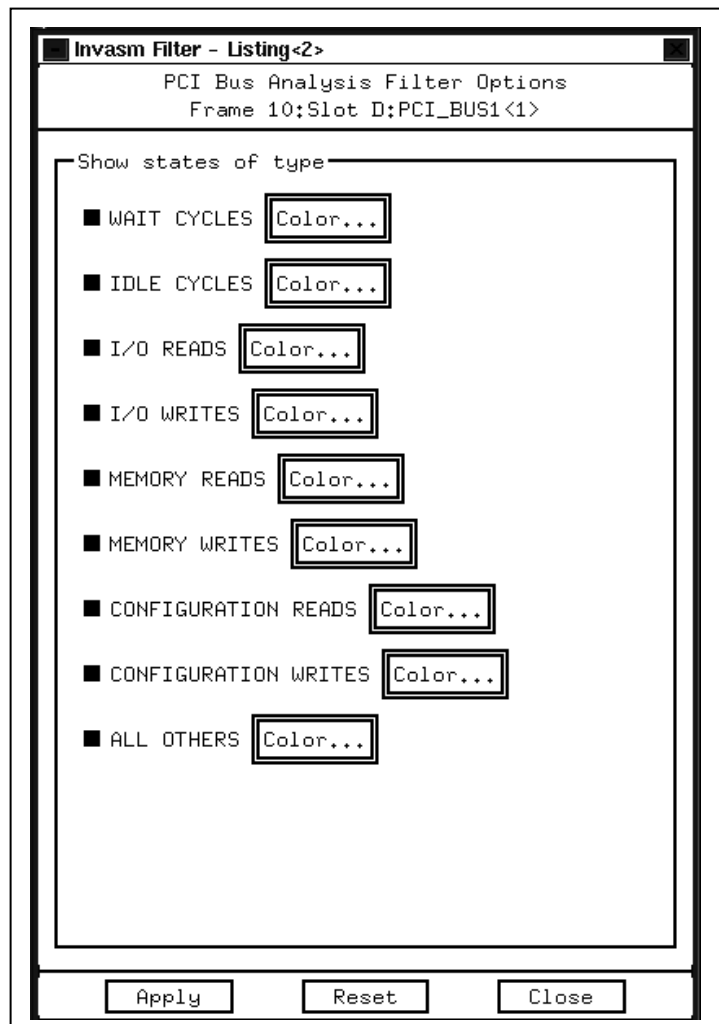
The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the show/suppress button to the right of the transaction cycle list.

For **16700** users, select filter under INVASM in the state listing and choose filter to display the color options. Below is a display taken from the 16700 showing the filter options screen. To filter out any state just point to the state you want filtered out, and click on it. The black box to the left of the state you chose will turn gray. To turn the state back on, simply click on the state again.

For **1680/90** users, select the Filter/Colorization pull down menus in the state listing and create a filter (downstream) tool.

The 1680/90 IA allows filtering that is equivalent to the 16700/702 environments. You may filter on any label, when using the filter tags label you can select symbols to make choosing transactions easier. To create a filter, navigate to the Tools->New->Filter/Colorize menu and fill in the information on the subsequent windows that are displayed. You must create a new filter for each item you want filtered. To remove, navigate to the Tools->Overview menu and then select the filter you want removed and click Delete.

16700 Invasm Filter Options



Using the PC Mapper Inverse Assembler

Setting up the Analyzer from the diskette

The Inverse Assembler

The CompactPCI Analysis Probe PC Mapper software is an enhanced version of the CompactPCI Analysis Probe inverse assembler and is for use only with CompactPCI Analysis Probe from FuturePlus Systems Corporation. The enhancement includes CompactPCI I/O and memory address decode to indicate common PC access.

PC Mapper is currently not available on the 1680/90 analyzer.

After the configuration file is loaded the CompactPCI PC Mapper software can be loaded:

1. Install the CompactPCI Analysis Probe software flexible diskette in the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the appropriate file (see table below)

16500 Inverse Assemblers

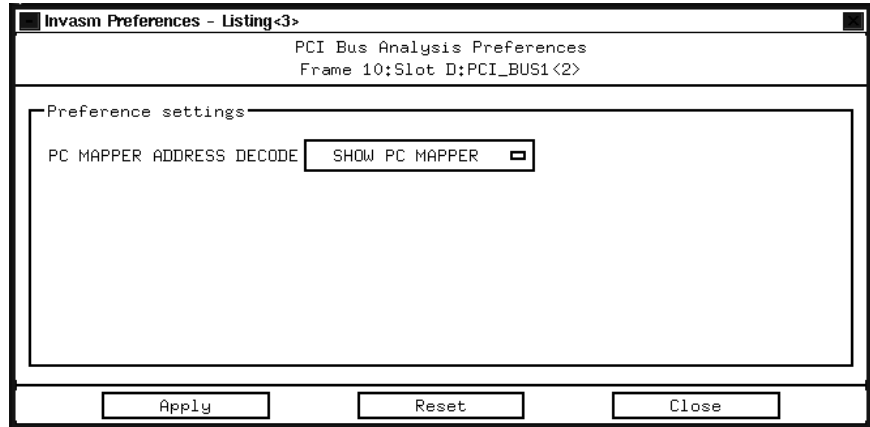
Logic Analyzer	File name
16500B mainframe with 16555, 16550A or 167x series	IAPCIMPE
16500B mainframe with 16510	IAPCIMP
16500A mainframe (all logic analyzer models)	IACPCIMP
166x (with REV 2.2 system software or later)	IAPCIMPE
165x logic analyzers	IAPCIMP

3. Execute the load operation to load the file into the logic analyzer.

IFS3020E is the inverse assembler for all logic analyzers installed into the 16700 and is auto loaded when the configuration file is loaded.

To select PC Mapper function on the 16700, select INVASM from the state listing display then select PREFERENCES. When you select PREFERENCES it will come up with a box and there you can choose to turn on PC Mapper or suppress PC Mapper. The picture below displays PC Mapper function enabled on the 16700.

Acquiring Data



The State Display with the CompactPCI PC Mapper

Captured data is as shown in the following figure. The first figure displays the state listing after disassembly. The PCI PC Mapper is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the CompactPCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays CompactPCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

100/500MHz LA E Listing 1 Invasm Options Print Run

Markers Time Trig to X 0 s Trig to 0 0 s X to 0 0 s

Label>	PCI BUS TRANSACTIONS	Time	C/B3_0
Base>	PC MAPPER PRE-RELEASE VERSION	Relative	Hex
39	RTC/CMOS RAM DATA PORT I/O WRITE ADR=00000071 REQ64 D32=xxxx00xx	2.960 us	3
40		1.168 us	D
41	VIDEO MEMORY MEM WRITE ADR=000B81E0 REQ64 D32=xxxxxx30	41.55 us	7
42		72 ns	E
43	VGA CRT CNTRLR ADDR REG I/O WRITE ADR=000003D4 REQ64 D32=xxxx000E	4.832 us	3
44		264 ns	C
45	VGA CRT CNTRLR ADDR REG I/O WRITE ADR=000003D4 REQ64 D32=xxxxF10F	440 ns	3
46		264 ns	C

The above display data using the CompactPCI Inverse Assembly software, without the CompactPCI PC Mapper functionality is shown as follows.

100/500MHz LA E Listing 1 Invasm Options Print Run

Markers Time Trig to X 0 s Trig to 0 0 s X to 0 0 s

Label>	PCI BUS TRANSACTIONS		Time	C/B3_0
Base>	REV 2.2		Relative	Hex
37	I/O WRITE	ADR=00000070 REQ64#	1.200 us	3
38		D32=xxxxxx8F	1.072 us	E
39	I/O WRITE	ADR=00000071 REQ64#	2.960 us	3
40		D32=xxxx00xx	1.168 us	D
41	MEM WRITE	ADR=000B81E0 REQ64#	41.55 us	7
42		D32=xxxxxx30	72 ns	E
43	I/O WRITE	ADR=000003D4 REQ64#	4.832 us	3
44		D32=xxxx000E	264 ns	C
45	I/O WRITE	ADR=000003D4 REQ64#	440 ns	3
46		D32=xxxxF10F	264 ns	C
47	I/O WRITE	ADR=00000070 REQ64#	4.064 us	3

The following listing shows the PC Mapper preference selected on the 16700.

Listing<4>

File Window Edit Options Invasm Source Help

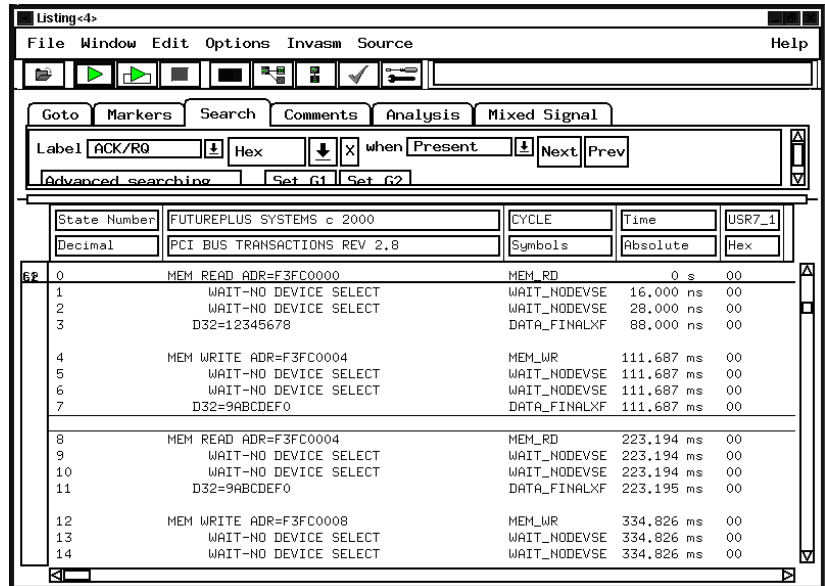
Goto Markers Search Comments Analysis Mixed Signal

Label ACK/RQ Hex when Present Next Prev

Advanced searching Set G1 Set G2

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	USR7_1
Decimal	PCI BUS TRANSACTIONS REV 2.8	Symbols	Absolute	Hex
0	SYSTEM MEMORY	MEM_RD	0 s	00
	MEM READ ADR=F3FC0000			
1	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	16.000 ns	00
2	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	28.000 ns	00
3	D32=12345678	DATA_FINALXF	88.000 ns	00
4	SYSTEM MEMORY	MEM_WR	111.687 ms	00
	MEM WRITE ADR=F3FC0004			
5	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111.687 ms	00
6	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111.687 ms	00
7	D32=9ABCDEF0	DATA_FINALXF	111.687 ms	00
8	SYSTEM MEMORY	MEM_RD	223.194 ms	00
	MEM READ ADR=F3FC0004			
9	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223.194 ms	00
10	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223.194 ms	00
11	D32=9ABCDEF0	DATA_FINALXF	223.195 ms	00

The following listing shows the PC Mapper preference suppressed on the 16700.



PCI PC Mapping for memory transactions

This section lists the addresses, the commands and the corresponding mapping done by the PCI PC Mapper software. For information on the standard PCI configuration register mapping please refer to the PCI Local Bus Specification Rev 2.0.

Address bits 23-0	PC Mapper output
greater than 0FFFFFFH	System Memory
0FFFFFF-0E0000H	System BIOS
0DFFFFFF-0C0000H	ROM Scan
0BFFFFFF-0A0000H	Video Memory
09FFFFFF-000400H	System Memory
0003FF-000000H	See Interrupt Vector Table

Interrupt Vector Table

Address bits 23-0	PC Mapper output
0003C4H	INT #F1-FF USER PROGRAMS
000200H	INT #80-F0 BASIC
0001E0H	INT #78-7F USER PROGRAMS
0001DCH	INT #77 IRQ15
0001D8H	INT #76 IRQ14
0001D4H	INT #75 IRQ13
0001D0H	INT #74 IRQ12
0001CCH	INT #73 IRQ11
0001C8H	INT #72 IRQ10
0001C4H	INT #71 IRQ9
0001C0H	INT #70 IRQ8
0001A0H	INT #68-6F RESERVED
00019CH	INT #67 EXP MEM MANG
000180H	INT #60-66 USER PROGRAMS
00012CH	INT #4B-5F RESERVED
000128H	INT #4A USER RTC ALARM
00011CH	INT #47-49 RESERVED
000118H	INT #46 HD DISK #1 PARAM
000110H	INT #44-45 RESERVED
00010CH	INT #43 VIDEO CHAR TABLE
000108H	INT #42 EGA BIOS
000104H	INT #41 HD DISK #0 PARAM
000100H	INT #40 FLOPPY DISK ISR
000080H	INT #20-3F RESERVED DOS
00007CH	INT #1F VIDEO CHAR TABLE
000078H	INT #1E FLOPPY PARAMS
000074H	INT #1D AVAILABLE
000070H	INT #1C AVAILABLE
00006CH	INT #1B KEYBOARD BREAK
000068H	INT #1A RTC ISR
000064H	INT #19 BOOSTRAP LOADER
000060H	INT #18 ROM BASIC
00005CH	INT #17 LPT PRINTER BIOS
000058H	INT #16 KEYBOARD BIOS
000054H	INT #15 SYS SERVICE BIOS
000050H	INT #14 SERIAL PORT BIOS
00004CH	INT #13 FLOPPY DISK BIOS
000048H	INT #12 MEM SIZE INT
000044H	INT #11 EQUIP LIST
000040H	INT #10 VIDEO BIOS
00003CH	INT #0F IRQ7 LPT1
000038H	INT #0E IRQ6 FLOPPY DISK
000034H	INT #0D IRQ5 LPT2
000030H	INT #0C IRQ4 SERIAL #1
00002CH	INT #0B IRQ3 SERIAL #2
000028H	INT #0A IRQ2 SLAVE INT
000024H	INT #09 KEYBOARD
000020H	INT #08 IRQ0 SYS TIMER
00001CH	INT #07 NUM COPROCESSOR
000018H	INT #06 INVALID OPCODE
000014H	INT #05 PRINT SCREEN
000010H	INT #04 OVERFLOW DETECT

Address bits 23-0	PC Mapper output
00000CH	INT #03 BREAKPOINT TRACE
000008H	INT #02 NMI
000004H	INT #01 SINGLE STEP
000000H	INT #00 DIVIDE BY ZERO

**CompactPCI PC
Mapping - I/O
Transactions**

Address bits 23-0	PC Mapper output
0000H	MSTR DMA CH 0
0001H	MSTR DMA CH 0
0002H	MSTR DMA CH 1
0003H	MSTR DMA CH 1
0004H	MSTR DMA CH 2
0005H	MSTR DMA CH 2
0006H	MSTR DMA CH 3
0007H	MSTR DMA CH 3
0008H	MSTR DMA STAT REG
0009H	UNKNOWN IO DEVICE
000AH	MSTR DMA MASK REG
000BH	MSTR DMA MODE REG
000CH	MSTR DMA CLR BYTE PTR
000DH	MSTR DMA MSTR CLEAR
000EH	MSTR DMA CLEAR MASK
000FH	MSTR DMA WRT MASK
0018H	MSTR DMA CH EXT FUNCT REG
001AH	MSTR DMA EXT FUNCT
0020H	MSTR INT REQ REG
0021H	MSTR INT REQ REG2
0040H	INTERVAL TIMER 0
0042H	INTERVAL TIMER SPKR TIMER
0043H	INTRVAL TIMER #1 CNTRL
0044H	INTERVL TIMER #2 WATCHDOG
0047H	INTERVAL TIMER #2 CNTRL
0060H	KEYBOARD/MOUSE DATA PORT
0061H	SYSTEM CONTOL PORT B
0064H	KEYBOARD/MOUSE CMD PORT
0070H	RTC/CMOS RAM ADDR PORT
0071H	RTC/CMOS RAM DATA PORT
0074H	EXT CMOS RAM ADDR PORT
0075H	EXT CMOS RAM ADDR PORT
0076H	EXT CMOS RAM DATA PORT
0081H	CH 2 DMA PAGE REGISTER
0082H	CH 3 DMA PAGE REGISTER
0083H	CH 1 DMA PAGE REGISTER
0087H	CH 0 DMA PAGE REGISTER
0089H	CH 6 DMA PAGE REGISTER
008AH	CH 7 DMA PAGE REGISTER
008BH	CH 5 DMA PAGE REGISTER
008FH	CH 4 DMA PAGE REGISTER
0090H	ARB CNTRL POINT REG
0091H	FEEDBACK REG
0092H	SYSTEM CONTROL PORT A
0094H	SYS SETUP/CARD ENABLE REG
0096H	ADAPTOR SETUP/ENABLE REG
00A0H	SLAVE INTERRUPT CNTRLR
00A1H	SLAVE INTERRUPT CNTRLR
00C0H	SLAVE DMA CH4 MEM ADDR
00C2H	SLAVE DMA CH4 TRANS COUNT
00C4H	SLAVE DMA CH5 MEM ADDR
00C6H	SLAVE DMA CH5 TRANS COUNT

Address bits 23-0	PC Mapper output
00C8H	SLAVE DMA CH6 MEM ADDR
00CAH	SLV DMA CH6 TRANS COUNT
00CCH	SLAVE DMA CH7 MEM ADDR
00CEH	SLAVE DMA CH7 TRANS COUNT
00D0H	SLV DMA STATUS REG CH 4-7
00D4H	SLV DMA MASK REG CH 4-7
00D6H	SLAVE DMA MODE REG CH 4-7
00D8H	SLAVE DMA CLEAR BYTE PNTR
00DAH	SLAVE DMA MASTER CLEAR
00DCH	SLV DMA CLR MASK CH 4-7
00DEH	SLAVE DMA WRITE MASK REG
00E0H	IBM MODELS - ENCODE REG
00E1H	IBM MODELS - ENCODE REG
00F1H	NUMERIC COPROCESSOR RESET
00F8H	NUMERIC COPROCESSOR PORT
00F9H	NUMERIC COPROCESSOR PORT
00FAH	NUMERIC COPROCESSOR PORT
00FBH	NUMERIC COPROCESSOR PORT
00FCH	NUMERIC COPROCESSOR PORT
0100H	ADAPTER CARD POS REG 0
0101H	ADAPTER CARD POS REG 1
0102H	SYS BD/ADP CD POS REG 2
0103H	SYS BD/ADP CD POS REG 3
0104H	ADAPTER CARD POS REG 4
0105H	ADAPTER CARD POS REG 5
0106H	ADAPTER CARD POS REG 6
0107H	ADAPTER CARD POS REG 6
0278H	PARALLEL PORT 3 DATA PORT
0279H	PARALLEL PORT 3 STAT PORT
027AH	PARALLEL PORT 3 CMD PORT
02F8H	SERIAL PORT 2 XMIT/REC
02F9H	SER PORT 2 DIV LATCH/INT
02FAH	SERIAL PORT 2 INT ID REG
02FBH	SERIAL PORT 2 CNTRL REG
02FDH	SERIAL PORT 2 MODEM CNTRL
02FEH	SERIAL PORT 2 MODEM STAT
02FFH	SERIAL PORT 2 SCRTCH REG
0378H	PARALLEL PORT 2 DATA PORT
0379H	PARALLEL PORT 2 STAT PORT
037AH	PARALLEL PORT 2 CMD PORT
03B4H	VGA CRT CNTRLR ADDR REG
03B5H	VGA CRT CNTRLR DATA REG
03BAH	VGA STAT 1/FEATURE CNTRL
03BCH	PARALLEL PORT 1 DATA PORT
03BDH	PARALLEL PORT 1 STAT PORT
03BEH	PARALLEL PORT 1 CMD PORT
03C0H	VGA ATTRIBUTE CNTRLR ADDR
03C1H	VGA ATTRIBUTE CNTRLR DATA
03C2H	VGA OUTPUT/STAT REG
03C3H	VGA VIDEO SUBSYSTEM ENABLE
03C4H	VGA SEQUENCER ADDR REG
03C5H	VGA SEQUENCER DATA REG

Address bits 23-0	PC Mapper output
03C6H	VIDEO DAC PEL MASK
03C7H	VIDEO DAC PAL ADDR/STAT
03C8H	VIDEO DAC PAL ADDR/WRITE
03C9H	VIDEO DAC PALETTE DATA
03CAH	VGA FEATURE CONTROL REG
03CCH	VGA MISC OUTPUT REG
03CEH	VGA GRAPHICS CONTROLR ADDR
03CFH	VGA GRAPHICS CONTROLR ADDR
03D4H	VGA CRT CONTROLR ADDR REG
03D5H	VGA GRAPHICS CONTROLR DATA
03DAH	VGA COLOR STAT 1/FEATURE
03F0H	FLOPPY STATUS REG A
03F1H	FLOPPY STATUS REG B
03F2H	FLOPPY DIGITAL OUTPUT REG
03F4H	FLOPPY DISK CONTROLR STAT
03F5H	FLOPPY DISK CONTROLR DATA
03F7H	FLOPPY CONFIG CONTROL REG
03F8H	SERIAL PORT 1 XMIT/RCV BUF
03F9H	SER PORT 1 DIV LATCH/INT
03FAH	SERIAL PORT 1 INT ID/FIFO
03FBH	SERIAL PORT 1 LINE CONTROL
03FCH	SERIAL PORT 1 MODEM CONTROL
03FDH	SERIAL PORT 1 STAT REG
03FEH	SERIAL PORT 1 MODEM STAT
03FFH	SERIAL PORT 1 SCRATCH REG
0680H	MANUFACTURING CHECKPOINT PORT

Timing Analysis

Since the CompactPCI Analysis Probe interface contains only passive matching terminators it introduces negligible skew to the CompactPCI Local Bus signals.

Installation Quick Reference

The following procedure describes the major steps required to perform timing analysis measurements with the CompactPCI Analysis Probe module.

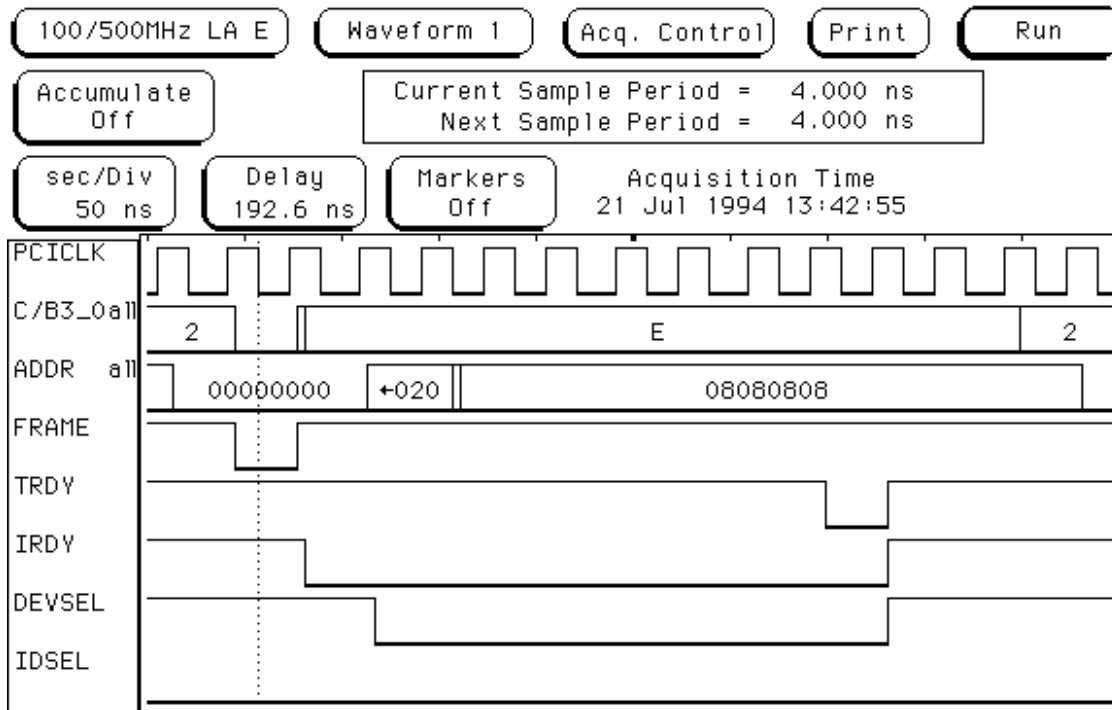
1. Set the jumpers to the appropriate position on the CompactPCI Analysis Probe module. See page 9 of this manual for details.
2. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe cable headers. See page 9 of this manual for details.
3. Install the CompactPCI Analysis Probe module into a slot in the target CompactPCI Local bus.
4. Load the logic analyzer configuration file by loading the appropriate file from the Analysis Probe interface diskette. See page 11 of this manual for details.

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The Waveform Display

Captured data is displayed as shown in the following figure.



General Information

This chapter provides additional reference information including the characteristics and signal connections for the CompactPCI Analysis Probe module.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the CompactPCI Analysis Probe module.

3.3V and 5.0V Analysis Probe Interface Compatibility

32/64 bit CompactPCI Local bus keyed for 5v operation . For 3.3V operation remove the 3.3V key from the CompactPCI connector.

JTAG Boundary Scan

The CompactPCI Analysis Probe does not implement JTAG Boundary SCAN. Pins TDI and TBO are connected to JP1. If the jumper is across pins 1 and 2 then TDI and TDO are connected together so the scan chain is not broken. If the jumper is removed the CompactPCI add-in card in the extender card connector is in control of these signals.

Standards Supported

The PCI Local Bus Specification Revision 2.1 and the CompactPCI specification.

Power Requirements

The CompactPCI Analysis Probe contains no active components and therefore requires no power. 5V, 3.3 and VI/O are passed up to the extender card connector.

Logic Analyzer Required Number of Probes Used

166x, 167x, 16550A, 16510B, 1650B

32 bit CompactPCI Local Bus - 4 cable headers

64 bit CompactPCI Local Bus - 6 cable headers

System slot signals - 1 additional header.

Minimum Clock Period (State)

Not limited by the Analysis Probe. Clocking is specified by the logic analyzer.

Signal loading

The FS3020 Analysis Probe logic presents one 10pf/90k ohm load on each PCI bus signal. The extender card connector adds an addition 2pf. If stake pins are installed as test points they add 1pf. The etch and associated via's add approximately 1pf of additional capacitance.

Etch length

The etch length from the CompactPCI connector to the pad of the extender card connector averages 9 inches on all signals. The signals are all daisy chained from the CompactPCI connector to the test points to the logic analyzer terminators to the extender card connector. From the output of the terminators the signal goes to the 40 pin headers.

Operations

All CompactPCI Local Bus operations supported.

***Environmental
Temperature***

Operating: 0 to 55 degrees C (+32 to +131 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 90% non condensing. Avoid sudden, extreme temperature changes which would cause condensation on the Analysis Probe module.

***Testing and
Troubleshooting***

There are no automatic performance tests or adjustments for the CompactPCI Analysis Probe module. If a failure is suspected in the CompactPCI Analysis Probe module contact the factory or your FuturePlus Systems authorized distributor.

Servicing

The repair strategy for the CompactPCI Analysis Probe is module replacement. However, if parts of the CompactPCI Analysis Probe module are damaged or lost contact the factory for a list of replacement parts.

Signal Connections

The CompactPCI Analysis Probe module monitors signals for both state and timing analysis. The below figure displays how the cable headers are numbered.

39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

The following tables list the CompactPCI Analysis Probe cable headers and the corresponding CompactPCI Local Bus signals after these signals have been terminated by the 90K ohm/10pf terminators.

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name
Header 1 pin 3	CLK/16	IRDY# visible here only on 166x, 167x/55x
5	no connect	
7	15	AD15
9	14	AD14
11	13	AD13
13	12	AD12
15	11	AD11
17	10	AD10
19	9	AD09
21	8	AD08
23	7	AD07
25	6	AD06
27	5	AD05
29	4	AD04
31	3	AD03
33	2	AD02
35	1	AD01
37	0	AD00

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name
Header 2 pin 3	CLK/16	FRAME# visible here only on 166x, 167x/55x
5	no connect	
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name
Header 3 pin 3	CLK/16	CompactPCI Clock visible here only on 166x, 167x/55x
5	no connect	
7	15	CompactPCI Clock/510 only controlled by JMP 4
9	14	INTD#
11	13	INTC#
13	12	INTB#
15	11	INTA#
17	10	RST#
19	9	C/BE3#
21	8	C/BE2#
23	7	C/BE1#
25	6	C/BE0#
27	5	DEVSEL#
29	4	STOP#
31	3	LOCK#
33	2	PERR#
35	1	SERR#
37	0	PAR

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name
Header 4 pin 3	CLK/16	TRDY# visible here only on 166x, 167x/55x
5	no connect	
7	15	USER7
9	14	USER6
11	13	USER5
13	12	USER4
15	11	USER3 FOR 166x, 167x AND 55x USERS TRDY# FOR 510 USERS
17	10	USER2 FOR 166x, 167x AND 55x USERS FRAME# FOR 510 USERS
19	9	USER1 FOR 166x, 167x AND 55x USERS IRDY# FOR 510 USERS
21	8	SDONE
23	7	SBO#
25	6	C/BE7#
27	5	C/BE6#
29	4	C/BE5#
31	3	C/BE4#
33	2	PAR64
35	1	ACK64#
37	0	REQ64#

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name
Header 5 pin 3	CLK/16	
5	no connect	
7	15	AD47
9	14	AD46
11	13	AD45
13	12	AD44
15	11	AD43
17	10	AD42
19	9	AD41
21	8	AD40
23	7	AD39
25	6	AD38
27	5	AD37
29	4	AD36
31	3	AD35
33	2	AD34
35	1	AD33
37	0	AD32

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name
Header 6 pin 3	CLK/16	
5	no connect	
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48

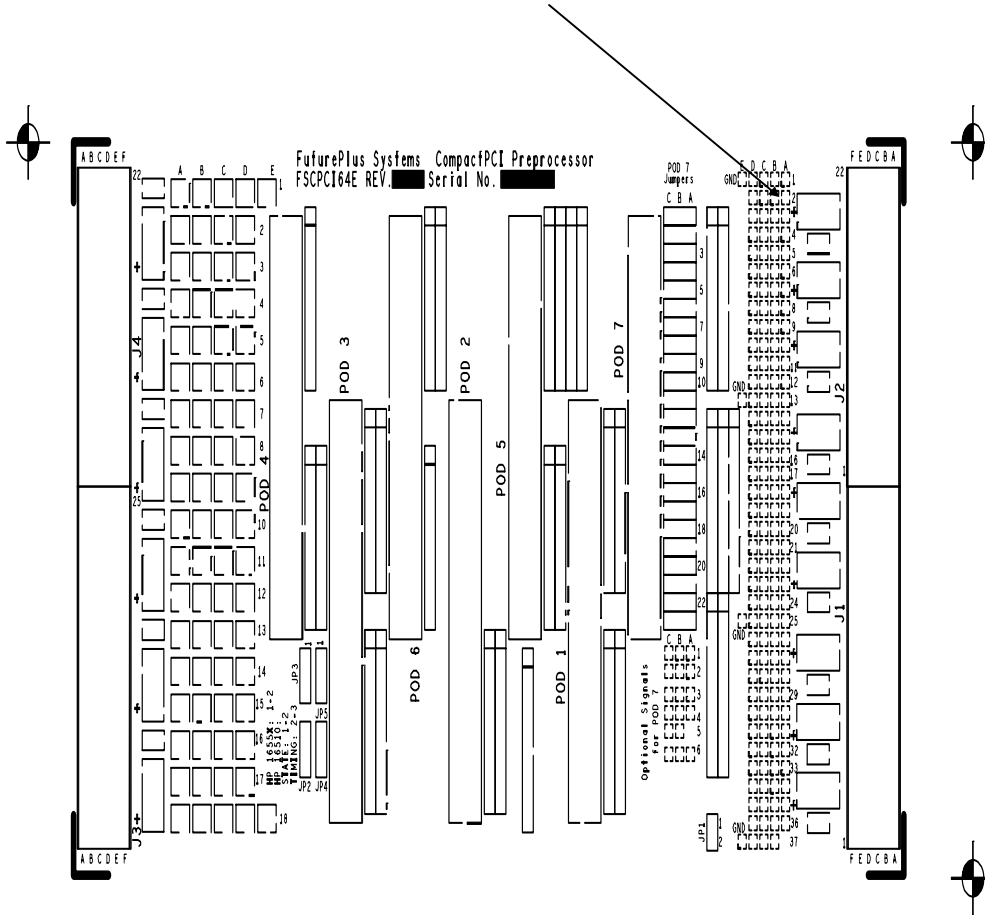
The POD 7 jumpers start at location 4 and go to location 19.
Jumpers are installed in position 1 (C-B).

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	CompactPCI Signal name jumper selectable position1 (C-B)/ position 2 (B-A)
Header 7 pin 3	CLK/16	CLK3
5	no connect	
7	15	CLK4/FAL#
9	14	PRST#/DEG#
11	13	INTP/ BRSVJ1A4
13	12	INTS/ BRSVJ1A5
15	11	REQ1#/ BRSVJ1B5
17	10	GNT1#/ BRSVJ1C25
19	9	REQ2#/ BRSVJ2B4
21	8	GNT2#/ BRSVJ2A15
23	7	REQ3#/ BRSVJ2A16
25	6	GNT3#/ BRSVJ2A17
27	5	REQ4#/ BRSVJ2B16
29	4	GNT4#/ BRSVJ2E16
31	3	REQ5#/ BRSVJ2A18
33	2	GNT5#/ BRSVJ2B18
35	1	REQ6#/ BRSVJ2C18
37	0	GNT6#/ BRSVJ2E18

Optional signals for POD 7 Location	CompactPCI Signal name
C5	RSVJ2A19
C3	RSVJ2A20
C3	RSVJ2A21
C4	RSVJ2A22
A3	RSVJ2B20
B5	RSVJ2B22
POD7.C1	RSVJ2C19
POD7.C21	RSVJ2C20
POD7.A1	RSVJ2C21
POD7.A2	RSVJ2C22
POD7.C23	RSVJ2D19
POD7.C20	RSVJ2D21
POD7.C22	RSVJ2D22
A1	RSVJ2E19
A2	RSVJ2E20
B2	RSVJ2E21
C1	RSVJ2E22
C2	SYSEN
B1	CLK1
A4	CLK2

Test Points

The FS3020 has test points that allow access to all the CompactPCI signals. The chart and drawing below show the location of each signal.



Location	CompactPCI signal	Location	CompactPCI signal
D32	C/BE3	B26	AD15
B29	C/BE2	A26	AD14
A6 OPTIONAL SIGNALS AREA	C/BE1	C26	AD13
C25	C/BE0	A25	AD12
D34	AD31	B25	AD11
A33	AD30	D26	AD10
B32	AD29	A24	AD09
C34	AD28	D25	AD08
B33	AD27	C24	AD07
C33	AD26	B24	AD06
C32	AD25	A23	AD05
D33	AD24	C23	AD04
A31	AD23	B23	AD03
A32	AD22	D24	AD02
D31	AD21	C22	AD01
C31	AD20	A22	AD00
A30	AD19	B34	CLK
C30	AD18	B35	GNT
B30	AD17	D23	ACK64
D30	AD16	D27	SERR
A36	INTA	A27	PERR
D37	INTB	B28	STOP
C37	INTC	D29	TRDY
B37	INTD	B27	SDONE
C35	RST	D28	SBO
D19	PAR64	B21	REQ64
B18	CLK3	A29	LOCK
B31	IDSEL	C28	DEVSEL
D35	REQ	C29	IRDY
B19	CLK1	A28	FRAME
D21	CLK2	C27	PAR
B18	CLK3	A13	AD49
D20	CLK4	B12	AD48

Location	CompactPCI signal	Location	CompactPCI signal
B16	C/BE4	B14	AD47
D18	C/BE5	A12	AD46
B17	C/BE6	C12	AD45
C19	C/BE7	B11	AD44
C17	AD63	C13	AD43
B15	AD62	B10	AD42
A17	AD61	A11	AD41
D16	AD60	A10	AD40
C16	AD59	D12	AD39
A14	AD58	B9	AD38
A16	AD57	C11	AD37
C14	AD56	A9	AD36
C15	AD55	C10	AD35
D14	AD54	A8	AD34
A15	AD53	D11	AD33
D13	AD52	C9	AD32
D15	AD51	C21	GNT1
B13	AD50	A21	GNT2
A18	SYSEN	C18	GNT3
D10	FAL	B20	GNT4
C7	DEG	B8	GNT5
D8	PRST	D7	GNT6
B36	INTP	A20	REQ1
C36	INTS	B22	REQ2
		A19	REQ3
		C20	REQ4
		A7	REQ5
		B7	REQ6