

# FuturePlus Systems® Corporation



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## FS3012 Users Manual

For use with Agilent Logic Analyzers

Revision 1.1

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# Introduction

The FS3012 PMC Analysis Probe and extender card performs three functions.

1. The first is to act as an extender card, extending the PMC card under test beyond the host board for easy debug at a maximum recommended clock speed of 66 MHz.
2. The second is to provide test points to measure power and AD signal fidelity.
3. The third is to provide a complete interface between any PMC add-in slot and Logic Analyzers. The Analysis Probe interface connects the signals from the PMC Local bus to the logic analyzer inputs.

The Analysis Probe interface is a passive bus monitor which does not assert any signals on the PMC bus. The PMC bus signals are terminated with 90k ohm/10pf terminators so that they are matched to the logic analyzer. Since the Analysis Probe interface does not actively buffer the PMC bus signals very little skew (500ps max.) is introduced.

The configuration software on the diskette sets up the format specification menu of the logic analyzer for compatibility with your PMC bus. When the state configuration file is loaded, an inverse assembler is also loaded which decodes PMC transactions into easy to read mnemonics.

## How to Use This Manual

This manual is organized to help you quickly find the information you need.

Analyzing the PMC Local Bus chapter introduces you to the FS3012 and lists the minimum equipment required and accessories supplied for PMC bus analysis.

The State Analysis chapter explains how to configure the FS3012 to perform state analysis on your PMC bus.

The Timing Analysis chapter explains how to configure the FS3012 to perform timing analysis on your PMC bus.

The General Information chapter provides information on the operating characteristics, the test point and cable header pinout.

# Analyzing the PMC Local Bus

This chapter introduces you to the FS3012 and lists the minimum equipment required and accessories supplied for PMC Local Bus analysis. This chapter also contains information that is common to both state and timing analysis.

## Duplicating the 167xx Logic Analyzer Master Diskette

Before you use the FS3012 software, make a duplicate copy of the master diskette. Then store the master diskette and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the diskette wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate diskette operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

## Accessories Supplied

The FS3012 product consists of the following accessories:

- The FS3012 hardware, which includes the interface circuit module.
- The inverse assembly and configuration software on 3.5 inch diskettes.
- This operating manual

## Minimum Equipment Required

The minimum equipment required for analysis of a PMC Local Bus consists of the following equipment:

- 167xx Analyzers. The diskette labeled "16700/702 Analysis Probe Install Disk for the FS3012" supports the 167xx analyzers. This is a licensed software product that is locked to a specific logic analyzer.
- CD containing the install executable program for the 1680/90/900 analyzers.
- The FS3012 probe
- A PMC target bus

## Signal Naming Conventions

This operating manual uses the same signal notation as the PCIX LOCAL BUS SPECIFICATION - REVISION 1.0a. That is, a # symbol at the end of a signal name indicates that the signal's

active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

## Connecting the logic analyzer to the FS3012

The following explains how to connect the logic analyzer to the FS3012 for either state or timing analysis:

1. Remove the probe tip assemblies from the logic analyzer cables.
2. Plug the logic analyzer cables into the FS3012 cable headers as shown in the appropriate table. For 64 bit analysis, configure 2 cards as a Master/Expander combination.

### For 1660/61/62, 167x, 16550A, 1674x, 167xx, 1695x Cards

Logic Analyzer	FS3012	Comment
POD 1	Header 1	Master Card
POD 2	Header 2	Master Card
POD 3	Header 3	L Clock
POD 4	Header 4	Master Card
POD 1	Header 5	Expander Card (64 bit only)
POD 2	Header 6	Expander Card (64 bit only)

### For 1680/90, 1691x Cards

Logic Analyzer	FS3012	Comment
POD 1	Header 1	
POD 2	Header 2	
POD 3	Header 3	Clock C3
POD 4	Header 4	
POD 5	Header 5	
POD 6	Header 6	

## How to install a PMC add-in card into the FS3012

The extender card connector of the FS3012 module can accommodate one PMC add in card. Simply align the module with the connector and gently push the module in until it is seated in the connector. The FS3012/PMC add-in card combination can then be installed in any slot of the PMC Local bus. For mechanical stability the FS3012 front bezel should be secured to the PMC target host board. In addition, two stand-offs are installed on the PMC Analysis Probe card and those can be secured to the host board.

When removing the PMC add-in card from the card edge extender connector grasp the FS3012 with one hand and the

## Operation of the PMC add-in card

PMC add-in card with the other. Gently rock the PMC add-in card until it is free from the connector.

The nature of an extender card is that it extends the etch length of the bus. Due to the sensitivity of most PMC designs, extending the etch length can interfere with the PMC add-in card operation. Operation of the PMC add-in card when installed in the card edge extender connector is not guaranteed. Please check your system design if you experience failures due to poor signal fidelity.

## Setting up the Analyzer installed in the 167xx mainframe

The 16700 requires a special install procedure to install the PCI Inverse Assembler. To accomplish this, insert the diskette labeled 16700 Analysis Probe Install Disk for the FS3012 into the 16700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen, select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL*.

**The installation procedure does not need to be repeated. It only needs to be done the first time the PMC Analysis Probe Adapter is used.**

When installation has completed, load the appropriate configuration file from the /configs/FuturePlus/FS3012 directory. Refer to the table on the following pages for a list of configuration files that will load into your specific logic analyzer cards.

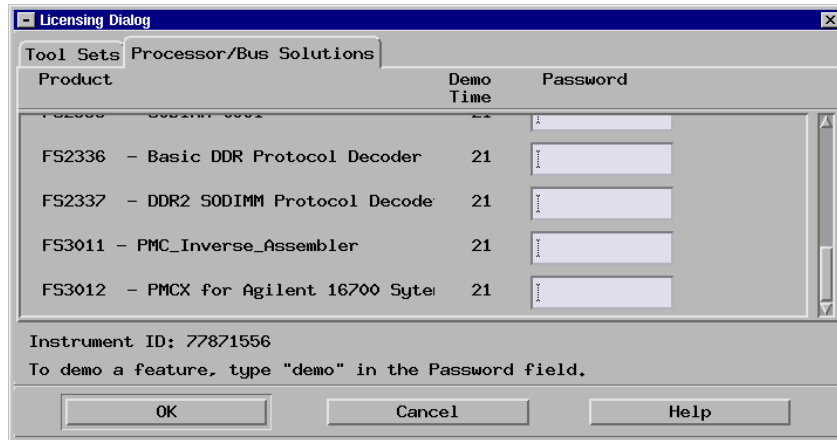
## 167xx Licensing

The FS3012 product is a licensed product, which is locked to a single Agilent 1670x frame. Complete instructions for licensing this software are detailed on the Entitlement Certificate that is enclosed with this product.

The licensing area for the 1670x mainframe is found under System Administration. Once you are at the licensing area choose the *Processor/Bus* Solutions tab, in here you will find the PMC inverse assembler listed. Type your password in the space provided to enable the use of the inverse assembler.

A demo period is provided by typing the word *demo* into the password space next to the product name.

The following picture shows the licensing area after pressing the licensing button on the previous screen. This is where you would enter the password you will receive after following the instructions on the SW License Entitlement Certificate.



## Setting up the 1680/90/900 Analyzer

The 1680/90/900 Analyzer is a PC based application that requires a PC running the Windows OS with the Agilent logic analyzer software installed or a 16900 frame.

Before installing the protocol decoder for the PCIX protocol on a PC you **must** install the Agilent logic analyzer software. Once the Agilent logic analyzer software is installed, you can install the FS3012 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the .exe file on the CD-ROM disk and then double click the .exe file name from within the File Explorer navigation panel.

**The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe Adapter is used.**

## 1680/90/900 Licensing

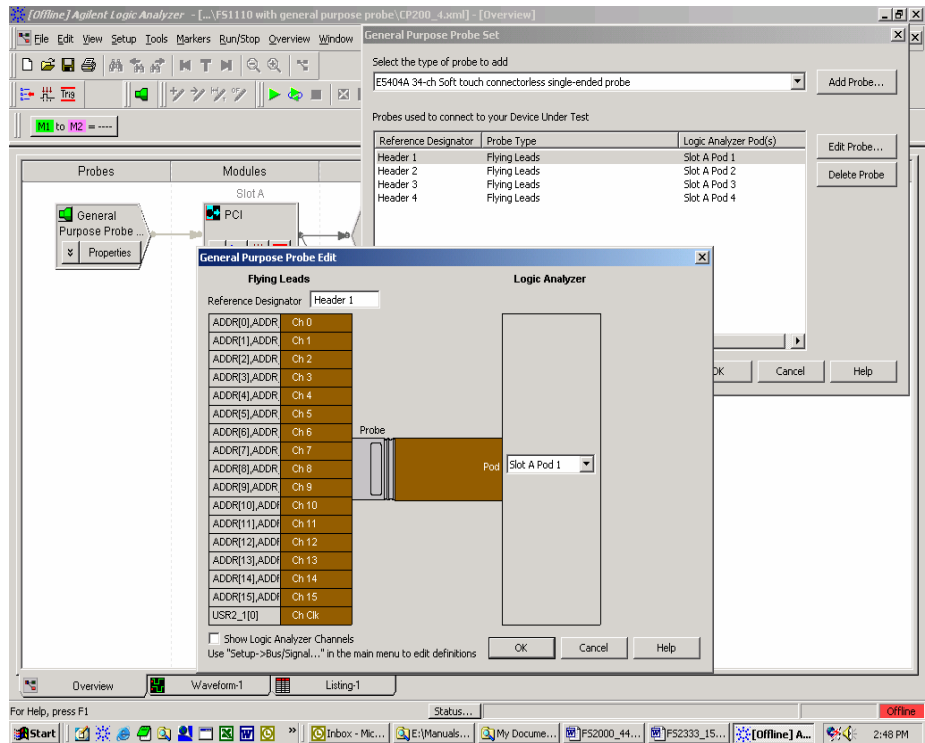
The PCIX Inverse Assembler is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

## Loading 1680/90/900 configuration files and the General Purpose Probe feature

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

Once you have loaded a configuration file on the 169xx machine you can find out how to attach the logic analyzer cables to the probe by going to the workspace and selecting Properties on the General Purpose Probe tool icon that appears before the logic analyzer icon. Once you click on the Properties box a new window will appear showing which analyzer pod attaches to which probe cable.

The figure below may differ from your display; this is an example of how the display looks in general.



## Configuration Files

Refer to the table below for a list of analyzers and corresponding configuration files.

167xx Analyzer	169xx Analyzer	File name for State/Timing	Configuration
16555/6/7		CP312_3	64 bit 2 card
16550, 16711/2		CP312_5	32/64 bit 1 card
16715/6/7/9, 16740/1/2, 16750/1/2	1680/90, 16750/1/2, 1695x, *1691x	CP312_1	64 bit 2 card  *1691x only requires 1 card for 64 bit.
167XX	1680/90, 16750/1/2, 1695x	CP312_2	32 bit 1 card
16555/6/7		CP312_4	32 bit 1 card

## Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a \*.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

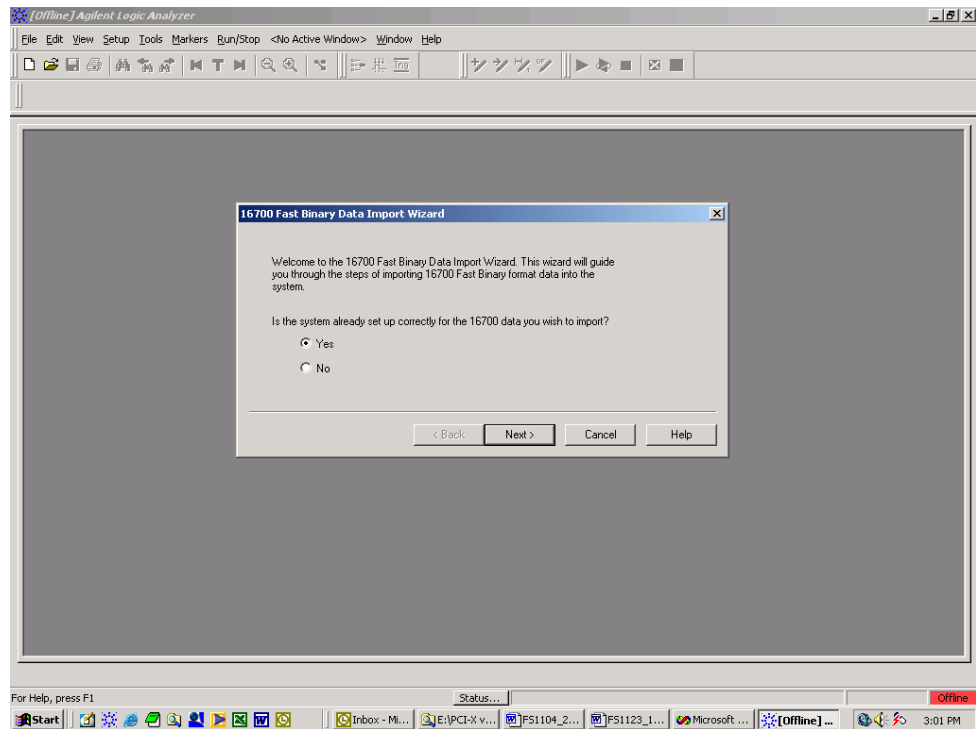
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may buy additional licenses, please contact FuturePlus sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up 1680/90/900 analyzer". Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

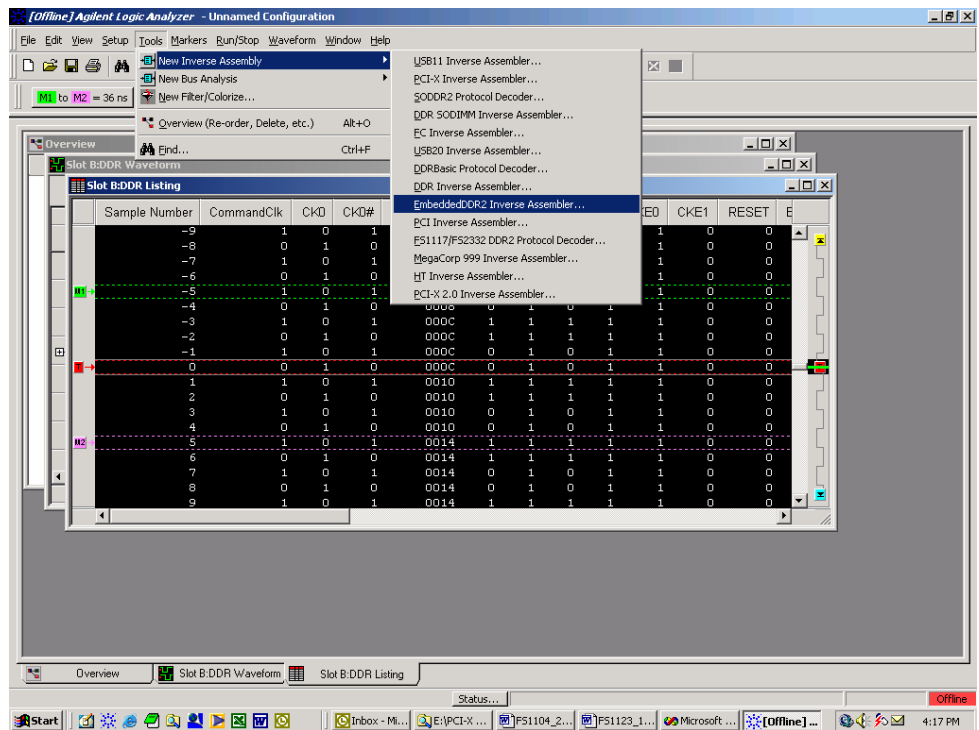
For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select “yes” when it asks if the system is ready to import 16700 data.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.



After the decoder has loaded, select Preferences if required, from the overview screen and set the preferences to their correct value in order to decode the trace properly. This is a general requirement, some decoders do not have preferences, if this is the case then no preference setting is necessary.

## The Format Menu

The FS3012 diskette sets up the format menu as shown in the following table. This format is the same for both Timing and State Analysis.

Label	Clk Input	POD 6	POD 5	POD 4	POD 3	POD 2	POD 1
STAT				14,13, 12,11 ,6:3, 1,0	9:6,5, 4		
ADDR						15-0	15-0
ADDR_B		15-0	15-0				
INTD_A					14-11		
RESET					10		
C/B3_0					9-6		
C/B7_4				6-3			
DATA						15-0	15-0
DEVSEL					5		
STOP					4		
LOCK					3		
PERR					2		
SERR					1		
PAR					0		
PAR64				2			
SD/SB0				8-7			
ACK/RQ				1-0			
IRDY				12			
FRAME				13			
TRDY				14			
PCICLK	L						
IDSEL				9			
GNT				10			
M66EN				15			
CYCLE				14-12	9-4		
REQ				11			
PCIXCAP	M						

### ***The STAT variable***

The STAT variable is used by the PMC inverse assembler to decode PMC bus transactions. *It should not be changed or deleted from the format menu.* The signals that make up the STAT variable are listed in the following table. The STAT variable can be useful to set up SYMBOLS since it contains all of the key PMC control and status signals.

<b>STAT Variable</b>	<b>PMC Bus Signal Name</b>
<b>Bit 15</b>	ACK64#
<b>Bit 14</b>	REQ64#
<b>Bit 13</b>	REQ#
<b>Bit 12</b>	C/BE7#
<b>Bit 11</b>	C/BE6#
<b>Bit 10</b>	C/BE5#
<b>Bit 9</b>	C/BE4#
<b>Bit 8</b>	C/BE3#
<b>Bit 7</b>	C/BE2#
<b>Bit 6</b>	C/BE1#
<b>Bit 5</b>	C/BE0#
<b>Bit 4</b>	FRAME#
<b>Bit 3</b>	IRDY#
<b>Bit 2</b>	TRDY#
<b>Bit 1</b>	STOP#
<b>Bit 0</b>	DEVSEL#

### ***The ADDR, ADDR\_B and DATA variables***

The ADDR and ADDR\_B variables are AD[63-0] bits of the PMC bus. The DATA variable is a dummy variable that needs to be defined for the PMC inverse assembler. *These variables should not be changed or deleted from the format Menu.*

**The CYCLE variable**

The CYCLE variable is made up of the following PMC signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL# and STOP#. This variable has 30 symbols defined that can be used to help make triggering, timing analysis and pattern filtering (16505A) easier. The following lists the bit pattern and the corresponding symbol.

Symbol	IRDY#	FRAME#	DEVSEL#	TRDY#	CBE3-0#	STOP#
INTACK	1	0	1	1	0000	1
SPEC_CYC	1	0	1	1	0001	1
I/O_RD	1	0	1	1	0010	1
I/O_WR	1	0	1	1	0011	1
RESVRD	1	0	1	1	0100	1
RESVRD	1	0	1	1	0101	1
MEM RD DWORD	1	0	1	1	0110	1
MEM WR	1	0	1	1	0111	1
ALIAS MEM RD BL	1	0	1	1	1000	1
ALIAS MEM WR BL	1	0	1	1	1001	1
CONF RD	1	0	1	1	1010	1
CONF WR	1	0	1	1	1011	1
SPLIT COMPLETE	1	0	1	1	1100	1
DAC	1	0	1	1	1101	1
MEM RD BL	1	0	1	1	1110	1
MEM WR BL	1	0	1	1	1111	1
IO XACTION	1	0	1	1	001X	1
MEM XACTION	1	0	1	1	011X	1
CONFIG XACTION	1	0	1	1	101X	1
ADDR CYCLE	1	0	1	1	XXXX	1
DATA XFER	0	X	0	0	XXXX	1
INITIATOR TERM	0	0	1	1	XXXX	1
SNGL DATA XFER	0	X	1	0	XXXX	0
STOP NEXT ADB	0	X	0	0	XXXX	0
RETRY	0	X	0	1	XXXX	0

Symbol	IRDY#	FRAME#	DEVSEL#	TRDY#	CBE3-0#	STOP#
TARGET ABORT	1	X	1	1	XXXX	0
IDLE	1	1	X	X	XXXX	X
SINGLE DATA DISC	0	0	1	0	XXXX	0
TARGET RESPONSE	0	0	0	1	XXXX	1
SPLIT RESPONSE	0	0	1	0	XXXX	1

# State Analysis

This chapter explains how to configure the FS3012 to perform state analysis on the PMC Local Bus. The configuration software on the flexible diskette sets up the format specification menu of the logic analyzer for compatibility with the PMC Local Bus. The next chapter explains how to configure the FS3012 to perform timing analysis.

The FS3012 Analysis Probe interface does not require that a PMC add-in card be installed in the FS3012 card edge extender connector.

## Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the FS3012 module.

1. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe interface cable headers. See page 9 of this manual for details.
2. Install the FS3012 module into a slot in the target PMC Local bus.
3. Load the logic analyzer configuration file by loading the appropriate file. See page 13 of this manual for details.

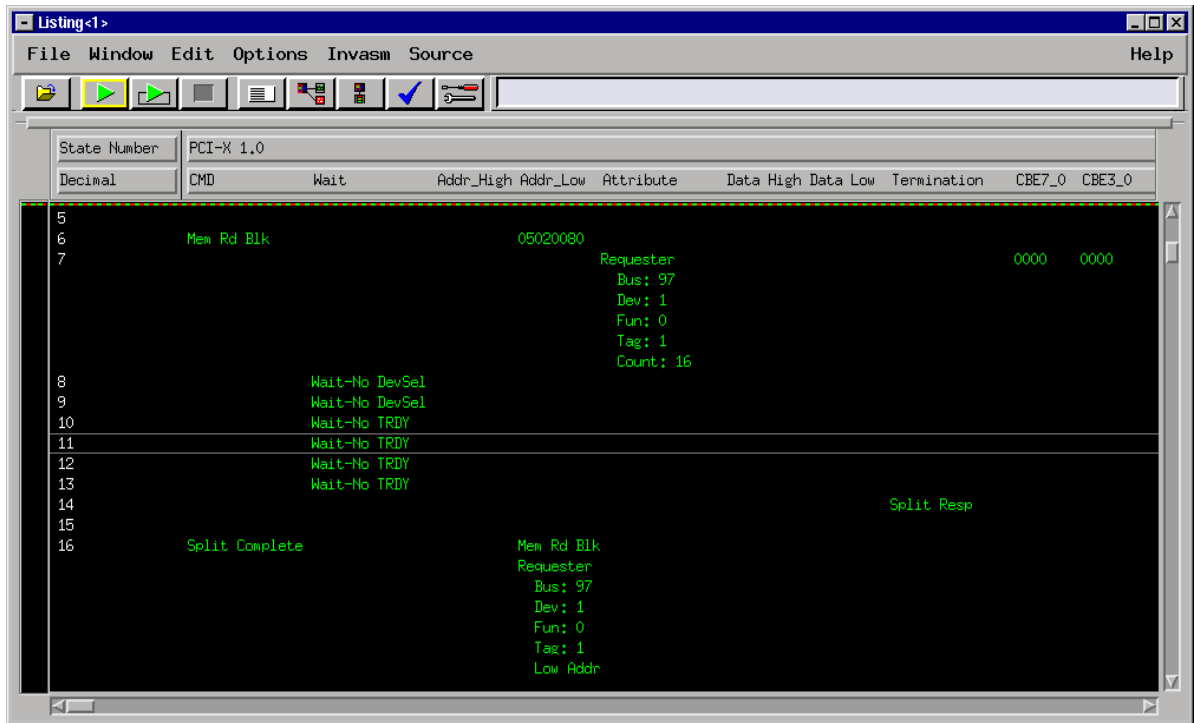
## Acquiring Data

Touch RUN and as soon as there is activity on the bus and the trigger condition has been satisfied, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

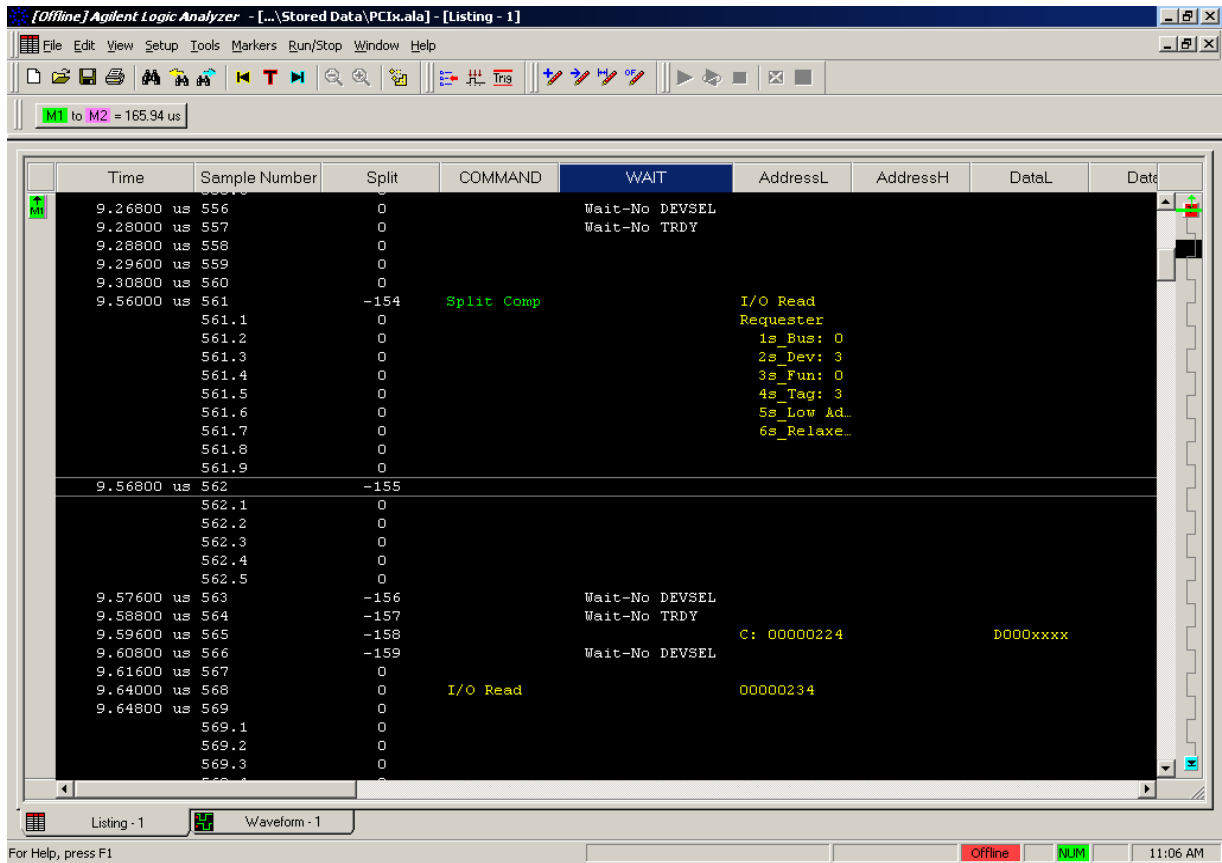
The logic analyzer will flash "Slow or Missing Clock" if it does not see the PMC signal CLK toggling.

## The State Display

Captured data is as shown in the following figures. The following figures display the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PMC Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PMC bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.



16700 Display



## 1680/90/900 Display

### Error Messages

The following error messages are reported by the PMC inverse assembler.

#### ERROR-NO DEVICE SELECTED

This error is displayed during a non special cycle data phase when IRDY and TRDY are asserted and DEVSEL is not asserted.

#### ERROR DEVSEL ASSERTED

This error is displayed during a special cycle data phase if DEVSEL is asserted.

#### SYSTEM ERROR

This error is displayed anytime SERR# is asserted.

### **1680/90/900 Errors:**

XXX input label could not be attached to.

This error is displayed when the 1680/90 IA is being started and a failure occurs during the creation of an input label/column.

XXX: input label invalid Min/Max parameters.

This error is displayed during the creation of a label/column. The IA expects the label/column to fall within a min/max number of bits which has been violated.

XXX: Failed to unattach from label

This error is displayed when the 1680/90 IA is being exited and a failure occurs during the label/column destruction

XXX: output label could not be created.

This error is displayed when the 1680/90 IA is being started and a failure occurs when an output label/column is being constructed

XXX: symbol could not be created.

This error is displayed when the 1680/90 IA is being started and a failure occurs when an output or input label/column symbol could not be created

XXX: Could not save Label

This error is displayed when the 1680/90 IA configuration file is being created and/or updated. The configuration data for the specified label could not be written to the file and thus will be lost.

XXX: Could not load Label

This error is displayed when the 1680/90 IA configuration file is being read. The configuration data for the specified label could not be read to the file and thus will be lost.

## Filtering

For **16700** users, select filter under INVASM in the state listing.

For **1680/90/900** users, select the Filter/Colorization pull down menus in the state listing and create a filter (downstream) tool.

The 1680/90/900 IA allows filtering just like the 16700/702 environments. You may filter on any label, when using the filter tags label you can select symbols to make choosing transactions easier. To create a filter, choose Tools->New->Filter/Colorize. Then fill in the information on the window that opens up. You must create a new filter for each item you want filtered. To remove filters that you no longer want, go to Tools->Overview and then choose the filter you want removed and click Delete.

# Timing Analysis

## Installation Quick Reference

Since the FS3012 interface contains only passive matching terminators it introduces negligible skew to the PMC Local Bus signals.

The following procedure describes the major steps required to perform timing analysis measurements with the FS3012 module.

1. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe cable headers. See page 9 of this manual for details.
2. Install the FS3012 module into a slot in the target PMC Local bus.
3. Load the logic analyzer configuration file by loading the appropriate file from the Analysis Probe interface diskette.
4. Once the appropriate configuration file has been loaded, double click on the logic analyzer icon and go to the sampling tab. Change from state mode to timing mode. You are now ready for timing analysis.

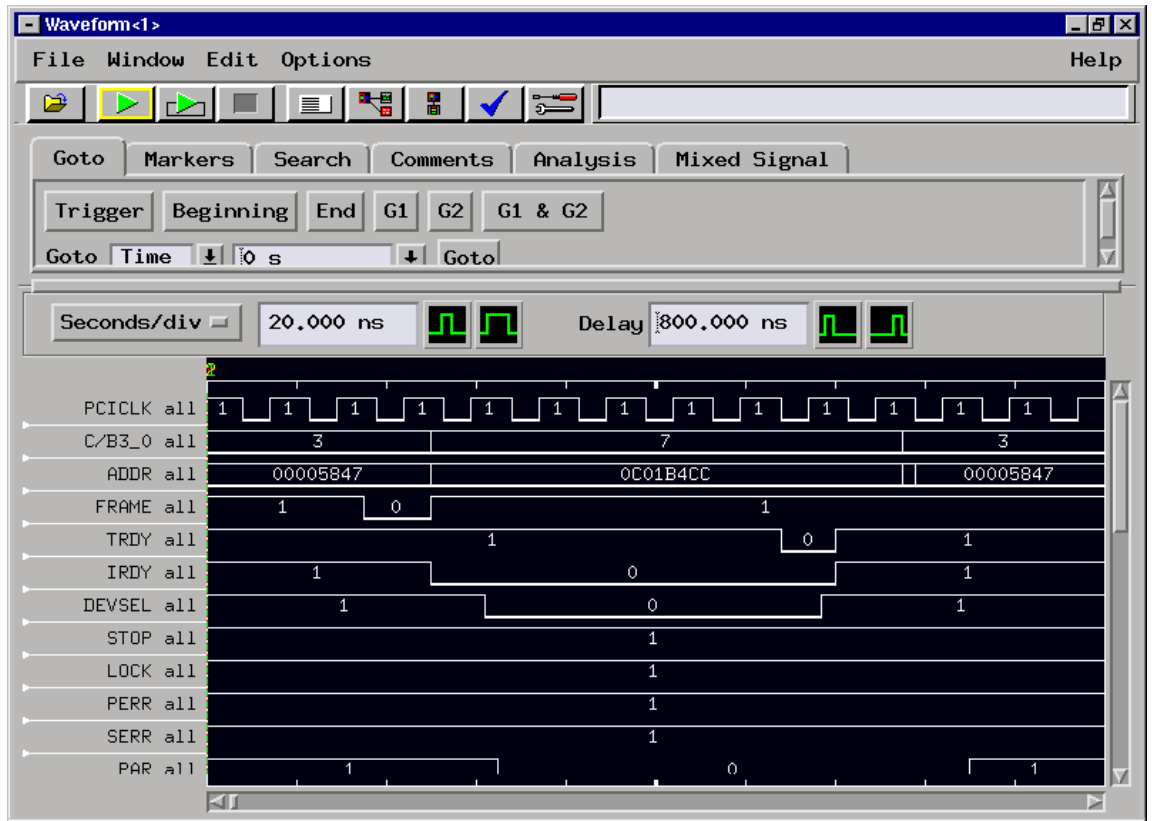
## Acquiring Data

Touch RUN and, as soon as there is activity on the bus and the trigger condition has been satisfied, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Waiting for Trigger" if the trigger specification has not been met.

# The Waveform Display

Captured data is displayed as shown in the following figure.



# General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS3010 module.

## **Characteristics**

The following operating characteristics are not specifications, but are typical operating characteristics for the FS3010 module.

### ***Analysis Probe Interface Compatibility***

64 bit PMC Local bus accepting the IEEE 1386 connector. All PMC local bus ground pins are connected to the ground plane of the FS3012 module. Maximum recommended clock speed of 66 MHz

### ***Bus Extender Connector***

This connector is a universal 64 bit connector. All of the signals from the PMC bus are routed to the extender connector. Users are advised to ensure that the PMC card under test matches the voltage levels of their Host board.

### ***Turret Ground Points***

2 Turret style ground points are provided for convenient attachment to ground. These are labeled P1 and P2.

### ***Fuse Protection***

Self-resetting polymer fuses are provided on the PMC extender to help protect against over-current conditions on the +5V, +3.3V, +12V, and -12V power rails. The fuse current limits are as follows:

+3.3V: 8 Amps Trip, 4 Amps hold

+5V: 4 Amps Trip, 2 Amps hold

+12V: 1.5 Amps Trip, 0.75 Amps hold

The term "TRIP" refers to the current at which a current-trip is guaranteed to occur. The term "HOLD" is the maximum current allowed without tripping the fuse.

### ***PCI-X Specification***

The PCI-X Local Bus Specification Revision 1.0a, IEEE P1386.1 Specification.

**Power Requirements**

The FS3012 Analysis Probe logic contains no active components and therefore requires no power. The PMC add-in card installed in the FS3012 can draw power from the +/-12V, 3.3V, 5V and the VI/O pins as if it were installed without the FS3012.

**Logic Analyzer Required**

1680/90, 1655x, 167xx, 169xx.

The Analysis Probe interface uses 6 cable headers.

**Minimum Clock Period (State)**

Not limited by the Analysis Probe interface logic. Clocking is specified by the logic analyzer.

**Signal loading**

The FS3012 Analysis Probe logic presents one 8pf/90k ohm load on each PMC bus signal. The extender connector adds an additional 2pf. The etch and associated via's add approximately 1pf of additional capacitance.

**Etch length**

The etch length from the host card connector to the extender card edge connector is approximately 10 inches on all signals. The length of the signals has been controlled to minimize signal-to-signal skew to less than 500 ps.

**Operations**

All PMC Local Bus operations supported by the hardware and the inverse assembler.

**Environmental Temperature**

Operating: 0 to 55 degrees C (+32 to +131 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

**Altitude**

Operating: 4,600m (15,000 ft)

Non operating: 15,300m (50,000 ft)

**Humidity**

Up to 90% non condensing. Avoid sudden, extreme temperature changes which would cause condensation on the FS3012 module.

**Testing and Troubleshooting**

There are no automatic performance tests or adjustments for the FS3012 module. If a failure is suspected in the FS3010 module contact the factory or your FuturePlus Systems authorized distributor.

**Servicing Number of Probes Used**

The repair strategy for the FS3012 is module replacement. However, if parts of the FS3012 module are damaged or lost contact the factory for a list of replacement parts.

## Signal Connections

The FS3012 contains 6, forty pin headers for connection to Agilent logic analyzers, as well as, 80 test points for scope or flying lead logic analyzer connection.

### *Test Point pinout*

The 80 pin 2mm connector labeled “JP1” provides access to all 64 AD signals, power supply voltages and their current draw per the following table:

Test Point Header and Pin number	PMC Signal name	Test Point Header and Pin number	PMC Signal name
JP1 Header pin 1	AD0	JP1 Header pin 2	AD32
3	AD01	4	AD33
5	AD02	6	AD34
7	AD03	8	AD35
9	AD04	10	AD36
11	AD05	12	AD37
13	AD06	14	AD38
15	AD07	16	AD39
17	AD08	18	AD40
19	AD09	20	AD41
21	AD10	22	AD42
23	AD11	24	AD43
25	AD12	26	AD44
27	AD13	28	AD45
29	AD14	30	AD46
31	AD15	32	AD47
33	AD16	34	AD48
35	AD17	36	AD49
37	AD18	38	AD50
39	AD19	40	AD51

Test Point Header and Pin number	PMC Signal name	Test Point Header and Pin number	PMC Signal name
41	AD20	42	AD52
43	AD21	44	AD53
45	AD22	46	AD54
47	AD23	48	AD55
49	AD24	50	AD56
51	AD25	52	AD57
53	AD26	54	AD58
55	AD27	56	AD59
57	AD28	58	AD60
59	AD29	60	AD61
61	AD30	62	AD62
63	AD31	64	AD63
65	POD1-3	66	POD2-3
67	POD3-7	68	PCIXCAP
69	GND	70	GND
71	V+VIO	72	GND
73	V+12	74	I+12
75	V-12	76	I-12
77	V+5	78	I+5
79	V+3.3	80	I+3.3

### Current Measuring Capabilities

The 64-bit PMC analysis probe has provision for measuring current on +12, -12, +5, and 3.3V supplies. The voltage across a 0.01 ohm resistor in series with each supply is amplified by a differential amplifier and the resulting voltage appears on pins on the 2mm header.

The amplifier gain is set at 100x, and therefore the voltage measurement represents the number of amps being drawn by the associated supply (gain is 1 volt per amp). Also, a single-pole low-pass filter is incorporated in the amplifier with a cutoff frequency of approximate 1 KHz. Thus, transient current draw on the PMC is effectively filtered out of the current measurement.

There is an intrinsic "offset" characteristic of the amplifiers, which must be accounted for to achieve accurate measurements. The user first measures this offset voltage with no PMC installed (i.e., the "no load" condition), and then measures the voltage with the PMC installed (i.e., the "load" condition). The arithmetic difference between the no-load and load voltages is the current drawn by the board.

**Analysis Probe interface  
pinout**

The FS3012 module monitors signals for both state and timing analysis. The below figure displays how the cable headers are numbered.

The following tables list the FS3012 cable headers and the corresponding PMC Local Bus signals after these signals have been terminated by the 90K ohm/10pf terminators.

39 37 35 33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
40 38 36 34 32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PMC Signal name
Header 1 pin 3	CLK/16	
5	no connect	
7	15	AD15
9	14	AD14
11	13	AD13
13	12	AD12
15	11	AD11
17	10	AD10
19	9	AD09
21	8	AD08
23	7	AD07
25	6	AD06
27	5	AD05
29	4	AD04
31	3	AD03
33	2	AD02
35	1	AD01
37	0	AD00

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PMC Signal name
Header 2 pin 3	CLK/16	
5	no connect	
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PMC Signal name
Header 3 pin 3	CLK/16	PCIXCLK
5	no connect	
7	15	
9	14	INTD#
11	13	INTC#
13	12	INTB#
15	11	INTA#
17	10	RST#
19	9	C/BE3#
21	8	C/BE2#
23	7	C/BE1#
25	6	C/BE0#
27	5	DEVSEL#
29	4	STOP#
31	3	LOCK#
33	2	PERR#
35	1	SERR#
37	0	PAR

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PMC Signal name
Header 4 pin 3	CLK/16	PCIXCAP
5	no connect	
7	15	M66EN
9	14	TRDY#
11	13	FRAME#
13	12	IRDY#
15	11	REQ#
17	10	GNT#
19	9	IDSEL
21	8	SD
23	7	SB0#
25	6	C/BE7#
27	5	C/BE6#
29	4	C/BE5#
31	3	C/BE4#
33	2	PAR64
35	1	ACK64#
37	0	REQ64#

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PMC Signal name
Header 5 pin 3	CLK/16	
5	no connect	
7	15	AD47
9	14	AD46
11	13	AD45
13	12	AD44
15	11	AD43
17	10	AD42
19	9	AD41
21	8	AD40
23	7	AD39
25	6	AD38
27	5	AD37
29	4	AD36
31	3	AD35
33	2	AD34
35	1	AD33
37	0	AD32

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PMC Signal name
Header 6 pin 3	CLK/16	
5	no connect	
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48