

FuturePlus Systems Corporation



Agilent Technologies
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FS2102 and FS2103

Users Manual

For Agilent Logic Analyzers

Revision 1.6

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For products returned to FuturePlus Systems for warranty service, the Buyer shall prepay shipping charges to FuturePlus Systems and FuturePlus Systems shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to FuturePlus Systems from another country.

FuturePlus Systems warrants that its software and hardware designated by FuturePlus Systems for use with an instrument will execute its programming instructions when properly installed on that instrument. FuturePlus Systems does not warrant that the operation of the hardware or software will be uninterrupted or error-free.

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Introduction

The PCI State Analysis Probe module provides a complete interface between any PCI add-in slot and Agilent Logic Analyzers. The on board logic interface buffers latch all signals (except the clock) and decode all PCI cycle types and transactions.

The PCI State Analysis Probe is a bus monitor which does not assert any signals on the PCI bus. The etch from the PCI local bus is routed directly from the PCI local bus to the extender card connector. Although the etch is connected to the input of the PCI State Analysis Probe input buffers, the extender card connector is NOT buffered from the PCI local bus.

The configuration software on the diskette sets up the format, configuration and trigger specification menu of the logic analyzer for compatibility with your PCI bus. When the configuration file is loaded, an inverse assembler is also loaded which decodes PCI transactions into easy to read mnemonics.

This manual is organized to help you quickly find the information you need.

How to Use This Manual

- **Analyzing the PCI Local Bus** chapter introduces you to the PCI State Analysis Probe and lists the minimum equipment required and accessories supplied for PCI bus analysis.
- The **State Analysis** chapter explains how to configure the PCI State Analysis Probe to perform state analysis on your PCI bus.
- The Timing Analysis chapter briefly explains how to use the FS2102/3 for timing analysis.
- The **General Information** chapter provides some general information including the operating characteristics for the PCI State Analysis Probe module and the cable header pinout.

Analyzing the PCI Local Bus

Duplicating the Master Diskette

This chapter introduces you to the PCI State Analysis Probe and lists the minimum equipment required and accessories supplied for PCI Local Bus analysis.

Before you use the PCI State Analysis Probe software, make a duplicate copy of the master diskette. Then store the master diskette and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the diskette wears out, is damaged, or a file is accidentally deleted.

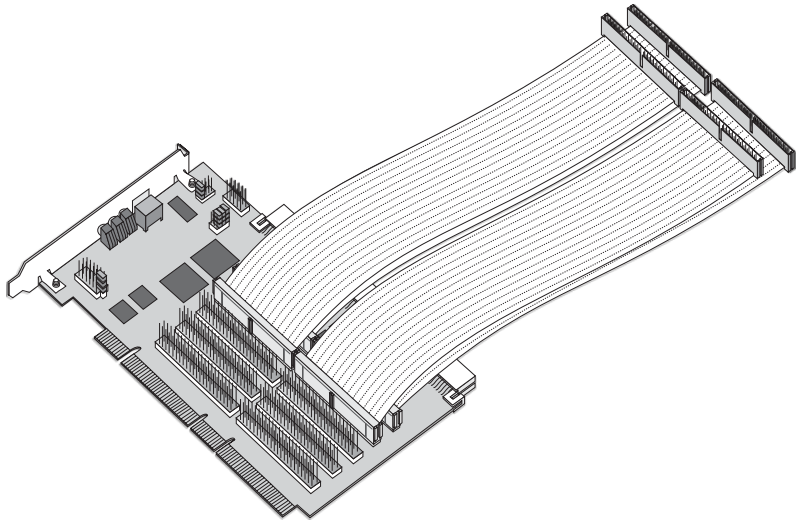
To make a duplicate copy, use the Duplicate Diskette operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Accessories Supplied

The PCI State Analysis Probe product consists of the following accessories:

- The State Analysis Probe interface hardware, which includes the interface circuit module.
- The inverse assembly and configuration software on a 3.5 inch diskettes.
- 10 cables
- This operating manual

The PCI State Analysis Probe module



Minimum Equipment Required

The minimum equipment required for analysis of a PCI Local Bus consists of the following equipment:

- 1660A/C, 1661A/C, 1662A/C, 16550A, 16554A, 16555A, 16556A, 16557A, 1670A, 1671A, 1672A, 16710A, 16711A, 16712A
- The PCI State Analysis Probe Product
- A PCI target bus

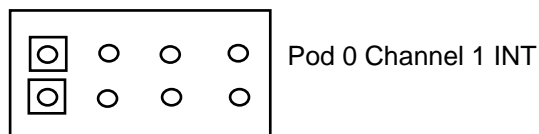
Signal Naming Conventions

This operating manual uses the same signal notation as the PCI LOCAL BUS SPECIFICATION - REVISION 2.2. That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

Viewing the interrupts

Pod 1 channel 0 can be configured to view any one of the four PCI interrupts. The interrupt jumper is configured at the factory on INTA. Move the jumper so that it corresponds to the desired interrupt and that interrupt line will be routed to POD 1 channel 0. The jumper and interrupt stake pins are clearly labeled.

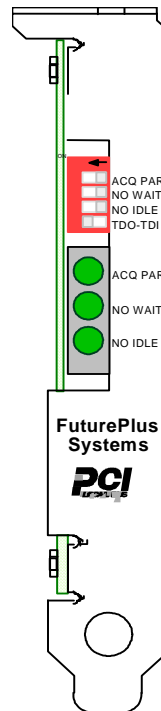
Interrupt Jumper



I	I	I	I
N	N	N	N
T	T	T	T
A	B	C	D

Configuring the front panel switches and LEDs

Switch	Setting	LED
ACQ PAR	Parity bit and PERR acquired	ON
ACQ PAR	Parity bit and PERR not acquired	OFF
No Wait	No Wait cycles acquired	ON
No Wait	All Wait cycles acquired	OFF
No Idle	No Idle cycles acquired	ON
No Idle	All Idle cycles acquired	YES
TDO/TDI	TDO connected to TDI	No LED, switch in rightmost position
TDO/TDI	TDO not connected to TDI	No LED, switch in leftmost position



PCI State Analysis Probe front panel

Powering the PCI State Analysis Probe

The active circuitry on the PCI State Analysis Probe module gets its power from the logic analyzer PODs. No power is taken from the target PCI system. **Please Note: If the State Analysis Probe is plugged into the PCI bus without having the logic analyzer powered and connected the input buffers on the State Analysis Probe will create a low impedance path to ground thus inhibiting the PCI local bus and any card in the extender card connector from working.**

The Logic analyzer must be connected and powered on for the PCI State Analysis Probe to work properly.

The PCI State Analysis probe has on-board circuitry such that if it is removed from the target PCI system while the logic analyzer is powered on it will disconnect power to it's on-board components (except U52 and U53). However, care must still be taken since power from the logic analyzer is still present.

Connecting to the PCI State Analysis Probe

The following explains how to connect the logic analyzer to the PCI State Analysis Probe:

1. Remove the probe tip assemblies from the logic analyzer cables.
2. Plug the logic analyzer cables into the PCI State Analysis Probe cable headers as shown in the appropriate following tables.

Multiplexed versus Demultiplexed

The PCI Local Bus specification specifies that the AD lines and the C/BE lines carry different information at different times. This is referred to as multiplexed. Loading in the configuration file that indicates “demultiplexed” will assign two extra PODS for the address. The address is latched and then incremented to the logic analyzer during a burst transaction.

Please note that the C/BE lines have been demultiplexed on the PCI State Analysis Probe. Thus the command is held through out the transaction and no additional clocking or pods is required. The latched command L_CMD signals are on pod 1 channels 10-7.

32 bit PCI Demultiplexed

Logic Analyzer	PCI State Analysis Probe	Comment
Master POD 1	Header 1	
POD 2	Header 2	
POD 3	Header 3	
POD 4	Header 4	
POD 5	Header 5	1655x expander card POD 1
POD 6	Header 6	1655x expander card POD 2

32 bit PCI Multiplexed

Logic Analyzer	PCI State Analysis Probe	Comment
Master POD 1	Header 1	
POD 2	Header 2	
POD 3	Header 3	
POD 4	Header 4	

64 bit PCI Demultiplexed

Logic Analyzer	PCI State Analysis Probe	Comment
Master POD 1	Header 1	
POD 2	Header 2	
POD 3	Header 3	
POD 4	Header 4	
POD 5	Header 5	1655x expander card POD 1
POD 6	Header 6	1655x expander card POD 2
POD 7	Header 7	1655x expander card POD 3 16550 expander card Pod 1
POD 8	Header 8	1655x expander card POD 4 16550 expander card Pod 2

PCI Compliance Violation Detection

These violations are derived from the PCI Compliance Checklist and the PCI Specification. They are sent as individual signals to the logic analyzer on PODs 9 and 10. If any of these errors occur the signal ANYERROR on POD 2 will assert and will be clocked to the logic analyzer by the master clock. The error signals, the encoded error summary and the signal ANYERROR will be asserted for 1-2 PCI clock tics.

Logic Analyzer	PCI State Analysis Probe	Comment
Master POD 1	Header 9	Compliance violations
POD 2	Header 10	Compliance violations

There are additional signals from the Violation CPLD that are available to be used for additional compliance violations. They are currently reserved for future use. The compliance violations detected by the FS2102 and FS2103 are listed below

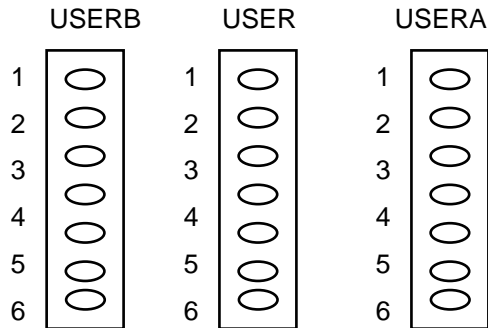
- ERROR 0: FRAME MUST BE DEASSERTED AS SOON AS POSSIBLE AFTER STOP IS ASSERTED
- ERROR 1: FAST BACK TO BACK ONLY AFTER WRITE OR MASTER ABORT
- ERROR 2: IRDY ASSERTED IN THE ADDRESS PHASE
- ERROR 3: FRAME CANNOT BE DEASSERTED UNLESS IRDY IS ASSERTED
- ERROR 4: IRDY MUST BE DEASSERTED AFTER LAST TRANSFER OR WHEN FRAME IS DEASSERTED
- ERROR 5: IRDY MUST NOT GO LOW WHEN FRAME IS HIGH
- ERROR 6: IRDY CANNOT DEASSERT UNTILL DATA PHASE COMPLETE
- ERROR 7: NO DEVSEL ON RESERVED OR SPECIAL CYCLE
- ERROR 8: ONCE DEVSEL HAS BEEN ASSERTED IT CANNOT BE DEASSERTEED UNTIL DATA PHASE
- ERROR 9: DEVSEL MUST BE DEASERTEED AFTER THE LAST RELEASE
- ERROR10: DEVSEL MUST BE ASSERTED WITH OR PRIOR TO TRDY
- ERROR 11: ONCE TRDY ASSERTS IT CANNOT CHANGE UNTIL DATA PHASE
- ERROR 12: DEVSEL MUST BE ASSERTED WITH OR PRIOR TO STOP
- ERROR 13: STOP MUST REMAIN ASSERTED UNTIL FRAME IS DEASSERTED
- ERROR 14 : PERR MUST NEVER BE ASSERTED TWO CLOCKS AFTER ADDRESS PHASE OR SPECIAL CYCLE
- ERROR 15: TRDY VALID IN COMMAND CYCLE
- ERROR 16: TRDY VALID IN A IDLE CYCLE
- ERROR 17: DEVSEL ASSERTED IN COMMAND CYCLE
- ERROR 18: FRAME NOT ASERTEED ON CYCLE FOLLOWING DAC
- ERROR 19: STOP ASSERTED DURING IDLE CYCLE
- ERROR 20: NO TRDY IN THE TURN AROUND PHASE

USER PINS

PCI State Analysis Probe Header 10 contains 6 *User Defined* pins. These user pins are available on the logic analyzer on POD 10 channels 15 through 10. These pins are clearly marked in the lower left hand corner of the board.

Additional Grant lines

USERA pins 2 and 3 are used to attach additional PCI GNT# signals to the logic analyzer. Once these GNT# signals have been manually connected to USERA2 and 3 a jumper should be placed across USERB 2 and 3 to USER 2 and 3 respectively. These latched grant signals can be viewed by the logic analyzer on POD 10 channels 11 and 12.



The CYCLE CPLD will provide the latching feature so that the GNT# signal fed to the logic analyzer will be held throughout the transaction. This will provide for easy triggering and performance monitoring.

USERB signals are tied through a zero ohm resistor to the VIOLATION CPLD for additional programming by the factory and are reserved.

PME

The PME signal from the PCI bus is on J9 which is located near the USER pins in the lower left hand corner of the module. It is by default jumpered to USER1 and appears in the format menu as PME on POD 10 channel 10.

A Summary of the USER pins appears in the table below.

User Pin	Comment
1	Set at the factory to connect to the PME signal. This pin goes to the logic analyzer on POD 10 channel 10. The jumper can be removed and the user can attach any desired signal to USER1. This pin is terminated for direct connection to the logic analyzer by the 90K ohm/10pf terminators.
2	This pin goes to the logic analyzer on POD 10 channel 11. The user can attach any desired signal to USER2. This pin is terminated for direct connection to the logic analyzer by the 90K ohm/10pf terminators. For viewing the latched GNT line attached to USERA2 place a jumper between USERB2 and USER2.

User Pin	Comment
3	This pin goes to the logic analyzer on POD 10 channel 12. The user can attach any desired signal to USER3. This pin is terminated for direct connection to the logic analyzer by the 90K ohm/10pf terminators. For viewing the latched GNT line attached to USERA3 place a jumper between USERB3 and USER3.
4	This pin goes to the logic analyzer on POD 10 channel 13. The user can attach any desired signal to USER4. This pin is terminated for direct connection to the logic analyzer by the 90K ohm/10pf terminators.
5	This pin goes to the logic analyzer on POD 10 channel 14. The user can attach any desired signal to USER5. This pin is terminated for direct connection to the logic analyzer by the 90K ohm/10pf terminators.
6	Reserved for factory use

Installing the PCI State Analysis Probe

The PCI State Analysis Probe can be installed in any slot of the PCI Local bus. The following steps explain how to install the PCI State Analysis Probe into the PCI Local bus.

1. Install the logic analyzer cables as described in the previous section.
2. Power off the PCI target. Align the PCI State Analysis Probe with the appropriate slot on the target system and plug the module into the PCI connector. Power on the logic analyzer and then power on the target.

If your PCI Local bus is 32 bits the upper portion of the edge connector will not be inserted into any connector. This will not affect the modules operation on a 32-bit PCI Local bus.

How to install a PCI add-in card into the extender card connector

The card edge connector of the PCI State Analysis Probe module can accommodate one 32 or 64 bit 5V(FS2103) OR 3.3V (FS2102) PCI add in card. The extender card connector is a 3.3V connector if you have a FS2102 or a 5V connector if you have a FS2103.

Simply align the module with the connector and gently push the module in until it is seated in the connector. There is sufficient clearance for the add-in card front plate. The PCI State Analysis Probe/PCI add-in card combination can then be installed in any slot of the PCI Local bus. For mechanical stability the PCI State Analysis Probe front plate should be secured to the PCI target system chassis.

When removing the PCI add-in card from the card edge extender connector grasp the PCI State Analysis Probe with one hand and the PCI add-in card with the other. Gently rock the PCI add-in card until it is free from the connector.

WARNING: DO NOT install an add-in card into the PCI State Analysis Probe extender card connector while power is applied to the PCI State Analysis Probe or power is applied to the target.

Operation of the PCI add-in card

The nature of an extender card is that it extends the etch length of the bus. Due to the sensitivity of most PCI designs, extending the etch length can interfere with the PCI add-in card operation. Operation of the PCI add-in card when installed in the card edge extender connector is not guaranteed. Please check your system design if you experience failures due to poor signal fidelity.

The etch from the PCI local bus is routed directly from the PCI local bus to the extender card connector. Although the etch is connected to the input of the PCI State Analysis Probe input buffers, the extender card connector is NOT buffered from the PCI local bus.

Please Note: If the State Analysis Probe is plugged into the PCI bus and the logic analyzer is not powered up, the input buffers on the State Analysis Probe will create a low impedance path to ground thus inhibiting the PCI local bus and any card in the extender card connector from working.

The Extender Card Connector

The PCI bus is extended up from the gold fingers to the to the extender card connector and then to the input of the IDT162543 buffers. The etch is extended approximately 5 inches from the gold fingers and is on the inner most layer of the board.

The PCI State Analysis Probe module itself is a universal card. It can operate in either a 5V or 3V PCI system.

Setting up the 16600/16700 Analyzer

The 16600/16700 requires a special install procedure to install the PCI software. To accomplish this, insert the diskette labeled **16600/16700 PCI Analysis Probe Software for the FS2102/3** into the 16600/700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY* once the title appears (FS2102_3 FS2102 PCI Inverse Assembler) select it and then and then select *INSTALL*. **This procedure does not need to be repeated. It only needs to be done the first time the PCI Analysis Probe is used.**

When this has completed load the appropriate configuration file from the /configs/FuturePlus/FS2102_3 directory. Refer to the **logic analyzer configuration** section of this manual for a list of analyzers and corresponding configuration files.

Setting up Analyzers installed in the 16500 mainframe and portable logic analyzers

The logic analyzer can be configured for PCI analysis by loading the PCI configuration file. Loading this file will load the PCI Local bus inverse assembler and configure your logic analyzer. To load the configuration and inverse assembler:

1. Install the appropriate FS2102/3 16500 PCI State Analysis Probe software flexible diskette in the disk drive of the logic analyzer. **Disk 1 contains the files for the 16550 and 166x logic analyzers. Disk 2 contains the files for the 16554/5/6/7 logic analyzers.**
2. Configure the menu to "Load" the analyzer with the appropriate configuration file (see table below).
3. Execute the load operation to load the file into the logic analyzer that the PCI State Analysis Probe module is connected to. **DO NOT SELECT ALL OR SYSTEM.**

Logic Analyzer Configuration Files

Logic Analyzer	Number of PODS required/Number of Cards required	File name for State Analysis	Comment
166x	4/NA	CP223_1	32 bit Multiplexed - State Analysis Probe PODS 1-4 connect to Logic Analyzer PODS 1-4 DISK 1
166x	6/NA	CP223_2	32 bit Demultiplexed - State Analysis Probe PODS 1-6 connect to Logic Analyzer PODS 1-6 DISK 1
166x	6/NA	CP223_3	64-bit Demultiplexed - State Analysis Probe PODS 1-8 to Logic Analyzer PODS 1-8 DISK 1
166X	8/NA	CP223_3E	32 bit Demultiplexed w/ Error Analysis - State Analysis Probe PODS 1-6,9-10 connect to Logic Analyzer PODS 1-6,9-10 DISK 1
16550A	4/1	CP223_4	32 bit Multiplexed - State Analysis Probe PODS 1-4 connect to Logic Analyzer PODS 1-4 DISK 1
16550A	6/1	CP223_5	32 bit Demultiplexed - State Analysis Probe PODS 1-6 connect to Logic Analyzer PODS 1-6 DISK 1

Logic Analyzer	Number of PODS required/Number of Cards required	File name for State Analysis	Comment
16550A	8/2	CP223_5E	32 bit Demultiplexed w/Error Analysis - State Analysis Probe PODS 1-6 connect to Logic Analyzer Master Card PODS 1-6 and PODS 1-2 on the Slave Card respectively DISK 1
16550A	8/2	CP223_7	64 bit Demultiplexed - State Analysis Probe PODS 1-8 connect to Logic Analyzer PODS 1-6 on the Master card and PODS 1-2 on the Slave Card respectively DISK 1
16550A	10/2	CP223_7E	64 bit Demultiplexed w/ Error Analysis - State Analysis Probe PODS 1-10 connect to Logic Analyzer PODS 1-6 on the Master card and PODS 1-4 on the Slave Card respectively DISK 1
1655x,167x	4/1	CP223_8	32 bit Multiplexed - State Analysis Probe PODS 1-4 connect to Logic Analyzer PODS 1-4 DISK 2
1655x, 1670/71	6/2	CP223_9	32 bit Demultiplexed - State Analysis Probe PODS 1-6 connect to PODS 1-4 on the Master card and 1-2 on the Slave card 1-2 respectively (PODS 1-6 on the 1670/71) DISK 2
1655x, 1670/71	8/2	CP223_9E	32 bit Demultiplexed w/ Error Analysis - State Analysis Probe PODS 1-6,9,10 connect to PODS 1-4 on the Master card and 1-4 on the Slave card (PODS 1-8 on the 1670/71) DISK 2
1655x	8/2	CP223_11	64 bit Demultiplexed - State Analysis Probe PODS 1-8 connect to Logic Analyzer PODS 1-4 on the Master card, 1-4 on the lower slave card (positioned below the master card in the mainframe) DISK 2
1655x	10/3	CP223_1E	64 bit Demultiplexed w/ Error Analysis - State analysis Probe PODS 1-8 connect to Logic Analyzer PODS 1-4 on the master card, 1-4 on the lower slave card (positioned below the master card in the mainframe) and PODS 1-2 on the slave card positioned above the master card in the mainframe respectively DISK 2
16715/6/7 16750/1/2	4/1	CP223_12	32 bit Multiplexed - State Analysis Probe PODS 1-4 connect to Logic Analyzer PODS 1-4 DISK 2

Logic Analyzer	Number of PODS required/Number of Cards required	File name for State Analysis	Comment
16715/6/7 16750/1/2	6/2	CP223_13	32 bit Demultiplexed - State Analysis Probe PODS 1-6 connect to PODS 1-4 on the master card and 1-2 on the slave card 1-2 respectively DISK 2
16715/6/7 16750/1/2	8/2	CP223_13E	32 bit Demultiplexed w/ Error Analysis - State Analysis Probe PODS 1-6,9,10 connect to PODS 1-4 on the Master card and 1-4 on the Slave card DISK 2
16715/6/7 16750/1/2	8/2	CP223_14	64 bit Demultiplexed - State Analysis Probe PODS 1-8 connect to Logic Analyzer PODS 1-4 on the Master card, 1-4 on the lower slave card (positioned below the master card in the mainframe) DISK 2
16715/6/7 16750/1/2	10/3	CP223_14E	64 bit Demultiplexed w/ Error Analysis- State Analysis Probe PODS 1-8 connect to Logic Analyzer PODS 1-4 on the Master card, 1-4 on the lower slave card (positioned below the master card in the mainframe) and PODS 1-2 on the slave card positioned above the master card in the mainframe respectively DISK 2

The PCI Inverse Assembler

The Inverse Assembler is auto loaded into the logic analyzer when the configuration file is loaded.

- IFS2102 is the Inverse Assembler for the 166x, 167x and all supported logic analyzers installed into the 16500A/B/C mainframe.
- IFS2102E is the Inverse Assembler for all logic analyzers installed into the 16600 and 16700.

If the Inverse Assembler does not appear on the state listing screen select the base of the label DATA. From the menu that appears select INVASM. For the 16600/700 series logic analyzers select INVASM in the listing window and then LOAD IFS2102E.

The Format Menu

The PCI State Analysis Probe diskette sets up the format menu to include all of the signals that are presented to the logic analyzer. The labels STAT, DATA , DATA_B, ADDR and ADDR_B are required in order run the Inverse Assembler. They should not be changed or deleted.

The STAT variable

The STAT variable is used by the PCI inverse assembler to decode PCI bus transactions. *It should not be changed or deleted from the format menu.* The signals that make up the STAT variable are listed in the following table.

STAT Variable	PCI Bus Signal Name
Bit 30	C/BE7
Bit 29	C/BE6
Bit 28	C/BE5
Bit 27	C/BE4
Bit 26	AVALID_L
Bit 25	FRAME#
Bit 24	WNODEV_L
Bit 23	ACK64#
Bit 22	TABORT_L
Bit 21	RETRY_L
Bit 20	WTARGET_L
Bit 19	IWINITI_L
Bit 18	DVALID_L
Bit 17	ANYERROR_L
Bit 16	IDLE_L
Bit 15	SERR#
Bit 14	MABORT_L
Bit 13	REQ64#
Bit 12	EOFT_L
Bit 11	IRDY#
Bit 10	TRDY#
Bit 9	STOP#
Bit 8	DEVSEL#
Bit 7	L_CM3
Bit 6	L_CM2

STAT Variable	PCI Bus Signal Name
Bit 5	L_CM1
Bit 4	L_CM0
Bit 3	C/BE3
Bit 2	C/BE2
Bit 1	C/BE1
Bit 0	C/BE0

The ADDR, ADDR_B, DATA_B and DATA variables

The ADDR, ADDR_B, DATA_B and DATA variables are defined in the format menu and used to pass the AD line information to the Inverse Assembler during state analysis. They are mapped as shown in the below table. *These variables should not be changed or deleted from the format Menu.*

Mode	ADDR	ADDR_B	DATA	DATA_B
32 BIT MUX	NOT USED	NOT USED	LOWER 32 AD LINES	NOT USED
32 BIT DEMUX	ADDRE SS	NOT USED	LOWER 32 AD LINES - DATA	NOT USED
64 BIT DEMUX	ADDRE SS	NOT USED	LOWER 32 AD LINES - DATA	UPPER 32 AD LINES- DATA
WITH ERROR	N/A	ERROR BITS	N/A	N/A

The BUS_UT variable

The Bus Utiliazation BUS_UT variable is made up of the following cycle bits : WNODEV, ADVALID, TABORT, DVALID, WTARGET, WINITI, RETRY, IDLE, MABORT. The list of symbols defined for this variable are the signal names themselves. This is a convenient grouping that helps make triggering and performance analysis easier.

The L_CMD variable

This variable is the C/BE[3:0] lines latched with the first rising edge of the PCI clock with FRAME# asserted. These signals are held until the end of the transaction. They indicated the command that is being transmitted on the PCI Local bus. Below is the encoding of these signals and the symbols defined for the L_CMD variable. These encodings can also be found in the PCI Specification.

Symbol	L_CMD encoding
INTACK	0000
SPEC_CYC	0001
I/O_RD	0010
I/O_WR	0011
RESRVD	0100
RESRVD	0101
MEM_RD	0110
MEM_WR	0111
RESRVD	1000
RESRVD	1001
CON_RD	1010
CON_WR	1011
MEMRDM	1100
DAC_CY	1101
MEMRDL	1110
MEMWRI	1111
I/O_XACTIONS	001X
MEM_XACTIONS	011X
CONFIG_XACTIONS	101X

Theory of Operation

The PCI State Analysis Probe is a universal PCI short card that attaches to logic analyzers. The State Analysis Probe has five major parts:

1. The primary stage input transparent latches
2. The secondary stage clocked buffers
3. The interface to the logic analyzer
4. The clocking and cycle bit generation logic
5. The Compliance Violation detection circuitry
6. The address increment logic
7. The extender card connector

The Primary and Secondary Stage Buffers

The primary stage input transparent latches present a single electrical load on the PCI bus and latch on the rising edge of the PCI clock. The secondary stage clocked buffers receive the output of the primary stage and are clocked on the falling edge of the PCI clock. The PCI clock is received by the PLX EQ6600A

The User pin signals 1 and 4-6 are not latched.

The interface to the Logic Analyzer

The input to the logic analyzer consist of 3 parts.

1. The RC terminators (90 ohm/10pf)
2. The 40 pin headers
3. The 40 pin cables

The user is instructed to remove the probe tip assemblies from the logic analyzer headers. The 40 pin logic analyzer headers then go directly the 40 pin headers of the State Analysis Probe provided cables. Any unused cables can be removed and attached at a later time when desired.

Power Circuitry

The logic analyzer provides the power to a power plane on the PCI State Analysis module. This power is then routed through 2 parts (one for 32 bit operation, one for 64 bit operation) to the on board logic. These parts operate such that if the PCI State Analysis module is removed from the target while the logic analyzer power is applied it will shut off power to the on board logic. This is to minimize the possibility of shorting if the module is laid down on a bench. However, shorting may still occur since power from the logic analyzer is live. No power is obtained from the target to power any on board circuitry. The PCI voltages are routed on a separate plane to the extender card connector.

The Clocking and Cycle bit Generation Logic

The master clock is controlled by the front panel switches and is generated by the on-board CPLD devices. All of the PCI cycle bits are generated based on the latched version of the PCI control signals. Their meaning is listed in the table below.

Cycle bit name	Function
EOFT_L - End of Transaction	True for one clock cycle and indicates the last cycle of a transaction
MABORT_L - Master Abort	True when a Master Abort condition has been detected. Five clock cycles on a single data transfer with no DEVSEL assertion and six clock cycles on a multi-beat transfer with no DEVSEL asserted. Remains true for one clock cycle.

Cycle bit name	Function
IDLE_L - Idle cycle	True when the bus is IDLE. False when the bus is busy.
DVALID_L - Data Valid	True when data is being transferred on the PCI bus.
WINITI_L - Master Initiated Wait State	True when a wait state is being initiated by the master
WTARGET_L - Target Initiated Wait State	True when a wait state is being initiated by the target
RETRY_L - Retry	True when a retry condition has been detected on the PCI bus
TABORT_L - Target Abort	True when a Target Abort condition has been detected on the PCI bus. This signal is true for one clock bit.
WNODEV_L - Wait state caused by no assertion of DEVSEL#	True when a wait state has been caused by no assertion of DEVSEL#.
GNT_L - The Grant signal for that slot	This signal is latched and held until the end of transaction. Useful as a store qualifier.
L_CMD - The latched command lines	The C/BE signals latched during the command /address phase and held until end of transaction.
AVALID_L - Address Valid	True on the first assertion of FRAME# and the rising edge of the PCI clock. True for one cycle except on Dual Address cycles when it is true for two cycles.

Address Increment

The ADDRESS CPLD takes the latched AD lines from the primary stage input latches and a clock from the cycle CPLD. The address is passed through to the logic analyzer during the address and first data cycle and incremented on each subsequent data cycles until the end of transaction. When the address reaches all F's the counter rolls over. The address increment functionality does not support increments past the lower 32 bits. DAC (Dual address cycle –64 bits) transactions are supported but only the lower 32 bits will increment. ADDR on PODs 5 and 6 is this latched and incremented address. Per the PCI specification the lower two bits 0 and 1 are zero'd out when feed to the address counter. However, the Inverse Assembler will display the address given on the bus (as will the DATA variable) during a valid address phase.

Compliance Violations

These violations are derived from the PCI Compliance Checklist and the PCI Specification. They are sent as individual signals to the logic analyzer on PODs 9 and 10 or as 5 bits encoded on channels 4-0 on POD 10. If any of these errors occur the signal ANYERROR on POD 2 will assert and will be clocked to the logic analyzer by the master clock. The error signals, the encoded error summary and the signal ANYERROR will be asserted for 1-2 PCI clock tics. A list of the violations appears on page 14.

State Analysis

This chapter explains how to configure the PCI State Analysis Probe to perform state analysis on the PCI Local Bus. The configuration software on the flexible diskette sets up the format specification menu of the logic analyzer for compatibility with the PCI Local Bus.

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the PCI State Analysis Probe module.

1. After removing the probe tip assemblies, plug the logic analyzer cables into the State Analysis Probe cable headers. See page 11 of this manual for details.
2. Power off the target. Install the PCI State Analysis Probe module into a slot in the target PCI Local bus. Then power on the target.

Load the logic analyzer configuration file by loading the appropriate file from the appropriate FS2102/3 software diskette. See page 17 of this manual for details.

Using the front panel switches

The front panel switches with corresponding LEDs are clearly marked on the front panel.

- **The acquire parity** switch control whether the logic analyzer will acquire the cycles that PAR and PERR signals are valid on. If the Parity acquire LED is lit then those cycles will be acquired.
- The **No Wait** switch controls the acquisition of WAIT cycles. If the No Wait LED is lit then NO WAIT cycles will be acquired.
- The **No Idle** switch controls the acquisition of IDLE cycles. If the No Idle LED is lit then NO IDLE cycles will be acquired.
- The **TDO-TDI** switch from the top connects TDO to TDI. If the switch is to the rightmost position TDO is connected to TDI. There is no LED corresponding to this switch.

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Slow or Missing Clock" when the data is not being transmitted across the bus.

The State Listing Display

Captured data is as shown in the following figure. The below figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

The screenshot shows a software window titled "Listing<1>". The menu bar includes "File", "Edit", "Options", "Invasm", "Source", and "Help". Below the menu bar are buttons for "Navigate" and "Run". A toolbar contains buttons for "Search", "Goto", "Markers", "Comments", "Analysis", and "Mixed Signal". A text box displays a message: "The NEW FS2102/3 has built in Compliance Violation triggering. Post processing filters and increments the address to the logic analyzer during burst operations.!". Below this is a table with columns for "State Number", "FUTUREPLUS SYSTEMS c 1998", "ADDR", "Decimal", "PCI BUS TRANSACTIONS REV 1.1", and "Hex".

State Number	FUTUREPLUS SYSTEMS c 1998	ADDR
4	MEM WRITE ADR=0061E000	0061E000
5	D32=FFF80000	0061E000
6	D32=0007FFFC	0061E004
7	D32=00000000	0061E008
8	D32=000007FF	0061E00C
9		0061E00C
	COMPLIANCE VIOLATION	
	RULE VIOLATION 4 DETECTED	
10		0061E00C
	COMPLIANCE VIOLATION	
	RULE VIOLATION 4 DETECTED	
11		FE04C348
	COMPLIANCE VIOLATION	
	RULE VIOLATION 6 DETECTED	
12		FE04C34C

Error Messages

In addition to the compliance violation messages, the following error messages are reported by the PCI inverse assembler.

ERROR-NO DEVICE SELECTED

This error is displayed during a non special cycle data phase when IRDY and TRDY are asserted and DEVSEL is not asserted.

ERROR DEVSEL ASSERTED

This error is displayed during a special cycle data phase if DEVSEL is asserted.

SYSTEM ERROR

This error is displayed anytime SERR# is asserted.

ADDRESS PHASE NOT VALID

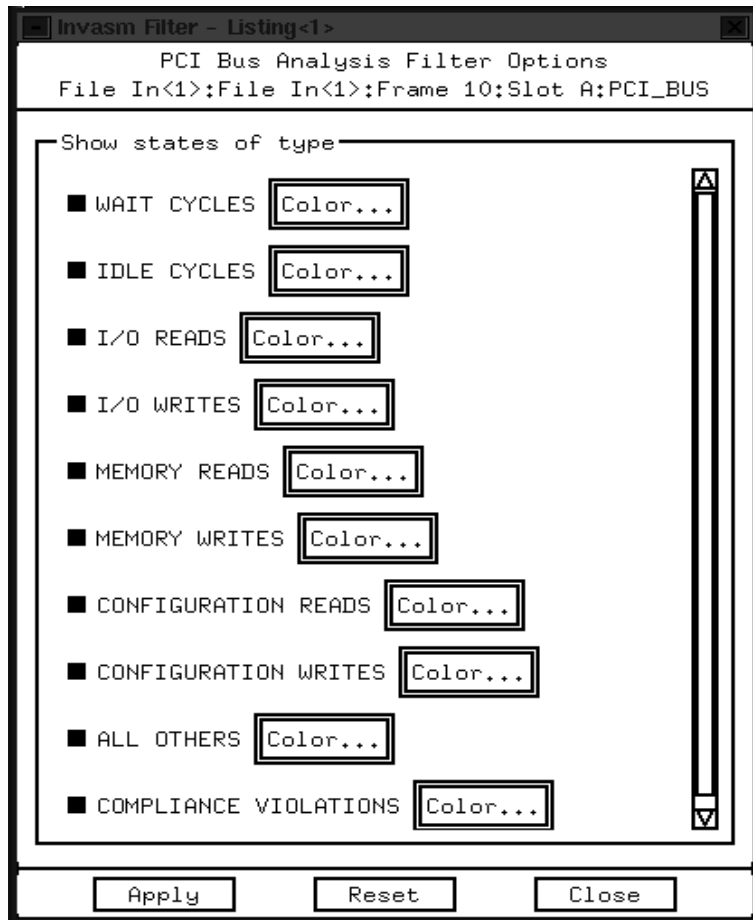
TRDY#, IRDY#, STOP or DEVSEL were asserted with the first assertion of FRAME# and the rising edge of the PCI clock.

Post Processing Filters

Post Processing Filters is only available with the 16600 or 16700 mainframe logic analyzers.

Filters can be invoked by selecting FILTER from the INVASM menu in the state listing display. The following selections can be suppressed or shown.

- I/O Reads
- I/O Writes
- Configuration Reads
- Configuration Writes
- Memory Reads
- Memory Writes
- IDLE cycles
- WAIT cycles
- All other transactions (this includes Interrupt Acknowledge and Special Cycle transactions)
- Compliance Violations

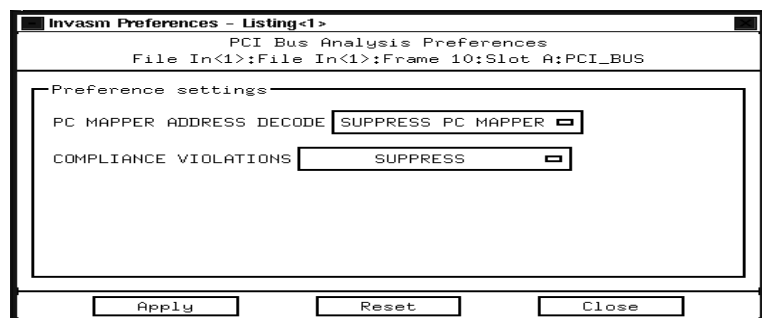


Filter selection for the FS2102 and FS2103 state listing

PC Mapper

The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the button to the left of the list. A default color scheme has been selected for each transaction type. This can be changed by selecting the button to the right of the list.

PC Mapper is a feature that adds additional decode to the state listing display. This includes PCI I/O and memory address decode to indicate common PC access. This feature can be enabled by selecting Preferences in the INVASM menu in the state listing screen. *This feature is only available with the 16600 or 16700 mainframe logic analyzers.*



Preferences selection for the PCI State Analysis Probe

Compliance violations are detected by the FS2102/FS2103 hardware and displayed in the Listing screen. The Inverse Assembler by default has the display of compliance violation error codes SUPPRESSED. Even when these violations are SUPPRESSED the user will still know that a violation occurred by seeing the PCI cycle displayed in red and by the assertion of ANYERROR. When the compliance violations are set to show POD's 9 and 10 must be connected so that the Inverse Assembler has access to the error codes.

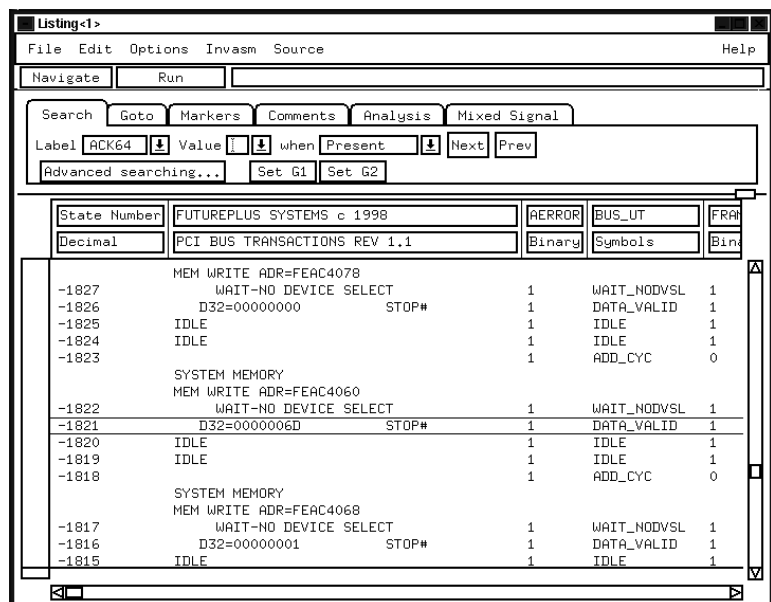
Acquiring Data

Data can be acquired by touching the RUN button. As soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Slow or Missing Clock" if the PCI Clock signal is not being detected by the logic analyzer. In this case, check the logic analyzer to PCI State Analysis Probe connection (refer to your logic analyzer User's Manual).

The State Display with the PCI PC Mapper

Captured data is as shown in the following figure. The first figure displays the state listing after disassembly. The PCI PC Mapper is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.



PCI PC Mapping for memory transactions

This section lists the addresses, the commands and the corresponding mapping done by the PCI PC Mapper software. For information on the standard PCI configuration register mapping please refer to the PCI Local Bus Specification Rev 2.1.

Address bits 23-0	PC Mapper output
greater than 0FFFFFFH	System Memory
0FFFFFF-0E0000H	System BIOS
0DFFFF-0C0000H	ROM Scan
0BFFFF-0A0000H	Video Memory
09FFFF-000400H	System Memory
0003FF-000000H	See Interrupt Vector Table

Interrupt Vector Table

Address bits 23-0	PC Mapper output
0003C4H	INT #F1-FF USER PROGRAMS
000200H	INT #80-F0 BASIC
0001E0H	INT #78-7F USER PROGRAMS
0001DCH	INT #77 IRQ15
0001D8H	INT #76 IRQ14
0001D4H	INT #75 IRQ13
0001D0H	INT #74 IRQ12
0001CCH	INT #73 IRQ11
0001C8H	INT #72 IRQ10
0001C4H	INT #71 IRQ9
0001C0H	INT #70 IRQ8
0001A0H	INT #68-6F RESERVED
00019CH	INT #67 EXP MEM MANG
000180H	INT #60-66 USER PROGRAMS
00012CH	INT #4B-5F RESERVED
000128H	INT #4A USER RTC ALARM
00011CH	INT #47-49 RESERVED
000118H	INT #46 HD DISK #1 PARAM
000110H	INT #44-45 RESERVED
00010CH	INT #43 VIDEO CHAR TABLE
000108H	INT #42 EGA BIOS
000104H	INT #41 HD DISK #0 PARAM
000100H	INT #40 FLOPPY DISK ISR
000080H	INT #20-3F RESERVED DOS
00007CH	INT #1F VIDEO CHAR TABLE
000078H	INT #1E FLOPPY PARAMS
000074H	INT #1D AVAILABLE
000070H	INT #1C AVAILABLE
00006CH	INT #1B KEYBOARD BREAK
000068H	INT #1A RTC ISR
000064H	INT #19 BOOSTRAP LOADER
000060H	INT #18 ROM BASIC
00005CH	INT #17 LPT PRINTER BIOS
000058H	INT #16 KEYBOARD BIOS
000054H	INT #15 SYS SERVICE BIOS
000050H	INT #14 SERIAL PORT BIOS
00004CH	INT #13 FLOPPY DISK BIOS
000048H	INT #12 MEM SIZE INT
000044H	INT #11 EQUIP LIST
000040H	INT #10 VIDEO BIOS
00003CH	INT #0F IRQ7 LPT1
000038H	INT #0E IRQ6 FLOPPY DISK
000034H	INT #0D IRQ5 LPT2
000030H	INT #0C IRQ4 SERIAL #1
00002CH	INT #0B IRQ3 SERIAL #2
000028H	INT #0A IRQ2 SLAVE INT
000024H	INT #09 KEYBOARD
000020H	INT #08 IRQ0 SYS TIMER
00001CH	INT #07 NUM COPROCESSOR
000018H	INT #06 INVALID OPCODE
000014H	INT #05 PRINT SCREEN
000010H	INT #04 OVERFLOW DETECT

Address bits 23-0	PC Mapper output
00000CH	INT #03 BREAKPOINT TRACE
000008H	INT #02 NMI
000004H	INT #01 SINGLE STEP
000000H	INT #00 DIVIDE BY ZERO

PCI PC Mapping - I/O Transactions

Address bits 23-0	PC Mapper output
0000H	MSTR DMA CH 0
0001H	MSTR DMA CH 0
0002H	MSTR DMA CH 1
0003H	MSTR DMA CH 1
0004H	MSTR DMA CH 2
0005H	MSTR DMA CH 2
0006H	MSTR DMA CH 3
0007H	MSTR DMA CH 3
0008H	MSTR DMA STAT REG
0009H	UNKNOWN IO DEVICE
000AH	MSTR DMA MASK REG
000BH	MSTR DMA MODE REG
000CH	MSTR DMA CLR BYTE PTR
000DH	MSTR DMA MSTR CLEAR
000EH	MSTR DMA CLEAR MASK
000FH	MSTR DMA WRT MASK
0018H	MSTR DMA CH EXT FUNCT REG
001AH	MSTR DMA EXT FUNCT
0020H	MSTR INT REQ REG
0021H	MSTR INT REQ REG2
0040H	INTERVAL TIMER TIMER 0
0042H	INTERVAL TIMER SPKR TIMER
0043H	INTRVAL TIMER #1 CNTRL
0044H	INTERVL TIMER #2 WATCHDOG
0047H	INTERVAL TIMER #2 CNTRL
0060H	KEYBOARD/MOUSE DATA PORT
0061H	SYSTEM CONTOL PORT B
0064H	KEYBOARD/MOUSE CMD PORT
0070H	RTC/CMOS RAM ADDR PORT
0071H	RTC/CMOS RAM DATA PORT
0074H	EXT CMOS RAM ADDR PORT
0075H	EXT CMOS RAM ADDR PORT
0076H	EXT CMOS RAM DATA PORT
0081H	CH 2 DMA PAGE REGISTER
0082H	CH 3 DMA PAGE REGISTER
0083H	CH 1 DMA PAGE REGISTER
0087H	CH 0 DMA PAGE REGISTER
0089H	CH 6 DMA PAGE REGISTER
008AH	CH 7 DMA PAGE REGISTER
008BH	CH 5 DMA PAGE REGISTER
008FH	CH 4 DMA PAGE REGISTER
0090H	ARB CNTRL POINT REG
0091H	FEEDBACK REG
0092H	SYSTEM CONTROL PORT A
0094H	SYS SETUP/CARD ENABLE REG
0096H	ADAPTOR SETUP/ENABLE REG
00A0H	SLAVE INTERRUPT CNTRLR
00A1H	SLAVE INTERRUPT CNTRLR
00C0H	SLAVE DMA CH4 MEM ADDR
00C2H	SLAVE DMA CH4 TRANS COUNT
00C4H	SLAVE DMA CH5 MEM ADDR
00C6H	SLAVE DMA CH5 TRANS COUNT

00C8H	SLAVE DMA CH6 MEM ADDR
Address bits 23-0	PC Mapper output
00CAH	SLV DMA CH6 TRANS COUNT
00CCH	SLAVE DMA CH7 MEM ADDR
00CEH	SLAVE DMA CH7 TRANS COUNT
00D0H	SLV DMA STATUS REG CH 4-7
00D4H	SLV DMA MASK REG CH 4-7
00D6H	SLAVE DMA MODE REG CH 4-7
00D8H	SLAVE DMA CLEAR BYTE PNTR
00DAH	SLAVE DMA MASTER CLEAR
00DCH	SLV DMA CLR MASK CH 4-7
00DEH	SLAVE DMA WRITE MASK REG
00E0H	IBM MODELS - ENCODE REG
00E1H	IBM MODELS - ENCODE REG
00F1H	NUMERIC COPROCESSOR RESET
00F8H	NUMERIC COPROCESSOR PORT
00F9H	NUMERIC COPROCESSOR PORT
00FAH	NUMERIC COPROCESSOR PORT
00FBH	NUMERIC COPROCESSOR PORT
00FCH	NUMERIC COPROCESSOR PORT
0100H	ADAPTER CARD POS REG 0
0101H	ADAPTER CARD POS REG 1
0102H	SYS BD/ADP CD POS REG 2
0103H	SYS BD/ADP CD POS REG 3
0104H	ADAPTER CARD POS REG 4
0105H	ADAPTER CARD POS REG 5
0106H	ADAPTER CARD POS REG 6
0107H	ADAPTER CARD POS REG 6
0278H	PARALLEL PORT 3 DATA PORT
0279H	PARALLEL PORT 3 STAT PORT
027AH	PARALLEL PORT 3 CMD PORT
02F8H	SERIAL PORT 2 XMIT/REC
02F9H	SER PORT 2 DIV LATCH/INT
02FAH	SERIAL PORT 2 INT ID REG
02FBH	SERIAL PORT 2 CNTRL REG
02FDH	SERIAL PORT 2 MODEM CNTRL
02FEH	SERIAL PORT 2 MODEM STAT
02FFH	SERIAL PORT 2 SCRTCH REG
0378H	PARALLEL PORT 2 DATA PORT
0379H	PARALLEL PORT 2 STAT PORT
037AH	PARALLEL PORT 2 CMD PORT
03B4H	VGA CRT CNTRLR ADDR REG
03B5H	VGA CRT CNTRLR DATA REG
03BAH	VGA STAT 1/FEATURE CNTRL
03BCH	PARALLEL PORT 1 DATA PORT
03BDH	PARALLEL PORT 1 STAT PORT
03BEH	PARALLEL PORT 1 CMD PORT
03C0H	VGA ATTRIBUTE CNTRLR ADDR
03C1H	VGA ATTRIBUTE CNTRLR DATA
03C2H	VGA OUTPUT/STAT REG
03C3H	VGA VIDEO SUBSYSTEM ENABLE
03C4H	VGA SEQUENCER ADDR REG
03C5H	VGA SEQUENCER DATA REG

Address bits 23-0	PC Mapper output
03C7H	VIDEO DAC PAL ADDR/STAT
03C8H	VIDEO DAC PAL ADDR/WRITE
03C9H	VIDEO DAC PALETTE DATA
03CAH	VGA FEATURE CONTROL REG
03CCH	VGA MISC OUTPUT REG
03CEH	VGA GRAPHICS CNTRLR ADDR
03CFH	VGA GRAPHICS CNTRLR ADDR
03D4H	VGA CRT CNTRLR ADDR REG
03D5H	VGA GRAPHICS CNTRLR DATA
03DAH	VGA COLOR STAT 1/FEATURE
03F0H	FLOPPY STATUS REG A
03F1H	FLOPPY STATUS REG B
03F2H	FLOPPY DIGITAL OUTPUT REG
03F4H	FLOPPY DISK CNTRLR STAT
03F5H	FLOPPY DISK CNTRLR DATA
03F7H	FLOPPY CONFIG CONTROL REG
03F8H	SERIAL PORT 1 XMIT/RCV BUF
03F9H	SER PORT 1 DIV LATCH/INT
03FAH	SERIAL PORT 1 INT ID/FIFO
03FBH	SERIAL PORT 1 LINE CNTRL
03FCH	SERIAL PORT 1 MODEM CNTRL
03FDH	SERIAL PORT 1 STAT REG
03FEH	SERIAL PORT 1 MODEM STAT
03FFH	SERIAL PORT 1 SCRATCH REG
0680H	MANUFACTURING CHECKPOINT PORT

Timing Analysis

Although the FS2102/3 2 was designed for state analysis, timing analysis can be accomplished using a flying lead set attached to the extender card connector pins. The below chart gives the pin out of the FS2102 (3.3V) and FS2103 (5.0V) extender card connector. It is recommended that for 66 MHz analysis the 16517A/518A high speed timing card be used due to its fast sampling rate.

Side B is the front side of the module and pin B1 is the first pin on side B closest to the front panel. Side A is the back side and pin A1 is the first pin on side A closest to the front panel.

PIN	5V		3.3V		COMMENT
	B	A	B	A	
1	-12V	TRST#	-12V	TRST#	32-bit connector start
2	TCK	+12V	TCK	+12V	
3	Ground	TMS	Ground	TMS	
4	TDO	TDI	TDO	TDI	
5	+5V	+5V	+5V	+5V	
6	+5V	INTA#	+5V	INTA#	
7	INTB#	INTC#	INTB#	INTC#	
8	INTD#	+5V	INTD#	+5V	
9	PRSNT1#	Reserved	PRSNT1#	Reserved	
10	Reserved	+5V (I/O)	Reserved	+3.3V (I/O)	
11	PRSNT2#	Reserved	PRSNT2#	Reserved	
12	Ground	Ground	KEYWAY	KEYWAY	Connector Key 3.3 volt key
13	Ground	Ground	KEYWAY	KEYWAY	Connector Key 3.3 volt key
14	Reserved	3.3Vaux	Reserved	3.3Vaux	

15	Ground	RST#	Ground	RST#	
16	CLK	+5V (I/O)	CLK	+3.3V (I/O)	
17	Ground	GNT#	Ground	GNT#	
18	REQ	Ground	REQ#	Ground	
19	+5V (I/O)	PME#	+3.3V (I/O)	PME#	
20	AD[31]	AD[30]	AD[31]	AD[30]	
21	AD[29]	+3.3V	AD[29]	+3.3V	
22	Ground	AD[28]	Ground	AD[28]	
23	AD[27]	AD[26]	AD[27]	AD[26]	
24	AD[25]	Ground	AD[25]	Ground	
25	+3.3V	AD[24]	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	AD[23]	+3.3V	
28	Ground	AD[22]	Ground	AD[22]	
29	AD[21]	AD[20]	AD[21]	AD[20]	
30	AD[19]	Ground	AD[19]	Ground	
31	+3.3V	AD[18]	+3.3V	AD[18]	
32	AD[17]	AD[16]	AD[17]	AD[16]	
33	C/BE[2]#	+3.3V	C/BE[2]#	+3.3V	
34	Ground	FRAME#	Ground	FRAME#	
35	IRDY#	Ground	IRDY#	Ground	
36	+3.3V	TRDY#	+3.3V	TRDY#	
37	DEVSEL#	Ground	DEVSEL#	Ground	
38	Ground	STOP#	Ground	STOP#	
39	LOCK#	+3.3V	LOCK#	+3.3V	
40	PERR#	SDONE	PERR#	SDONE	
41	+3.3V	SBO#	+3.3V	SBO#	
42	SERR#	Ground	SERR#	Ground	
43	+3.3V	PAR	+3.3V	PAR	
44	C/BE[1]#	AD[15]	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	AD[14]	+3.3V	
46	Ground	AD[13]	Ground	AD[13]	
47	AD[12]	AD[11]	AD[12]	AD[11]	
48	AD[10]	Ground	AD[10]	Ground	
49	Ground	AD[09]	M66EN	AD[09]	66 MHz / gnd
50	CONNECTOR KEY	CONNECTOR KEY	Ground	Ground	5 volt key

51	CONNECTOR KEY	CONNECTOR KEY	Ground	Ground	5 volt key
52	AD[08]	C/BE[0]#	AD[08]	C/BE[0]#	
53	AD[07]	+3.3V	AD[07]	+3.3V	
54	+3.3V	AD[06]	+3.3V	AD[06]	
55	AD[05]	AD[04]	AD[05]	AD[04]	
56	AD[03]	Ground	AD[03]	Ground	
57	Ground	AD[02]	Ground	AD[02]	
58	AD[01]	AD[00]	AD[01]	AD[00]	
59	+5V (I/O)	+5V (I/O)	+3.3V (I/O)	+3.3V (I/O)	
60	ACK64#	REQ64#	ACK64#	REQ64#	
61	+5V	+5V	+5V	+5V	
62	+5V	+5V	+5V	+5V	32-bit connector end
	CONNECTOR KEY	CONNECTOR KEY	CONNECTOR KEY	CONNECTOR KEY	64-bit spacer
	CONNECTOR KEY	CONNECTOR KEY	CONNECTOR KEY	CONNECTOR KEY	64-bit spacer
63	Reserved	Ground	Reserved	Ground	64-bit connector start
64	Ground	C/BE[7]#	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	+5V (I/O)	C/BE[4]#	+3.3V (I/O)	
67	Ground	PAR64	Ground	PAR64	
68	AD[63]	AD[62]	AD[63]	AD[62]	
69	AD[61]	Ground	AD[61]	Ground	
70	+5V (I/O)	AD[60]	+3.3V (I/O)	AD[60]	
71	AD[59]	AD[58]	AD[59]	AD[58]	
72	AD[57]	Ground	AD[57]	Ground	
73	Ground	AD[56]	Ground	AD[56]	
74	AD[55]	AD[54]	AD[55]	AD[54]	
75	AD[53]	+5V (I/O)	AD[53]	+3.3V (I/O)	
76	Ground	AD[52]	Ground	AD[52]M	
77	AD[51]	AD[50]	AD[51]	AD[50]	
78	AD[49]	Ground	AD[49]	Ground	
79	+5V (I/O)	AD[48]	+3.3V (I/O)	AD[48]	
80	AD[47]	AD[46]	AD[47]	AD[46]	
81	AD[45]	Ground	AD[45]	Ground	
82	Ground	AD[44]	Ground	AD[44]	

83	AD[43]	AD[42]	AD[43]	AD[42]	
84	AD[41]	+5V (I/O)	AD[41]	+3.3V (I/O)	
85	Ground	AD[40]	Ground	AD[40]	
86	AD[39]	AD[38]	AD[39]	AD[38]	
87	AD[37]	Ground	AD[37]	Ground	
88	+5V (I/O)	AD[36]	+3.3V (I/O)	AD[36]	
89	AD[35]	AD[34]	AD[35]	AD[34]	
90	AD[33]	Ground	AD[33]	Ground	
91	Ground	AD[32]	Ground	AD[32]	
92	Reserved	Reserved	Reserved	Reserved	
93	Reserved	Ground	Reserved	Ground	
94	Ground	Reserved	Ground	Reserved	64-bit connector end

General Information

This chapter provides additional reference information including the characteristics and signal connections for the PCI State Analysis Probe module.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the PCI State Analysis Probe module.

State Analysis Probe Interface Compatibility

32/64 bit PCI Local bus accepting the short card length and universal connector pinout. The ground coming from the PCI bus is common to the ground of the State Analysis Probe and the logic analyzer. The power is completely separate. The power from the PCI bus is routed up to the extender card connector to the card under test. The power for the logic on board the State analysis Probe is powered from the logic analyzer.

JTAG Boundary Scan

The PCI State Analysis Probe does not implement JTAG Boundary SCAN. The **TDO-TDI** switch on the front panel connects TDO to TDI. If the switch is to the rightmost position TDO is connected to TDI. In the leftmost position these signals are left open. There is no LED corresponding to this switch.

The PCI Present Pins

The PCI signals PRSNT1# and PRSNT2# are routed to the PCI State Analysis Probe extender card connector.

Standards Supported

The PCI Local Bus Specification Revision 2.1.

Power Requirements

The PCI State Analysis Probe contains several active components that buffer the PCI signals before they are acquired by the logic analyzer. The State Analysis Probe takes no power from the PCI bus but is powered by the logic analyzer. Power is removed from the on board components when the State Analysis Probe is removed from the PCI target.

Logic Analyzer Required

1660A/C, 1661A/C, 1662A/C, 16550A, 16554A, 16555A, 16556A, 1670A, 1671A, 1672A, 16710A, 16711A, 16712A, 16601A

Number of Probes Used

- 32 bit PCI multiplexed - 4 cable headers
- 32 bit PCI demultiplexed - 6 cable headers
- 64 bit demultiplexed, 64 bit data - 8 headers
- Compliance Error Analysis - Add 2 headers

Minimum Clock Period

0 to 66Mhz PCI clock

Signal loading

The PCI State Analysis Probe logic analyzer interface presents only one electrical load on each PCI bus signal. However, the extender card connector is an additional 3 inches beyond the maximum allowed stub length and the extender card connector and card under test presents an additional load.

Operations

All PCI Local Bus operations supported.

Environmental Temperature

Operating: 0 to 55 degrees C (+32 to +131 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Altitude

Operating: 4,600m (15,000 ft)

Non operating: 15,300m (50,000 ft)

Humidity

Up to 90% non condensing. Avoid sudden, extreme temperature changes which would cause condensation on the State Analysis Probe module.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the PCI State Analysis Probe module. If a failure is suspected in the PCI State Analysis Probe module contact the factory or your FuturePlus Systems authorized distributor.

Servicing

The repair strategy for the PCI State Analysis Probe is module replacement. However, if parts of the PCI State Analysis Probe module are damaged or lost contact the factory for replacement parts.

Signal Connections

The PCI State Analysis Probe module monitors signals only for state analysis. The below figure displays how the cable headers are numbered.

39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

The following tables list the PCI State Analysis Probe cable headers and the corresponding PCI Local Bus signals after these signals have been terminated by the 90K ohm/10pf terminators.

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 1 pin 3	CLK/16	FRAME#
5	no connect	
7	15	IRDY#
9	14	TRDY#
11	13	STOP#
13	12	DEVSEL#
15	11	L_CM3
17	10	L_CM2
19	9	L_CM1
21	8	L_CM0
23	7	C/BE3#
25	6	C/BE2#
27	5	C/BE1#
29	4	C/BE0#
31	3	PAR64/SDONE - JUMPER
33	2	PERR#/SBO - JUMPER
35	1	RST#/LOCK#- JUMPER
37	0	INTx# - JUMPER

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	Signal name
Header 2 pin 3	CLK/16	GNT_L
5	no connect	
7	15	REQ#
9	14	IDSEL#
11	13	WNODEV_L
13	12	ACK64#
15	11	TABORT_L
17	10	RETRY_L
19	9	WTARGET_L
21	8	WINITI_L
23	7	DVALID_L
25	6	ANYERROR_L
27	5	IDLE_L
29	4	SERR#
31	3	MABORT_L
33	2	REQ64#
35	1	EOFT_L
37	0	PAR

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 3 pin 3	CLK/16	MSCLK_H
5	no connect	
7	15	AD15
9	14	AD14
11	13	AD13
13	12	AD12
15	11	AD11
17	10	AD10
19	9	AD09
21	8	AD08
23	7	AD07
25	6	AD06
27	5	AD05
29	4	AD04
31	3	AD03
33	2	AD02
35	1	AD01
37	0	AD00

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 4 pin 3	CLK/16	AVALID_L
5	no connect	
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 5 pin 3	CLK/16	C/BE4#
5	no connect	
7	15	ADD15
9	14	ADD14
11	13	ADD13
13	12	ADD12
15	11	ADD11
17	10	ADD10
19	9	ADD09
21	8	ADD08
23	7	ADD07
25	6	ADD06
27	5	ADD05
29	4	ADD04
31	3	ADD03
33	2	ADD02
35	1	ADD01
37	0	ADD00

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 6 pin 3	CLK/16	C/BE5#
5	no connect	
7	15	ADD31
9	14	ADD30
11	13	ADD29
13	12	ADD28
15	11	ADD27
17	10	ADD26
19	9	ADD25
21	8	ADD24
23	7	ADD23
25	6	ADD22
27	5	ADD21
29	4	ADD20
31	3	ADD19
33	2	ADD18
35	1	ADD17
37	0	ADD16

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 7 pin 3	CLK/16	C/BE6#
5	no connect	
7	15	AD47
9	14	AD46
11	13	AD45
13	12	AD44
15	11	AD43
17	10	AD42
19	9	AD41
21	8	AD40
23	7	AD39
25	6	AD38
27	5	AD37
29	4	AD36
31	3	AD35
33	2	AD34
35	1	AD33
37	0	AD32

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 8 pin 3	CLK/16	C/BE7#
5	no connect	
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 9 pin 3	CLK/16	ERROR11_L
5	no connect	
7	15	ERROR10_L
9	14	ERROR9_L
11	13	ERROR8_L
13	12	ERROR7_L
15	11	ERROR6_L
17	10	ERROR5_L
19	9	ERROR4_L
21	8	ERROR3_L
23	7	ERROR2_L
25	6	ERROR1_L
27	5	ERROR0_L
29	4	RESVD
31	3	RESVD
33	2	RESVD
35	1	RESVD
37	0	RESVD

State Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 10 pin 3	CLK/16	RESVD
5	no connect	
7	15	USER6
9	14	USER5
11	13	USER4
13	12	USER3
15	11	USER2
17	10	USER1
19	9	ERROR21
21	8	ERROR20
23	7	ERROR19
25	6	ERROR18
27	5	ERROR17
29	4	ERROR16
31	3	ERROR15
33	2	ERROR14
35	1	ERROR13
37	0	ERROR12