

FuturePlus Systems Corporation



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PCI Analysis Probe-FS2001 Users Manual

For Agilent Technologies Logic Analyzers

Revision 4.3

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Introduction

The PCI Analysis Probe module provides a complete interface between any PCI add-in slot and Agilent Logic Analyzers. The Analysis Probe interface connects the signals from the PCI Local bus to the logic analyzer inputs.

The PCI Analysis Probe is a passive bus monitor which does not assert any signals on the PCI bus. The PCI bus signals are terminated with 90k ohm/10pf terminators so that they are matched to the logic analyzer. Since the PCI Analysis Probe does not actively buffer the PCI bus signals no skew is introduced.

The configuration software on the diskette sets up the format specification menu of the logic analyzer for compatibility with your PCI bus. When the state configuration file is loaded, an inverse assembler is also loaded which decodes PCI transactions into easy to read mnemonics.

This manual is organized to help you quickly find the information you need.

How to Use This Manual

- **Analyzing the PCI Local Bus** chapter introduces you to the PCI Analysis Probe and lists the minimum equipment required and accessories supplied for PCI bus analysis.
- The **State Analysis** chapter explains how to configure the PCI Analysis Probe to perform state analysis on your PCI bus.
- The **Timing Analysis** chapter explains how to configure the PCI Analysis Probe to perform timing analysis on your PCI bus.
- The **General Information** chapter provides some general information including the operating characteristics for the PCI Analysis Probe module and the cable header pinout.

Analyzing the PCI Local Bus

This chapter introduces you to the PCI Analysis Probe and lists the minimum equipment required and accessories supplied for PCI Local Bus analysis. This chapter also contains information that is common to both state and timing analysis.

Duplicating the 167xx Logic Analyzer Master Diskette

Before you use the FS2001 software on the 167xx logic Analyzer, make a duplicate copy of the master diskette. Then store the master diskette and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the diskette wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate diskette operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Accessories Supplied

The PCI Analysis Probe product consists of the following accessories:

- The Analysis Probe interface hardware, which includes the interface circuit module.
- Four jumpers which come installed on the circuit module.
- The inverse assembly and configuration software on a 3.5 inch diskette.
- This operating manual

Minimum Equipment Required

The minimum equipment required for analysis of a PCI Local Bus consists of the following equipment:

- A 1650, 166x, 167x, 16550 or 16510 Logic Analyzer
- The PCI Analysis Probe Product
- A PCI target bus

Signal Naming Conventions

This operating manual uses the same signal notation as the PCI LOCAL BUS SPECIFICATION - REVISION 2.0. That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

Connecting the Jumpers

There are four sets of jumpers to be configured on the PCI Analysis Probe. These jumpers are used to configure the master clock used for state analysis.

The Master L Clock - JMP 1

For 166x, 167x and 16550 logic analyzers jumper 1 must be connected between pins 2 and 3 of JMP 1. For 1650 and 16510 logic analyzers JMP 1 must be connected between pins 1 and 2.

Logic Analyzer	JMP 1
166x, 167x, 1655x	Connect pins 2 and 3
1650, 16510 and 16540/541	Connect pins 1 and 2

JMP 2, 3 and 4

For 166x, 167x, 1680/90 and 16550 logic analyzers jumpers 2, 3 and 4 must each be connected between pins 2 and 3. For 1650 and 16510 logic analyzers jumpers 2, 3 and 4 must each be connected between pins 1 and 2.

Logic Analyzer	JMP 2	JMP 3	JMP 4
166x, 167x, 1680/90 and 1655x	Connect pins 2 and 3	Connect pins 2 and 3	Connect pins 2 and 3
1650, 16540/541 and 16510	Connect pins 1 and 2	Connect pins 1 and 2	Connect pins 1 and 2

Connecting to the PCI Analysis Probe

The following explains how to connect the logic analyzer to the PCI Analysis Probe for either state or timing analysis:

1. Remove the probe tip assemblies from the logic analyzer cables.
2. Plug the logic analyzer cables into the PCI Analysis Probe cable headers as shown in the appropriate following tables.

FOR 16540/541 Logic Analyzers

Logic Analyzer	PCI Analysis Probe	Comment
16540 POD 1	Header 3	L clock
16541 POD 1	Header 1	
16541 POD 2	Header 2	
15541 POD 3	Header 4	optional User pins

For logic analyzers : 16510, 165x, 166x, 167x series and the 16550.

Logic Analyzer	PCI Analysis Probe	Comment
Master POD 1	Header 1	L clock
POD 2	Header 2	
POD 3	Header 3	
POD 4	Header 4	optional User pins
POD 5	Header 5	optional 64 bit
POD 6	Header 6	optional 64 bit

For logic analyzers 16555, 167xx

Logic Analyzer	PCI Analysis Probe	Comment
Master POD 1	Header 1	L clock
Master POD 2	Header 2	
Master POD 3	Header 3	
Master POD 4	Header 4	optional User pins
Expander POD 1	Header 1	optional 64 bit
Expander POD 2	Header 2	optional 64 bit

1680/90/900 users please refer to the 1680/90/900 setup section for directions on attaching the analyzer pods to the probe.

USER PINS

PCI Analysis Probe Header 4 contains up to 7 *User Defined* pins. These pins are available to the user to connect whatever additional signals the users wishes to view along with the PCI bus. These pins are terminated as described in the INTRODUCTION section of this manual. These pins are located below POD 5 on the PCI Analysis Probe module and clearly marked.

These pins may be used to connect the individual IDSEL signals or the bus grant signals from the PCI bus arbitration logic.

Installing the PCI Analysis Probe

The PCI Analysis Probe can be installed in any slot of the PCI Local bus. The following steps explain how to install the PCI Analysis Probe into the PCI Local bus.

1. Install the logic analyzer cables as described in the previous section.
2. Align the PCI module with the appropriate slot on the target system and plug the module into the PCI connector.

If your PCI Local bus is 32 bits the upper portion of the edge connector will not be inserted into any connector. This will not affect the modules operation on a 32-bit PCI Local bus.

Setting up the Analyzer installed in the 16500 mainframe and the portables

The logic analyzer can be configured for PCI analysis by loading the PCI configuration file. Loading this file will load the PCI Local bus inverse assembler and configure your logic analyzer. To load the configuration and inverse assembler:

1. Install the PCI Analysis Probe software flexible diskette in the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the appropriate configuration file (see table below).
3. Execute the load operation to load the file into the logic analyzer.

Logic Analyzer	File name for State Analysis	File name for Timing Analysis	Comment
16555, 167x	F555PCI	F555PCI	32 bit analysis
16555 (<i>requires 2 16555 cards</i>), 167x	F555P64	F555P64	64 bit analysis
166x	F660PCI	F660PCI	32/64 bit analysis
16550	F550PCI	F550PCI	32/64 bit analysis
16540	F540PCI	F540PCI	32 bit analysis
1650 and 16510	F510PCIS	F510PCIT	32 bit analysis

Please note that 166x, 67x, 1680/90 and 1655x users do not need to reload any files from the diskette when switching between state and timing analysis.

For 16500B main frame users with 16540/541, 1655x and 166x, 167x REV 2.0 (system software) users an enhanced inverse

Setting up the Analyzer installed in the 16700 mainframe

assembler is included on the Analysis Probe software diskette. After loading the above file, Load the file IAPCIE . This will configure the STATE Listing menu to include INVASM OPTIONS.

The 16600/16700 requires a special install procedure to install the PCI Inverse Assembler. To accomplish this, insert the diskette labeled 16600/16700 ANALYSIS PROBE INSTALL DISK FOR THE FS2001 into the 16600/700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*, once the title appears select it and then select *INSTALL*.

This procedure does not need to be repeated. It only needs to be done the first time the PCI Probe Adapter is used.

Once the software is installed you may load the configuration file from /configs/FuturePlus/FS2001 directory. The table below lists the configuration files.

Setting up the 1680/90/900 Analyzer

The 1680/90/900 Analyzer is a PC based application that requires a PC running the Windows OS or a 16900 frame.

Before installing the protocol decoder for the PCI protocol on a PC you **must** install the Agilent logic analyzer software. Once the Agilent logic analyzer software is installed, you can install the FS2001 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the .exe file on the CD-ROM disk and then double click the .exe file name from within the File Explorer navigation panel.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe Adapter is used.

1680/90/900 Licensing

The PCI Inverse Assembler is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

Loading 1680/90/900 configuration files and the General Purpose Probe feature

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

16700 and 1680/90/900 Configuration Files

167xx Analyzer	169xx Analyzer	File name for State/Timing	Comment
16715/6/7/9, 16750/1/2		CP201_4	32 Bit
16715/6/7/9, 16750/1/2		CP201_5	64 Bit
	1680/90, 16750/1/2, 1691x	CP201_6	32 Bit
	1680/90, 16750/1/2, 1691x	CP201_7	32/64 Bit
16550		F550PCI	32/64 Bit
16554/5/6/7		F555P64	64 Bit
16554/5/6/7		F555PCI	32 Bit

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

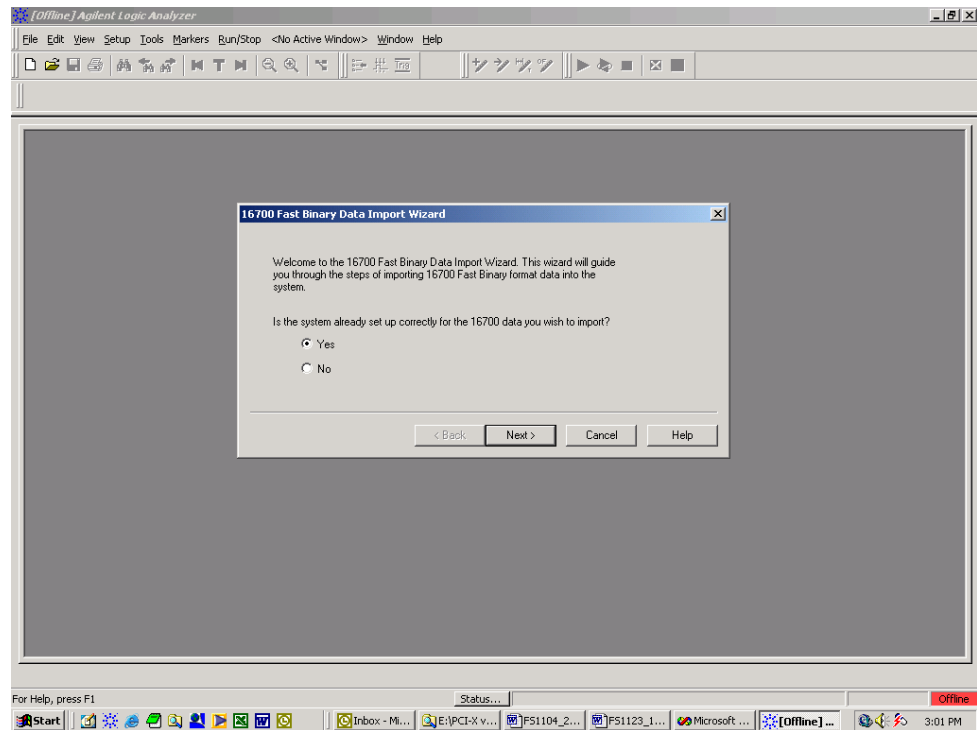
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may buy additional licenses, please contact FuturePlus sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up 1680/90/900 analyzer". Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

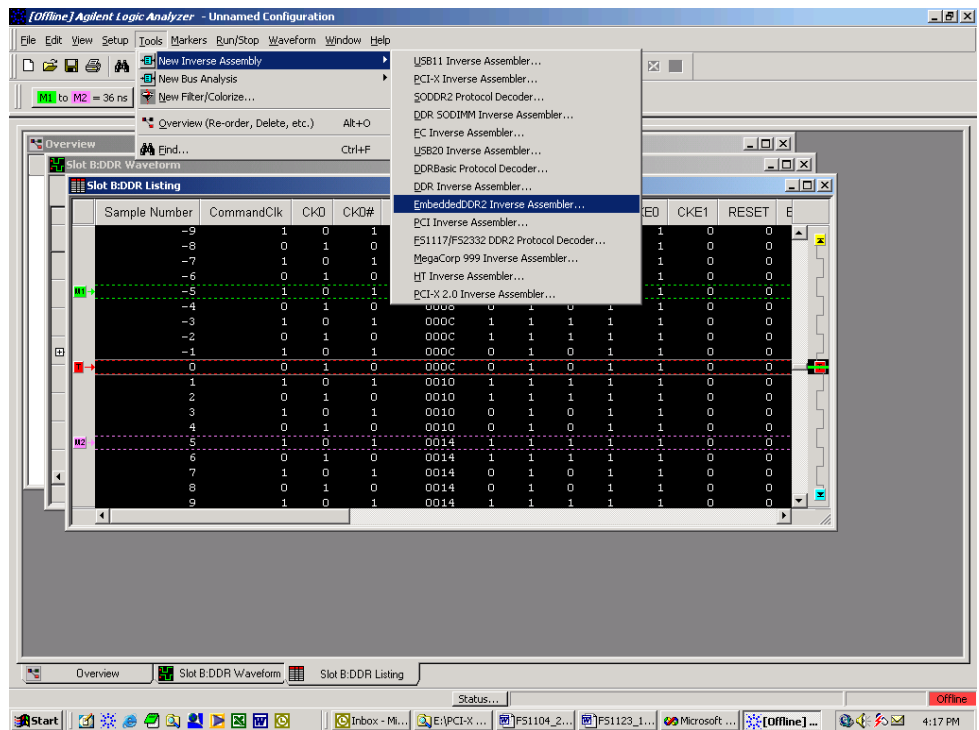
For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select “yes” when it asks if the system is ready to import 16700 data.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.



After the decoder has loaded, select Preferences if required, from the overview screen and set the preferences to their correct value in order to decode the trace properly. This is a general requirement, some decoders do not have preferences, if this is the case then no preference setting is necessary.

The Format Menu

The PCI Analysis Probe diskette sets up the format menu as shown in the following table. This format is the same for both Timing and State Analysis.

The 16510 Format will differ slightly. The STAT variable will be channels 11-0 on POD 4 and channels 14-0 on POD 3. The Format for the 16540/541 will also differ. The 541 PODS 1 and 2 will contain the data bits and the 16540 and the 16541 POD 3 will contain the status bits. In addition, the 16510 and the 16540/541 are only capable of 32 bit analysis due to having less than 6 PODS.

Label	Clk Inputs	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
STAT	M,K,J			8-0	14-0		
ADDR						15-0	15-0
ADDR_B		15-0	15-0				
USER7_1				15-9			
INTD_A					14-11		
RESET					10		
C/B7_0					9-6		
DATA						15-0	15-0
DEVSEL					5		
STOP					4		
LOCK					3		
PERR					2		
SERR					1		
PAR					0		
SD/SB0				8-7			
PAR64				2			
ACK/RQ				1-0			
IRDY	J			9			
FRAME	K			10			
TRDY	M			11			
PCICLK	L						

The STAT variable

The STAT variable is used by the PCI inverse assembler to decode PCI bus transactions. *It should not be changed or deleted from the format menu.* The signals that make up the STAT variable are listed in the following table. The STAT variable can be useful to set up SYMBOLS since it contains all of the key PCI control and status signals.

STAT Variable	PCI Bus Signal Name
Bit 26	TRDY#
Bit 25	FRAME#
Bit 24	IRDY#
Bit 23	SDONE
Bit 22	SB0#
Bit 21	C/BE7#
Bit 20	C/BE6#
Bit 19	C/BE5#
Bit 18	C/BE4#
Bit 17	PAR64#
Bit 16	ACK64#
Bit 15	REQ64#
Bit 14	INTD#
Bit 13	INTC#
Bit 12	INTB#
Bit 11	INTA#
Bit 10	RESET#
Bit 9	C/BE3#
Bit 8	C/BE2#
Bit 7	C/BE1#
Bit 6	C/BE0#
Bit 5	DEVSEL#
Bit 4	STOP#
Bit 3	LOCK#
Bit 2	PERR#
Bit 1	SERR#
Bit 0	PAR

The ADDR, ADDR_B and DATA variables

The ADDR variable is the lower 32 bits of the PCI AD bus. The ADDR_B is the upper 32 bits of the PCI AD bus. The DATA variable is a dummy variable that needs to be defined for the PCI inverse assembler. *These variables should not be changed or deleted from the format Menu.*

The CYCLE variable

The CYCLE variable is made up of the following PCI signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL# and STOP#. This variable has 30 symbols defined that can be used to help make triggering, timing analysis and pattern filtering (16505A) easier. The following lists the bit pattern and the corresponding symbol.

Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP
INTACK	1	0	1	0000	1	1
SPEC_CYC	1	0	1	0001	1	1
I/O_RD	1	0	1	0010	1	1
I/O_WR	1	0	1	0011	1	1
RESVRD	1	0	1	0100	1	1
RESVRD	1	0	1	0101	1	1
MEM_RD	1	0	1	0110	1	1
MEM_WR	1	0	1	0111	1	1
RESRVD	1	0	1	1000	1	1
RESRVD	1	0	1	1001	1	1
CON_RD	1	0	1	1010	1	1
CON_WR	1	0	1	1011	1	1
MEMRDM	1	0	1	1100	1	1
DAD_CY	1	0	1	1101	1	1
MEMRDL	1	0	1	1110	1	1
MEMWRI	1	0	1	1111	1	1
IO_XACTION	1	0	1	001X	1	1
MEM_XACTION	1	0	1	011X	1	1
CONFIG_XACTION	1	0	1	101X	1	1
ADD_CYCLE	1	0	1	XXXX	1	1

Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP
DATA_XFER	0	0	0	XXXX	0	1
WAIT_TARGET	1	X	0	XXXX	0	1
WAIT_INITIATOR	0	X	1	XXXX	0	1
DATA_FINALXFER	0	1	0	XXXX	0	1
STOP_NOXFER	X	0	1	XXXX	0	0
STOP_DATAXFER	0	X	0	XXXX	0	0
STOP_RETRY	1	1	0	XXXX	0	0
TARGET_ABORT	1	0	1	XXXX	1	0
IDLE	X	1	1	XXXX	X	X
WAIT_NODEVSEL	X	X	0	XXXX	1	1

State Analysis

Installation Quick Reference

This chapter explains how to configure the PCI Analysis Probe to perform state analysis on the PCI Local Bus. The configuration software on the flexible diskette sets up the format specification menu of the logic analyzer for compatibility with the PCI Local Bus. The next chapter explains how to configure the PCI Analysis Probe to perform timing analysis.

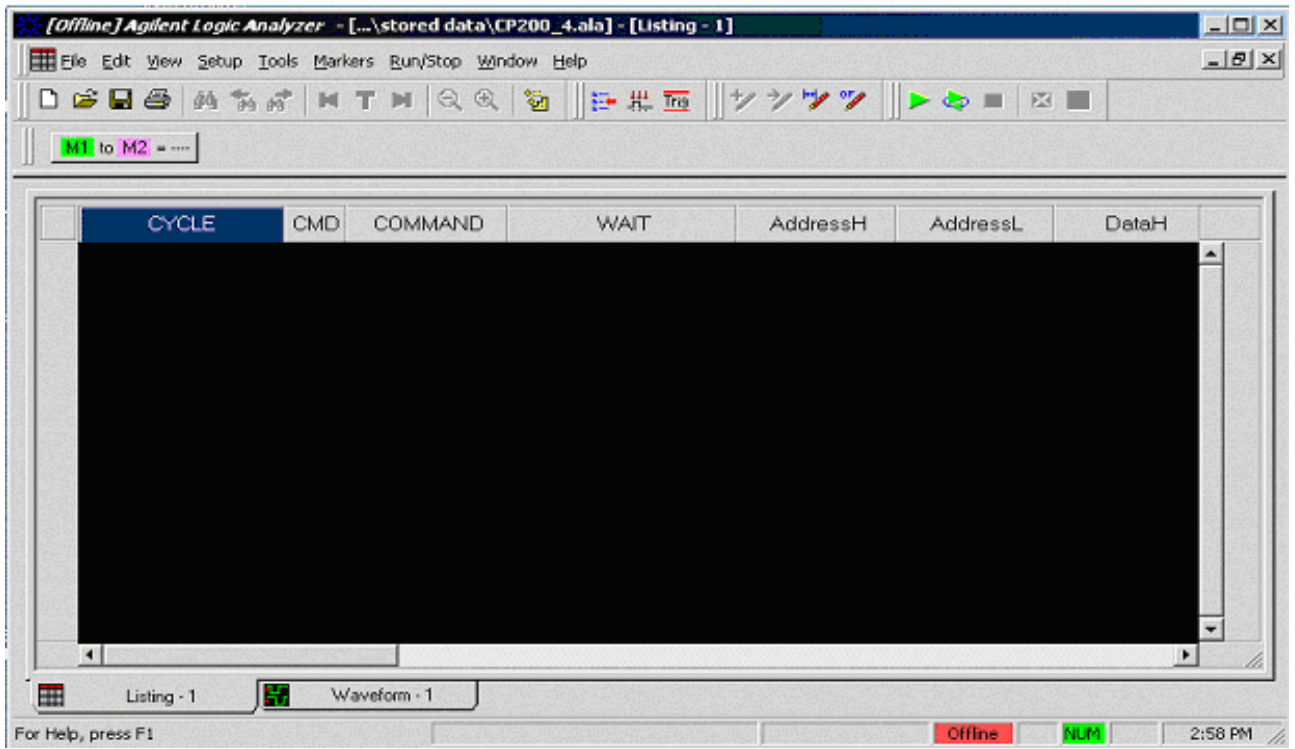
The following procedure describes the major steps required to perform measurements with the PCI Analysis Probe module.

1. Set the jumpers to the appropriate position on the PCI Analysis Probe module. See page 9 of this manual for details.
2. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe cable headers. See page 9 of this manual for details.
3. Install the PCI Analysis Probe module into a slot in the target PCI Local bus.
4. Load the logic analyzer configuration file by loading the appropriate file from the Analysis Probe interface diskette. See page 11 of this manual for details.

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Slow or Missing Clock" when the data is not being transmitted across the bus.



Capture Data Figure from 1680/90/900

The State Display

Captured data is as shown in the following figure. The below figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

16500 Display

100/500MHz LA E

Listing 1

Print

Run

Markers
Time

Trig to X
0 s

Trig to 0
0 s

X to 0
0 s

Label>	PCI BUS TRANSACTIONS	Time	C/B3_0
Base>	REV 2.2	Relative	Hex
242	D32=xxxxxxx08	296 ns	E
243	I/O READ ADR=00000073	9.072 us	2
244	D32=23xxxxxxx	1.096 us	7
245	I/O WRITE ADR=00000020	10.97 us	3
246	D32=xxxxxxx20	168 ns	E
247	INTERRUPT ACK CYCLE	54.90 ms	0
248	D32=xxxxxxx08	296 ns	E
249	I/O READ ADR=00000073	9.904 us	2
250	D32=23xxxxxxx	1.128 us	7
251	I/O WRITE ADR=00000020	10.97 us	3
252	D32=xxxxxxx20	168 ns	E

16700 Display

Listing<3>

File Edit Options Invasm Source Help

Navigate Run

Search Goto Markers Comments Analysis Mixed Signal

Label ACK/RQ Value when Present Next Prev

Advanced searching... Set G1 Set G2

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	INTD.
Decimal	PCI BUS TRANSACTIONS REV 2.8	Symbols	Relative	Hex
27	FUNC=0 REG OFFSET=4C TYPE=00 D32=xxxx00xx	DATA_FINALXF	188.000 ns	F
28	CONFIG WR ADR=0000404C	CON_WR	312.000 ns	F
30	FUNC=0 REG OFFSET=4C TYPE=00 D32=xxxxxx48	DATA_FINALXF	184.000 ns	F
31	CONFIG READ ADR=0000404C	CON_RD	220.000 ns	F
33	FUNC=0 REG OFFSET=4C TYPE=00 D32=xxxxxx48	DATA_FINALXF	156.000 ns	F
34	I/O WRITE ADR=00008020	I/O_WR	252.000 ns	F
38	D32=xxxxxx18	DATA_FINALXF	656.000 ns	F
39	I/O WRITE ADR=00008021	I/O_WR	220.000 ns	F
43	D32=xxxx6Axx	DATA_FINALXF	780.000 ns	F
44	I/O WRITE ADR=00008022	I/O_WR	188.000 ns	F
48	D32=xx29xxxx	DATA_FINALXF	812.000 ns	F
49	I/O WRITE ADR=00002400	I/O_WR	312.000 ns	F
53	D32=xxxxxx37	DATA_FINALXF	688.000 ns	F
54	I/O WRITE ADR=00006008	I/O_WR	6.262 ns	F
58	D32=xxxxxx0C	DATA_FINALXF	656.000 ns	F

1680/90/900 Display

[Offline] Agilent Logic Analyzer - [...\stored data\CP200_4.ala] - [Listing - 1]

File Edit View Setup Tools Markers Run/Stop Window Help

M1 to M2 = 4.95 ns

LE	CMD	COMMAND	WAIT	AddressH	AddressL	DataH	DataL	Termination	Term_Code
4B	0002	I/O Read							
BB	0002		Wait-No DEVSEL						
B9	0002						xxxxxx36	Initiator	0
4B	0002	I/O Read			00000040				
BB	0002		Wait-No DEVSEL						
B8	0002							STOP Retry	3
4B	0002	I/O Read			00000040				
BB	0002		Wait-No DEVSEL						
B9	0002						xxxxxx17	Initiator	0
4F	0003	I/O Write			00000021				
B7	0003		Wait-No DEVSEL						
B5	0003						xxxxFCxx	Initiator	0
4F	0003	I/O Write			000000A1				
B7	0003		Wait-No DEVSEL						
M1	B5	0003					xxxxFDxx	Initiator	0
M2	47	0001	Spec Cyc						
83	0001	Cmd=Halt, M...			00000001				
83	0001		Wait-No DEVSEL						
83	0001		Wait-No DEVSEL						
83	0001		Wait-No DEVSEL					Mstr Abort	4
43	0000	Int Ack			00000000				
9B	0000		Wait-No DEVSEL						
99	0000						50xxxx50	Initiator	0
4F	0003	I/O Write			00000021				
B7	0003		Wait-No DEVSEL						
B5	0003						xxxxFDxx	Initiator	0
4F	0003	I/O Write			00000020				
BB	0003		Wait-No DEVSEL						
B9	0003						xxxxxx60	Initiator	0
4F	0003	I/O Write			00000021				
B7	0003		Wait-No DEVSEL						

Listing - 1 Waveform - 1

For Help, press F1 Offline NUM 3:11 PM

Error Messages

The following error messages are reported by the PCI inverse assembler.

ERROR-NO DEVICE SELECTED

This error is displayed during a non special cycle data phase when IRDY and TRDY are asserted and DEVSEL is not asserted.

ERROR DEVSEL ASSERTED

This error is displayed during a special cycle data phase if DEVSEL is asserted.

SYSTEM ERROR

This error is displayed anytime SERR# is asserted.

1680/90 Errors:

XXX input label could not be attached to.

This error is displayed when the 1680/90 IA is being started and a failure occurs during the creation of an input label/column.

XXX: input label invalid Min/Max parameters.

This error is displayed during the creation of a label/column. The IA expects the label/column to fall within a min/max number of bits which has been violated.

XXX: Failed to unattach from label

This error is displayed when the 1680/90 IA is being exited and a failure occurs during the label/column destruction

XXX: output label could not be created.

This error is displayed when the 1680/90 IA is being started and a failure occurs when an output label/column is being constructed

XXX: symbol could not created.

This error is displayed when the 1680/90 IA is being started and a failure occurs when an output or input label/column symbol could not be created

XXX: Could not save Label

This error is displayed when the 1680/90 IA configuration file is being created and/or updated. The configuration data for the specified label could not be written to the file and thus will be lost.

XXX: Could not load Label

This error is displayed when the 1680/90 IA configuration file is being read. The configuration data for the specified label could not be read to the file and thus will be lost.

INVASM OPTIONS

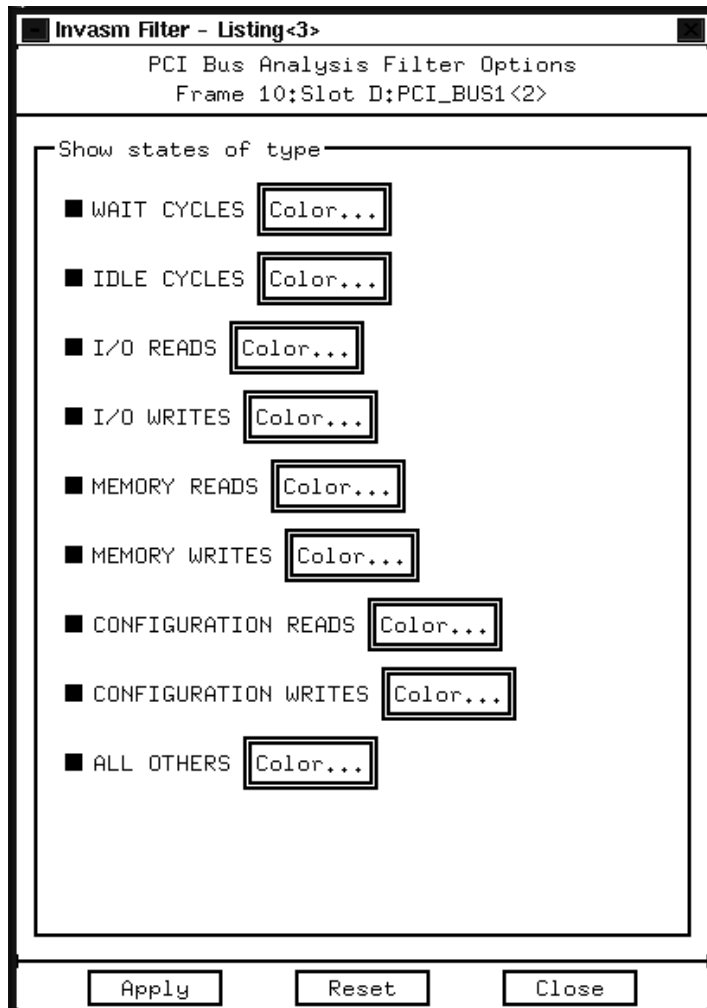
INVASM OPTIONS is available with the following logic analyzers.

- 16550A in a 16500B main frame
- 16540/541 in a 16500B main frame
- 166x, 167x series with 2.0 system software
- 16700 logic analysis system

1680/90 does not implement an INVASM Options menu.

INVASM OPTIONS can be invoked on the 16500 by selecting INVASM OPTIONS from the state listing display. The following selection will be displayed. For 16700 users select filter under INVASM in the state listing.

16700 Display showing invasm options



The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the show/suppress button to the right of the transaction cycle list.

For **1680/90** users, select the Filter/Colorization pull down menus in the state listing and create a filter (downstream) tool.

The **1680/90** IA allows filtering provides similar filtering capabilities as is provided in the 16700/702 environments. You may filter on any label, when using the filter tags label you can select symbols to make choosing transactions easier. To create a filter, choose Tools->New->Filter/Colorize. Then fill in the information on the window that opens up. You must create a new filter for each item you want filtered. To remove filters that you no longer want, go to Tools->Overview and then choose the filter you want removed and click Delete.

Using the PC Mapper Inverse Assembler

The PCI Analysis Probe PC Mapper software is an enhanced version of the PCI Analysis Probe inverse assembler and is for use only with PCI Analysis Probe from FuturePlus Systems Corporation. The enhancement includes PCI I/O and memory address decode to indicate common PC access.

PC Mapper is currently not available on the **1680/90**.

Setting up the Analyzer from the diskette

After the configuration file is loaded the PCI PC Mapper software can be loaded:

1. Install the PCI Analysis Probe software flexible diskette in the disk drive of the logic analyzer.
2. Configure the menu to "Load" the analyzer with the appropriate file (see table).

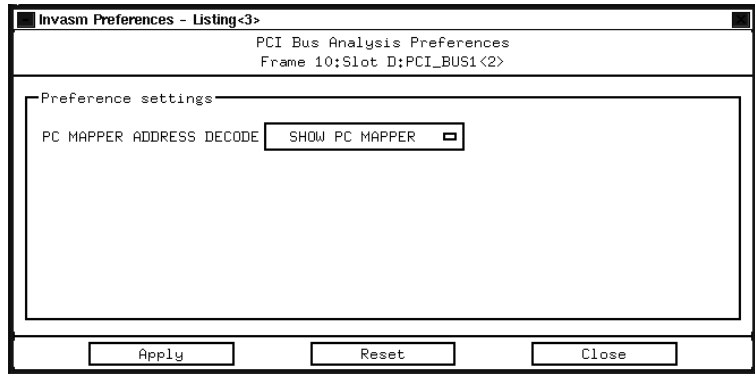
Logic Analyzer	File name
16500B mainframe with 16555, 16550A, or 16540/541 logic analyzer	IAPCIMPE
16500B mainframe with 16510	IAPCIMP
16500A mainframe (all logic analyzer models)	IAPCIMP
166x, 167x series (with REV 2.2 system software or later)	IAPCIMPE
165x logic analyzers	IAPCIMP

3. Execute the load operation to load the file into the logic analyzer.

IAPCIE is the inverse assembler for all logic analyzers installed into the 16700 and is auto loaded when the configuration file is loaded.

Setting up the 16700 for PC Mapper

To select PC Mapper function on the 16700, select INVASM from the state listing display then select PREFERENCES. When you select PREFERENCES it will come up with a box and there you can choose to turn on PC Mapper or suppress PC Mapper. The picture below displays PC Mapper function enabled on the 16700.



Acquiring Data

Data can be acquired by touching the RUN button. As soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash “Slow or Missing Clock” if the PCI Clock signal is not being detected by the logic analyzer. In this case, check the logic analyzer to PCI Analysis Probe connection (refer to your User’s Manual).

The State Display with the PCI PC Mapper

Captured data is as shown in the following figure. The first figure displays the state listing after disassembly. The PCI PC Mapper is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

100/500MHz LA E
Listing 1
Invasm Options
Print
Run

Markers Time
Trig to X 0 s
Trig to 0 0 s
X to 0 0 s

Label>	PCI BUS TRANSACTIONS	Time	C/B3_0
Base>	PC MAPPER PRE-RELEASE VERSION	Relative	Hex
39	RTC/CMOS RAM DATA PORT I/O WRITE ADR=0000071 REQ64 D32=xxxx00xx	2.960 us	3
40		1.168 us	D
41	VIDEO MEMORY MEM WRITE ADR=000B81E0 REQ64	41.55 us	7
42	D32=xxxxxx30	72 ns	E
43	VGA CRT CNTRLR ADDR REG I/O WRITE ADR=000003D4 REQ64 D32=xxxx000E	4.832 us	3
44		264 ns	C
45	VGA CRT CNTRLR ADDR REG I/O WRITE ADR=000003D4 REQ64	440 ns	3
46	D32=xxxxF10F	264 ns	C

The above display data using the PCI Inverse Assembly software without the PCI PC Mapper functionality is shown as follows.

100/500MHz LA E Listing 1 Invasm Options Print Run

Markers Time Trig to X 0 s Trig to 0 0 s X to 0 0 s

Label>	PCI BUS TRANSACTIONS		Time	C/B3_0
Base>	REV 2.2		Relative	Hex
37	I/O WRITE ADR=00000070	REQ64#	1.200 us	3
38	D32=xxxxxx8F		1.072 us	E
39	I/O WRITE ADR=00000071	REQ64#	2.960 us	3
40	D32=xxxx00xx		1.168 us	D
41	MEM WRITE ADR=000B81E0	REQ64#	41.55 us	7
42	D32=xxxxxx30		72 ns	E
43	I/O WRITE ADR=000003D4	REQ64#	4.832 us	3
44	D32=xxxx000E		264 ns	C
45	I/O WRITE ADR=000003D4	REQ64#	440 ns	3
46	D32=xxxxF10F		264 ns	C
47	I/O WRITE ADR=00000070	REQ64#	4.064 us	3

Display with PC Mapper enabled on the 16700

Listing<4>

File Window Edit Options Invasm Source Help

Goto Markers Search Comments Analysis Mixed Signal

Label ACK/RQ Hex X when Present Next Prev

Advanced searching Set G1 Set G2

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	USR7_1
Decimal	PCI BUS TRANSACTIONS REV 2.8	Symbol	Absolute	Hex
0	SYSTEM MEMORY	MEM_RD	0 s	00
	MEM READ ADR=F3FC0000			
1	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	16.000 ns	00
2	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	28.000 ns	00
3	D32=12345678	DATA_FINALXF	88.000 ns	00
4	SYSTEM MEMORY	MEM_WR	111.687 ms	00
	MEM WRITE ADR=F3FC0004			
5	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111.687 ms	00
6	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111.687 ms	00
7	D32=9ABCDEF0	DATA_FINALXF	111.687 ms	00
8	SYSTEM MEMORY	MEM_RD	223.194 ms	00
	MEM READ ADR=F3FC0004			
9	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223.194 ms	00
10	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223.194 ms	00
11	D32=9ABCDEF0	DATA_FINALXF	223.195 ms	00

Display with PC Mapper suppressed on the 16700

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	USR7_1
Decimal	PCI BUS TRANSACTIONS REV 2.8	Symbols	Absolute	Hex
0	MEM READ ADR=F3FC0000	MEM_RD	0 s	00
1	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	16,000 ns	00
2	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	28,000 ns	00
3	D32=12345678	DATA_FINALXF	88,000 ns	00
4	MEM WRITE ADR=F3FC0004	MEM_WR	111,687 ms	00
5	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111,687 ms	00
6	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111,687 ms	00
7	D32=9ABCDEF0	DATA_FINALXF	111,687 ms	00
8	MEM READ ADR=F3FC0004	MEM_RD	223,194 ms	00
9	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223,194 ms	00
10	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223,194 ms	00
11	D32=9ABCDEF0	DATA_FINALXF	223,195 ms	00
12	MEM WRITE ADR=F3FC0008	MEM_WR	334,826 ms	00
13	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	334,826 ms	00
14	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	334,826 ms	00

Error Messages

The error messages reported by the PCI PC Mapper are the same as those reported with the standard non mapper version of the PCI Inverse Assembler.

PCI PC Mapping for memory transactions

This section lists the addresses, the commands and the corresponding mapping done by the PCI PC Mapper software. For information on the standard PCI configuration register mapping please refer to the PCI Local Bus Specification Rev 2.0.

Address bits 23-0	PC Mapper output
greater than 0FFFFFFH	System Memory
0FFFFFF-0E0000H	System BIOS
0DFFFF-0C0000H	ROM Scan
0BFFFF-0A0000H	Video Memory
09FFFF-000400H	System Memory
0003FF-000000H	See Interrupt Vector Table

Interrupt Vector Table

Address bits 23-0	PC Mapper output
0003C4H	INT #F1-FF USER PROGRAMS
000200H	INT #80-F0 BASIC
0001E0H	INT #78-7F USER PROGRAMS
0001DCH	INT #77 IRQ15
0001D8H	INT #76 IRQ14
0001D4H	INT #75 IRQ13
0001D0H	INT #74 IRQ12
0001CCH	INT #73 IRQ11
0001C8H	INT #72 IRQ10
0001C4H	INT #71 IRQ9
0001C0H	INT #70 IRQ8
0001A0H	INT #68-6F RESERVED
00019CH	INT #67 EXP MEM MANG
000180H	INT #60-66 USER PROGRAMS
00012CH	INT #4B-5F RESERVED
000128H	INT #4A USER RTC ALARM
00011CH	INT #47-49 RESERVED
000118H	INT #46 HD DISK #1 PARAM
000110H	INT #44-45 RESERVED
00010CH	INT #43 VIDEO CHAR TABLE
000108H	INT #42 EGA BIOS
000104H	INT #41 HD DISK #0 PARAM
000100H	INT #40 FLOPPY DISK ISR
000080H	INT #20-3F RESERVED DOS
00007CH	INT #1F VIDEO CHAR TABLE
000078H	INT #1E FLOPPY PARAMS
000074H	INT #1D AVAILABLE
000070H	INT #1C AVAILABLE
00006CH	INT #1B KEYBOARD BREAK
000068H	INT #1A RTC ISR
000064H	INT #19 BOOSTRAP LOADER
000060H	INT #18 ROM BASIC
00005CH	INT #17 LPT PRINTER BIOS
000058H	INT #16 KEYBOARD BIOS
000054H	INT #15 SYS SERVICE BIOS
000050H	INT #14 SERIAL PORT BIOS
00004CH	INT #13 FLOPPY DISK BIOS
000048H	INT #12 MEM SIZE INT
000044H	INT #11 EQUIP LIST
000040H	INT #10 VIDEO BIOS
00003CH	INT #0F IRQ7 LPT1
000038H	INT #0E IRQ6 FLOPPY DISK
000034H	INT #0D IRQ5 LPT2
000030H	INT #0C IRQ4 SERIAL #1
00002CH	INT #0B IRQ3 SERIAL #2
000028H	INT #0A IRQ2 SLAVE INT
000024H	INT #09 KEYBOARD
000020H	INT #08 IRQ0 SYS TIMER
00001CH	INT #07 NUM COPROCESSOR
000018H	INT #06 INVALID OPCODE
000014H	INT #05 PRINT SCREEN
000010H	INT #04 OVERFLOW DETECT

00000CH	INT #03 BREAKPOINT TRACE
Address bits 23-0	PC Mapper output
000008H	INT #02 NMI
000004H	INT #01 SINGLE STEP
000000H	INT #00 DIVIDE BY ZERO

PCI PC Mapping - I/O Transactions

Address bits 23-0	PC Mapper output
0000H	MSTR DMA CH 0
0001H	MSTR DMA CH 0
0002H	MSTR DMA CH 1
0003H	MSTR DMA CH 1
0004H	MSTR DMA CH 2
0005H	MSTR DMA CH 2
0006H	MSTR DMA CH 3
0007H	MSTR DMA CH 3
0008H	MSTR DMA STAT REG
0009H	UNKNOWN IO DEVICE
000AH	MSTR DMA MASK REG
000BH	MSTR DMA MODE REG
000CH	MSTR DMA CLR BYTE PTR
000DH	MSTR DMA MSTR CLEAR
000EH	MSTR DMA CLEAR MASK
000FH	MSTR DMA WRT MASK
0018H	MSTR DMA CH EXT FUNCT REG
001AH	MSTR DMA EXT FUNCT
0020H	MSTR INT REQ REG
0021H	MSTR INT REQ REG2
0040H	INTERVAL TIMER TIMER 0
0042H	INTERVAL TIMER SPKR TIMER
0043H	INTRVAL TIMER #1 CNTRL
0044H	INTERVL TIMER #2 WATCHDOG
0047H	INTERVAL TIMER #2 CNTRL
0060H	KEYBOARD/MOUSE DATA PORT
0061H	SYSTEM CONTOL PORT B
0064H	KEYBOARD/MOUSE CMD PORT
0070H	RTC/CMOS RAM ADDR PORT
0071H	RTC/CMOS RAM DATA PORT
0074H	EXT CMOS RAM ADDR PORT
0075H	EXT CMOS RAM ADDR PORT
0076H	EXT CMOS RAM DATA PORT
0081H	CH 2 DMA PAGE REGISTER
0082H	CH 3 DMA PAGE REGISTER
0083H	CH 1 DMA PAGE REGISTER
0087H	CH 0 DMA PAGE REGISTER
0089H	CH 6 DMA PAGE REGISTER
008AH	CH 7 DMA PAGE REGISTER
008BH	CH 5 DMA PAGE REGISTER
008FH	CH 4 DMA PAGE REGISTER
0090H	ARB CNTRL POINT REG
0091H	FEEDBACK REG
0092H	SYSTEM CONTROL PORT A
0094H	SYS SETUP/CARD ENABLE REG
0096H	ADAPTOR SETUP/ENABLE REG
00A0H	SLAVE INTERRUPT CNTRLR
00A1H	SLAVE INTERRUPT CNTRLR
00C0H	SLAVE DMA CH4 MEM ADDR
00C2H	SLAVE DMA CH4 TRANS COUNT
00C4H	SLAVE DMA CH5 MEM ADDR
00C6H	SLAVE DMA CH5 TRANS COUNT

00C8H	SLAVE DMA CH6 MEM ADDR
Address bits 23-0	PC Mapper output
00CAH	SLV DMA CH6 TRANS COUNT
00CCH	SLAVE DMA CH7 MEM ADDR
00CEH	SLAVE DMA CH7 TRANS COUNT
00D0H	SLV DMA STATUS REG CH 4-7
00D4H	SLV DMA MASK REG CH 4-7
00D6H	SLAVE DMA MODE REG CH 4-7
00D8H	SLAVE DMA CLEAR BYTE PNTR
00DAH	SLAVE DMA MASTER CLEAR
00DCH	SLV DMA CLR MASK CH 4-7
00DEH	SLAVE DMA WRITE MASK REG
00E0H	IBM MODELS - ENCODE REG
00E1H	IBM MODELS - ENCODE REG
00F1H	NUMERIC COPROCESSOR RESET
00F8H	NUMERIC COPROCESSOR PORT
00F9H	NUMERIC COPROCESSOR PORT
00FAH	NUMERIC COPROCESSOR PORT
00FBH	NUMERIC COPROCESSOR PORT
00FCH	NUMERIC COPROCESSOR PORT
0100H	ADAPTER CARD POS REG 0
0101H	ADAPTER CARD POS REG 1
0102H	SYS BD/ADP CD POS REG 2
0103H	SYS BD/ADP CD POS REG 3
0104H	ADAPTER CARD POS REG 4
0105H	ADAPTER CARD POS REG 5
0106H	ADAPTER CARD POS REG 6
0107H	ADAPTER CARD POS REG 6
0278H	PARALLEL PORT 3 DATA PORT
0279H	PARALLEL PORT 3 STAT PORT
027AH	PARALLEL PORT 3 CMD PORT
02F8H	SERIAL PORT 2 XMIT/REC
02F9H	SER PORT 2 DIV LATCH/INT
02FAH	SERIAL PORT 2 INT ID REG
02FBH	SERIAL PORT 2 CNTRL REG
02FDH	SERIAL PORT 2 MODEM CNTRL
02FEH	SERIAL PORT 2 MODEM STAT
02FFH	SERIAL PORT 2 SCRTCH REG
0378H	PARALLEL PORT 2 DATA PORT
0379H	PARALLEL PORT 2 STAT PORT
037AH	PARALLEL PORT 2 CMD PORT
03B4H	VGA CRT CNTRLR ADDR REG
03B5H	VGA CRT CNTRLR DATA REG
03BAH	VGA STAT 1/FEATURE CNTRL
03BCH	PARALLEL PORT 1 DATA PORT
03BDH	PARALLEL PORT 1 STAT PORT
03BEH	PARALLEL PORT 1 CMD PORT
03C0H	VGA ATTRIBUTE CNTRLR ADDR
03C1H	VGA ATTRIBUTE CNTRLR DATA
03C2H	VGA OUTPUT/STAT REG
03C3H	VGA VIDEO SUBSYSTEM ENABLE
03C4H	VGA SEQUENCER ADDR REG
03C5H	VGA SEQUENCER DATA REG

03C6H	VIDEO DAC PEL MASK
03C7H	VIDEO DAC PAL ADDR/STAT
Address bits 23-0	PC Mapper output
03C8H	VIDEO DAC PAL ADDR/WRITE
03C9H	VIDEO DAC PALETTE DATA
03CAH	VGA FEATURE CONTROL REG
03CCH	VGA MISC OUTPUT REG
03CEH	VGA GRAPHICS CONTROL ADDR
03CFH	VGA GRAPHICS CONTROL ADDR
03D4H	VGA CRT CONTROL ADDR REG
03D5H	VGA GRAPHICS CONTROL DATA
03DAH	VGA COLOR STAT 1/FEATURE
03F0H	FLOPPY STATUS REG A
03F1H	FLOPPY STATUS REG B
03F2H	FLOPPY DIGITAL OUTPUT REG
03F4H	FLOPPY DISK CONTROL STAT
03F5H	FLOPPY DISK CONTROL DATA
03F7H	FLOPPY CONFIG CONTROL REG
03F8H	SERIAL PORT 1 XMIT/RCV BUF
03F9H	SER PORT 1 DIV LATCH/INT
03FAH	SERIAL PORT 1 INT ID/FIFO
03FBH	SERIAL PORT 1 LINE CONTROL
03FCH	SERIAL PORT 1 MODEM CONTROL
03FDH	SERIAL PORT 1 STAT REG
03FEH	SERIAL PORT 1 MODEM STAT
03FFH	SERIAL PORT 1 SCRATCH REG
0680H	MANUFACTURING CHECKPOINT PORT

Timing Analysis

Installation Quick Reference

Since the PCI Analysis Probe interface contains only passive matching terminators it introduces negligible skew to the PCI Local Bus signals.

The following procedure describes the major steps required to perform timing analysis measurements with the PCI Analysis Probe module.

1. Set the jumpers to the appropriate position on the PCI Analysis Probe module. See page 9 of this manual for details.
2. After removing the probe tip assemblies, plug the logic analyzer cables into the Analysis Probe cable headers. See page 9 of this manual for details.
3. Install the PCI Analysis Probe module into a slot in the target PCI Local bus.
4. Load the logic analyzer configuration file by loading the appropriate file. See page 11 of this manual for details.

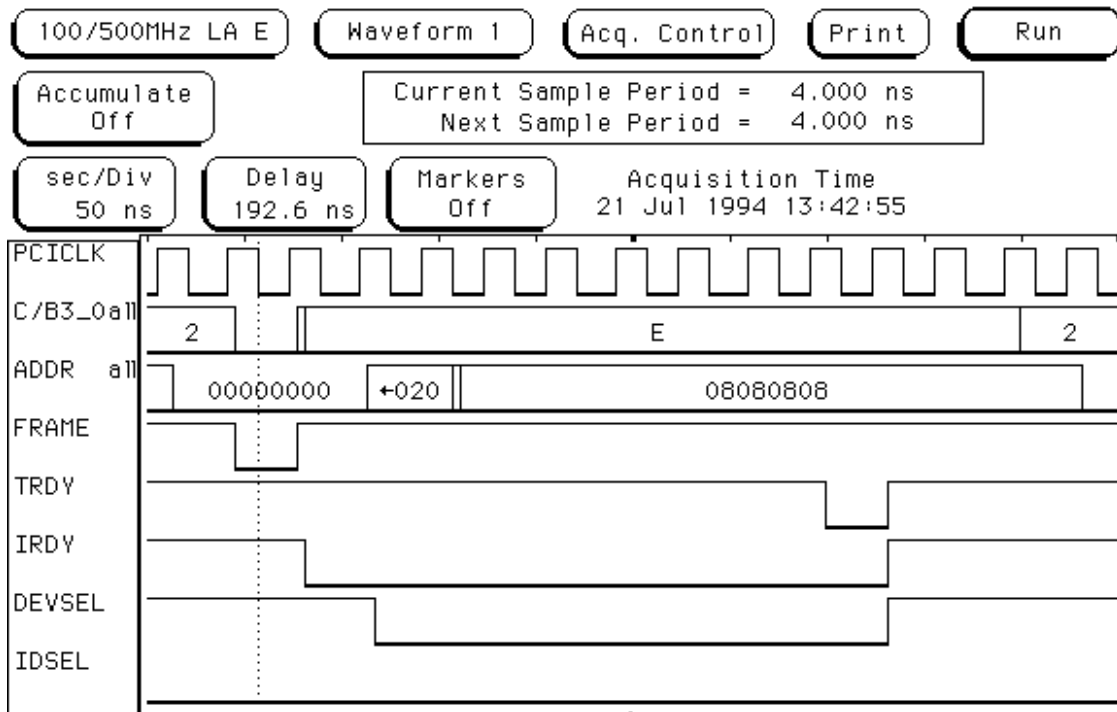
Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Waiting for Trigger" when the data is not being transmitted across the bus.

The Waveform Display

Captured data is displayed as shown in the following figure.



General Information

This chapter provides additional reference information including the characteristics and signal connections for the PCI Analysis Probe module.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the PCI Analysis Probe module.

Analysis Probe Interface Compatibility

32/64 bit PCI Local bus accepting the short card length and universal connector pinout. All PCI local bus ground pins of the universal board pinout are connected to the ground plane of the PCI Analysis Probe module.

JTAG Boundary Scan

The PCI Analysis Probe does not implement JTAG Boundary SCAN. Pins TDI and TBO (pins 4a and 4b) are connected together so the scan chain is not broken.

The PCI Present Pins

No connection is made to the PCI signals PRSNT1# and PRSNT2#.

Standards Supported

The PCI Local Bus Specification Revision 2.1

Power Requirements

The PCI Analysis Probe contains no active components and therefore requires no power.

Logic Analyzer Required

166x, 167x, 16550, 16510, 1650, 167xx

Number of Probes Used

32 bit PCI Local Bus - 4 cable headers

64 bit PCI Local Bus - 6 cable headers

Minimum Clock Period (State)

Not limited by the Analysis Probe. Clocking is specified by the logic analyzer.

Signal loading

Per the PCI Local Bus Specification the PCI Analysis Probe presents only one electrical load on each PCI bus signal. Some signals have multiple drops behind the 10pf /90 ohm termination but this does not change the electrical loading as seen from the PCI bus. All signal etch length, trace velocity and impedance is within specification.

Operations

All PCI Local Bus operations supported.

Environmental Temperature

Operating: 0 to 55 degrees C (+32 to +131 degrees F)

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Altitude

Operating: 4,600m (15,000 ft)

Non operating: 15,300m (50,000 ft)

Humidity

Up to 90% non condensing. Avoid sudden, extreme temperature changes which would cause condensation on the Analysis Probe module.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the PCI Analysis Probe module. If a failure is suspected in the PCI Analysis Probe module contact the factory or your FuturePlus Systems authorized distributor.

Servicing

The repair strategy for the PCI Analysis Probe is module replacement. However, if parts of the PCI Analysis Probe module are damaged or lost contact the factory for a list of replacement parts.

Signal Connections

The PCI Analysis Probe module monitors signals for both state and timing analysis. The below figure displays how the cable headers are numbered.

39 37 35 33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
40 38 36 34 32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2

The following tables list the PCI Analysis Probe cable headers and the corresponding PCI Local Bus signals after these signals have been terminated by the 90K ohm/10pf terminators.

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 1 pin 3	CLK/16	IRDY# visible here only on 166x, 167x/550
5	no connect	
7	15	AD15
9	14	AD14
11	13	AD13
13	12	AD12
15	11	AD11
17	10	AD10
19	9	AD09
21	8	AD08
23	7	AD07
25	6	AD06
27	5	AD05
29	4	AD04
31	3	AD03
33	2	AD02
35	1	AD01
37	0	AD00

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 2 pin 3	CLK/16	FRAME# visible here only on 166x, 167x/550
5	no connect	
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 3 pin 3	CLK/16	PCI Clock visible here only on 166x, 167x/550
5	no connect	
7	15	PCI Clock/510 only controlled by JMP 1
9	14	INTD#
11	13	INTC#
13	12	INTB#
15	11	INTA#
17	10	RST#
19	9	C/BE3#
21	8	C/BE2#
23	7	C/BE1#
25	6	C/BE0#
27	5	DEVSEL#
29	4	STOP#
31	3	LOCK#
33	2	PERR#
35	1	SERR#
37	0	PAR

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 4 pin 3	CLK/16	TRDY# visible here only on 166x, 167x/550
5	no connect	
7	15	USER7
9	14	USER6
11	13	USER5
13	12	USER4
15	11	USER3 FOR 166x, 167x AND 550 USERS TRDY# FOR 510 USERS
17	10	USER2 FOR 166x, 167x AND 550 USERS FRAME# FOR 510 USERS
19	9	USER1 FOR 166x, 167x AND 550 USERS IRDY# FOR 510 USERS
21	8	SDONE
23	7	SBO#
25	6	C/BE7#
27	5	C/BE6#
29	4	C/BE5#
31	3	C/BE4#
33	2	PAR64
35	1	ACK64#
37	0	REQ64#

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 5 pin 3	CLK/16	
5	no connect	
7	15	AD47
9	14	AD46
11	13	AD45
13	12	AD44
15	11	AD43
17	10	AD42
19	9	AD41
21	8	AD40
23	7	AD39
25	6	AD38
27	5	AD37
29	4	AD36
31	3	AD35
33	2	AD34
35	1	AD33
37	0	AD32

Analysis Probe Cable Header and Pin number	Logic Analyzer channel number	PCI Signal name
Header 6 pin 3	CLK/16	
5	no connect	
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48