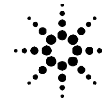


FuturePlus Systems Corporation



Agilent Technologies
Innovating the HP Way

Premier Solution Partner

FS1123/4 Embedded DDR2 Analysis Software

Users Manual

For use with Agilent Technologies Logic Analyzers

Revision 1.1

FuturePlus is a registered trademark of FuturePlus Systems Corporation

Copyright 2004 FuturePlus Systems Corporation

How to reach us	3
Software License Agreement	4
Use of the Software	4
Ownership	4
Sublicensing and Distribution	4
Termination.....	5
Export Clause	5
Limitation of warranty.....	5
Exclusive Remedies	5
Introduction	6
Theory of Operation.....	6
Unique DDR2 Probing Considerations	6
Getting Started	8
Product Components	8
Logic Analyzer Card Definitions and Requirements.....	8
Logic Analyzer Card Configuration Options.....	10
Configuration files	11
Signal Naming Conventions	12
Setting up the FS1123 software on the 167xx Analyzer	12
16700 Licensing	12
Setting up the 16700 Inverse Assembler	13
Setting up the FS1124 software on the 16900 Analyzer.....	15
16900 Licensing	15
Pod Attachment for the 169xx	15
Threshold Considerations for Tristate.....	17
Cross Bus Analysis.....	17
EyeScan Operation.....	17
Symbols.....	19
Offline Analysis	20
Timing Analysis	23
Pod Attachment for Timing Analysis	23
Acquiring Data	23
Sample Waveform Display	24
State Analysis	25
Pod Attachment for State Analysis	25
Missing or slow clock.....	26
Calibration	27
State analysis calibration procedure	27
Acquiring Data in State Mode	34
General Information	36
Signal Connections.....	36

How to reach us

For Technical Support:

FuturePlus Systems Corporation

36 Olde English Road

Bedford NH 03110

TEL: 603-471-2734

FAX: 603-471-2738

On the web <http://www.futureplus.com>

For Sales and Marketing Support:

FuturePlus Systems Corporation

TEL: 719-278-3540

FAX: 719-278-9586

On the web <http://www.futureplus.com>

FuturePlus Systems has technical sales representatives in several major countries. For an up to date listing please see

<http://www.futureplus.com/contact.html>.

Agilent Technologies is also an authorized reseller of many FuturePlus products. Contact any Agilent Technologies sales office for details.

Software License Agreement

IMPORTANT Please read this license agreement before opening the media envelope. Rights in the software are offered only on the condition that the customer agrees to all terms and conditions of the license agreement. Opening the media envelope indicates your acceptance of these terms and conditions. If you do not agree to the licensing agreement, you may return the unopened package for a full refund.

In return for payment for this product, FuturePlus Systems grants the Customer a SINGLE user LICENSE in the software subject to the following:

Use of the Software

Customer may use the software on any one Agilent 1670x mainframe logic analysis system(FS1123) or any one 16900 mainframe logic analysis system (FS1124).

- Customer may not reverse assemble or decompile the software.

Customer may make copies or adaptations of the software:

- For archival purpose only
- When copying for adaptation is an essential step in the use of the software with the logic analyzer and/or logic analysis mainframe so long as the copies and adaptations are used in no other manner. Customer has no right to copy software unless it acquires an appropriate license to reproduce from FuturePlus Systems.

Ownership

- Customer agrees that it does not have any title or ownership of the software, other than the physical media.
- Customer acknowledges and agrees that the software is copyrighted and protected under the copyright laws.
- Transfer of the right of ownership shall only be done with the consent of FuturePlus Systems.

Sublicensing and Distribution

Customer may not sublicense the software or distribute copies of the software to the public in physical media, or by electronic means, or any other means without the prior written consent of FuturePlus Systems.

Termination FuturePlus Systems may terminate this software license for failure to comply with any of these terms provided FuturePlus Systems has requested the Customer to cure the failure and Customer has failed within 30 days of such notice.

Export Clause Customer agrees not to export or re-export the software or any copy or adaptation in violation of the U.S. Export Administration regulations or other applicable regulation.

Limitation of warranty

FuturePlus Systems warrants that its software designated by FuturePlus Systems for use with an instrument will execute its programming instructions when properly installed on that instrument. FuturePlus Systems does not warrant that the operation of the software will be uninterrupted or error-free.

The foregoing warranty shall not apply to defects resulting from improper or inadequate use by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. FUTUREPLUS SYSTEMS SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Exclusive Remedies

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. FUTUREPLUS SYSTEMS SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

Assistance

Product maintenance agreements and other customer assistance agreements are available for FuturePlus Systems products. For assistance, contact FuturePlus Systems.

Introduction

Thank you for purchasing the FuturePlus Systems FS1123/4 Embedded DDR2 DRAM solution. This is a software product that can be used with either a Samtec or soft touch connector designed into a target DDR2 bus. The embedded DDR2 solution, in conjunction with the Agilent Technologies Logic Analyzer, is a valuable tool to debug a system. This user manual will provide the information you need to install, configure, and use the solution. The solution can accommodate DDR2 DRAMs up to 1Gb X 32.

Theory of Operation

FuturePlus Systems FS1123/4 Embedded DDR2 SDRAM software license provides logic analyzer configuration and transaction level decode of the DDR2 SDRAM memory bus traffic. The transaction decode software includes all data, commands, and ECC signals.

The Embedded DDR2 solution, FS1123/4, can work with an embedded Samtec or soft touch connector. The design of the connectors onto a target board is covered in the FuturePlus Systems Application Note “**Embedded Probing of DDR SDRAM Applications**”. The suggested pinout is covered in a separate document as well as in the back of this manual.

The analyzer is clocked on both edges of the DDR2 clock. Chip Select is used to qualify commands on the bus. The software decodes transactions from the user provided CAS latency and burst size values and copies the valid data under the correct Read or Write command.

Users must use timing zoom in order to adjust the setup/hold values for capturing simultaneous Reads and writes. The calibration procedure is outlined later in the manual.

Unique DDR2 Probing Considerations

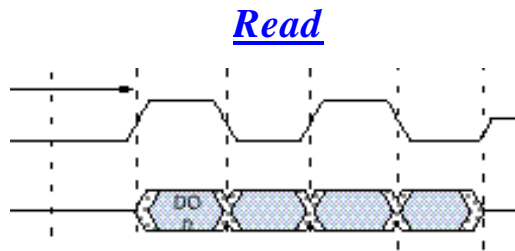
DDR2 has a differential clock, CK0/CK0#. For the purpose of discussion in this document, the crossing of CK0 and CK0# will be considered to be the mid-point of CK0 rising.

DDR2 can be thought of as consisting of two buses; the Command bus and the Data bus. The DDR2 command bus is clocked on the rising edge of CK0. State or timing analysis of the Command bus does not require any special considerations for logic analyzer operation.

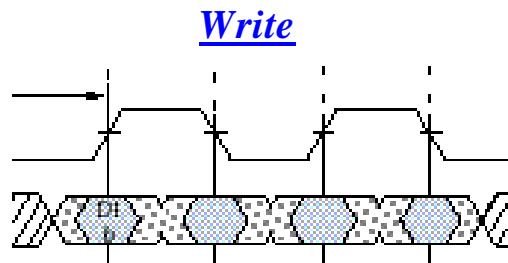
Strobe edges straddle the Data on Reads and are centered about Data on Writes. State mode analysis of the data bus requires special considerations, which are covered in the State Analysis section. Timing analysis of the data bus does not require special clocking considerations for proper logic analyzer operation.

DDR Timing Differences for Read or Write

- Strobe edges straddle data for READ



- Strobe edges centered on data for WRITE



Getting Started

This section introduces you to the Embedded DDR2 solution and lists the equipment required for DDR2 analysis.

Product Components

- FS1123 - Installation diskette with the protocol decoder and configuration files for 167xx analyzers.

or

- FS1124 - CD-ROM containing software for 1680/90/900 analyzers or offline analysis.
- SW License Entitlement Certificate

Additional equipment that must be ordered separately:

- Termination adapters for Samtec or Soft Touch connectors

For customers who put their own connectors down please refer to our application note “Embedded Probing of DDR SDRAM Applications” for routing information.

Logic Analyzer Card Definitions and Requirements

Logic Analyzer Modules – “Module” – A set of logic analyzer card(s) that have been configured (via cables connecting multiple cards) to operate as a single logic analyzer whose total available channels is the sum of the channels on each card. A trigger within a module can be specified using all of the channels of that module. Each module may be further broken up into “Machines.” A single module may not extend beyond a single 5 card 16700 frame.

Logic Analyzer Machines – “Machine” – A set of logic analyzer pods from a logic analyzer module grouped together to operate as a single state or timing analyzer. Each logic analyzer module may be partitioned into two independent “Machines” (either two state machines, or state and a timing machine), and the pods of a module may be assigned freely to either machine. Each state analyzer machine has its own state clock. Cross triggering between modules or machines is done via the Intermodule Bus or via the Flag bits, which will communicate across a 16700 frame and its expander, or across multiple frames if the Multiframe product is used. Turbo mode (333Mhz for 1671x or 400Mhz for 1675x cards) operation restricts a module to having only one machine.

Logic Analyzer Requirements – When using the 16700 analyzer, 16750A through 16756A modules will work for the solutions described in this manual, FuturePlus recommends using 16753A modules or better. The analyzer must be running A.02.80.00 or better operating system.

When using the 16900 analyzer, 1695x or 16753/6 modules are recommended.

Probing DDR2 generally requires two to four logic analyzer cards depending on the bus speed, whether state or timing measurements are being used, and the type of logic analyzer card being used. For full channel timing measurements, only two cards (configured as a single logic analysis module using one analyzer “machine”) are necessary.

When the analyzer is running in turbo mode you must leave 2 pod pairs unused. This mode is required at speeds above:

- 200 Mhz for 16750 - 2 cards
- 300 Mhz for 16753 - 6 cards
- 250 MHz for 16910 - 1 cards
- 300 Mhz for 16950 cards

Logic Analyzer Card Configuration Options

DDR2 Bus Speed	16900 Analyzer Type	16700 Analyzer Type	Timing Analysis	State Analysis (with 2Ghz TimingZoom™)
400 MT/s	16910/1 w/ Option 500	16750/1/2	2 cards configured as one module, one machine	<ul style="list-style-type: none"> • 4 cards configured as 1 module • 3 cards for 16910/1
		16753/4/5/6	2 cards configured as one module, one machine	<ul style="list-style-type: none"> • 4 cards configured as 1 module
Up to 533 MT/s	16950	16753/4/5/6	2 cards configured as one module	<ul style="list-style-type: none"> • 4 cards configured as 1 module

Configuration files

Logic Analyzer Cards and probe	File-name for 167xx FS1123	File-name for 169xx FS1124	Comments
1675x/169xx	DR123_1	DR123_1	4 Card config files for use with Samtec or Soft Touch connector, 1 machine
1675x/169xx	DR123_2	DR123_2	2 Card Timing, configured as 1 machine
1675x/169xx	DR123_3	DR123_3	2 Card State 16 bit data bus, 1 machine
1675x/169xx	DR123_4	DR123_4	3 Card state Read or write only, 1 machine
16753-6 only	DR123_5	DR123_5	2 Card config. used for Data Eyescan or Eyefinder
16753-6 only	DR123_6	DR123_6	1 Card config. used for Address Eyescan or Eyefinder
1675x/169x	DR123_7*	DR123_7*	4 Card State config. used for use with FS2340 Validation DIMM pcb

* This config file must be used to overwrite any FS2340 config files previously loaded on the analyzer for the Protocol Decoder labels to match.

The above chart shows the configuration file choices for the 167xx and 169xx analyzers.

Signal Naming Conventions

This operation manual uses the same signal notation as the DDR2 Bus specification. Reference the General Information section.

Setting up the FS1123 software on the 167xx Analyzer

Revision A.02.80.00 operating system or greater is required.

The Embedded DDR2 software consists of one diskette:

- 16700/702 Installation disk for the FS1123

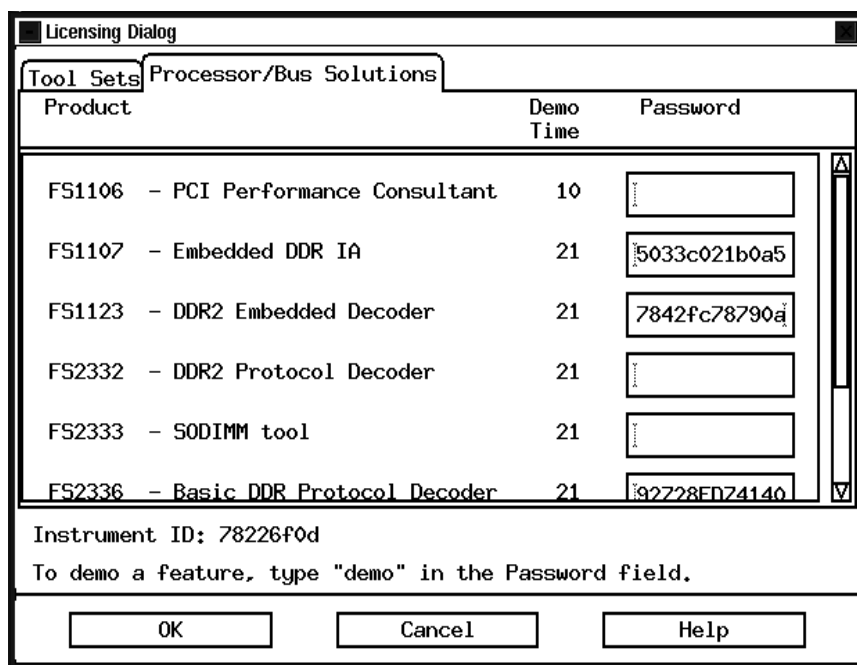
To install the FS1123 software, insert the diskette labeled **16700/702 Installation disk for the FS1123** into the diskette drive of the 16700. From the SYSTEM ADMINISTRATION TOOLS, select *INSTALL* under *SOFTWARE*. From the *SOFTWARE INSTALL* screen, select *FLEXIBLE DISK* and *APPLY*. Once the title appears, select it and then select *INSTALL*.

This procedure does not need to be repeated. It only needs to be done the first time the DDR2 analysis probe is used.

16700 Licensing

The FS1123 product is a licensed product which is locked to a single Agilent 1670x frame. Complete instructions for licensing this software are detailed on the Entitlement Certificate that is enclosed with this product. The licensing area for the 1670x mainframe is found under System Administration. Once you are at the licensing area choose the *Processor/Bus* Solutions tab, in here you will find the DDR2 inverse assembler listed. Type your password in the space provided to enable the use of the inverse assembler. A demo period is provided by typing the word *demo* into the password space next to the product name.

The following picture shows the licensing area after pressing the licensing button on the previous screen. This is where you would enter the password you will receive after following the instructions on the SW License Entitlement Certificate.



Setting up the 16700 Inverse Assembler

Once the software has been installed correctly, the configurations are located under logic/configs/futureplus/FS1123. Use the chart to determine which configuration should be loaded. Choose the file that corresponds to the setup you have. If you do not have the cards in the same slots that the configurations were originally developed in, the analyzer will tell you which slot it is trying to load the configuration into. You must click OK for it to continue to load.

When the configuration file is loaded the inverse assembler (IA) will automatically load. If the inverse assembler fails to load you can load it manually from the listing window. Press the INVASM button on the top of the screen, then choose IFS1123E from the list and select the analyzer. After selecting analyzer, press LOAD and the inverse assembler should load.

Once the configuration file is loaded you may make changes to the configuration if your pinout is different from the specified format. Labels that are used by the Protocol Decoder must be preserved; these labels must not be removed or renamed. You may reorder, add or remove some of the bits assigned to these labels; the exception to this is the Command label.

Note: Usage with the FS2340 VDIMM requires the FS1123/4 configuration file to overwrite the FS2340 configuration files in order for the DDR2 Protocol Decoder labels to match.

The following labels are used by the protocol decoder:

ADDRESS
ADDR
DATA_{Low}
DATA_{Hi}
READ_{dataLow}
READ_{dataHi}
Bank Address
Command
CommandClk
CB
CBRead
#S0
#S1

The above labels must appear exactly as shown in the format menu. In some applications you may only use 1 chip select line (#S0), in those cases assign #S1 to the same pod and channel you assigned #S0 to satisfy the protocol decoder.

Setting up the FS1124 software on the 16900 Analyzer

A CD containing the 16900 software is included in the FS1124 package. The CD contains a setup file that will automatically install the configuration files and protocol decoder onto a PC containing the 16900 operating system or onto a 16900 analyzer itself.

To install the software simply double click the .exe file on the CD containing the 16900 software. After accepting the license agreement the software should install within a couple of minutes.

16900 Licensing

Once the software has been successfully installed you must license the software. Please refer to the SW Entitlement certificate for instructions on licensing the software. The software can only be installed on one machine. If you need to install the software on more than one machine you must contact the FuturePlus sales department to purchase additional licenses.

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute it. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

Pod Attachment for the 169xx

Once you have loaded a configuration file on the 169xx machine you can find out how to attach the logic analyzer cables to the probe by going to the Overview tab and selecting Properties on the General Purpose Probe tool icon that appears before the logic analyzer icon. Once you click on the Properties box a new window will appear showing which adapter cables are required for the connectors on the probe. Highlight one of the connectors shown and click on the "Edit Probe" button. Another screen will pop up showing how to connect the analyzer pods to the specific adapter cable.

The following illustration is a general representation of how this process will look.

[Offline] Agilent Logic Analyzer - [...\windows configs\DR240...]

General Purpose Probe Set

Select the type of probe to add
 E5398A 17-ch Soft touch connectorless single-ended probe

Probes used to connect to your Device Under Test

Reference Designator	Probe Type	Logic Analyzer Pod(s)
311	E5378A 34-ch Samtec single-ended probe	Slot A Pod 1, Slot B Pod 4
312	E5378A 34-ch Samtec single-ended probe	Slot A Pod 3, Slot A Pod 4
313	E5378A 34-ch Samtec single-ended probe	Slot B Pod 1, Slot B Pod 2
314	E5378A 34-ch Samtec single-ended probe	Slot B Pod 3, Slot A Pod 2

General Purpose Probe Edit

E5378A 34-ch Samtec single-ended probe

Reference Designator: J11

Signal	Pin	Pin	Signal
ADDRESS[5]	Pin 7	Pin 8	DATA31-Q[3]
ADDRESS[0]	Pin 11	Pin 12	DATA31-Q[2]
ADDRESS[1]	Pin 15	Pin 16	DATA31-Q[0]
ADDRESS[6]	Pin 19	Pin 20	DATA31-Q[1]
ADDRESS[4]	Pin 23	Pin 24	#DQS8-2,0[0]
ADDRESS[7]	Pin 27	Pin 28	DQS8-Q[0]
ADDRESS[2]	Pin 31	Pin 32	DATA31-Q[5]
ADDRESS[3]	Pin 35	Pin 36	DATA31-Q[7]
ADDRESS[8]	Pin 39	Pin 40	DATA31-Q[4]
ADDRESS[12]	Pin 43	Pin 44	DATA31-Q[6]
ADDRESS[15]	Pin 47	Pin 48	DATA31-Q[8]
ADDRESS[14]	Pin 51	Pin 52	DATA31-Q[11]
ADDRESS[13]	Pin 55	Pin 56	DATA31-Q[10]
ADDRESS[9]	Pin 59	Pin 60	DATA31-Q[9]
ADDRESS[10]	Pin 63	Pin 64	DATA31-Q[15]
ADDRESS[11]	Pin 67	Pin 68	DATA31-Q[13]
CK0	Pin 79 Clk	Pin 80 Clk	DQS8-Q[1]

Logic Analyzer

Probe

Odd: Slot A Pod 1

Even: Slot B Pod 4

OK Cancel Help

Windows Taskbar: start, 3 Micros..., Peachtree..., 2 Micros..., E:\Softwa..., [Offline] A..., 1:10 PM

Threshold Considerations for Tristate

Each DDR2 bus implementation will have different timing due to trace length variation on the motherboard, variations in bus loading, and sensitivity to dynamic factors such as crosstalk or simultaneous switching noise. Many of these timing characteristics are fixed. These differences are difficult or impossible to predict in advance for a variety of implementations and configurations of devices.

You can vary the logic analyzer threshold to avoid false clocking. Each time you vary the threshold, take a trace with timing zoom on. This will help you to determine the optimal threshold setting for data capture and correct clocking. Please see the section on calibration for more information about using timing zoom.

Cross Bus Analysis

Real time acquisition of DDR2 traffic along with concurrent transactions on other system busses such as PCI-X, USB, SCSI and many others is supported. Use of an Agilent logic analyzer enables events on one bus to trigger measurements on other types of busses providing time-correlated views of all bus events. This capability is commonly referred to as cross-bus analysis. In addition to cross-triggering, global markers enable quick correlation between different buses.

FuturePlus Systems offers support for a wide variety of industry standard buses. To learn more please visit our web site at www.futureplus.com

EyeScan Operation

EyeScan is a feature of the 16753/4/5/6 cards that is used to view information about the signal integrity of each channel. Two configuration files are provided which allows the user to use Eyescan for the command bus and the data bus. You must reconfigure the pods for each configuration. Eyescan gives a visual representation of the data valid window on each channel; it also measures the voltage of the eye.

Command and Address

The EyeScan feature of the 16753/4/5 can be used to generate eye patterns of signals brought to the analyzer that are related to the CK0 clock signal on the DDR2 DIMM bus. Load the configuration file for Command/Address, attach pods as stated in the table below.

Chip Select Qualification

In order to capture the Address or commands at the proper time a chip select must be used as for clock qualification. The configuration file uses #S0 to qualify the clock, if you need to use a different chip select then you will physically need to move a chip select to a clock pin.

Embedded Connector	Analyzer Pod
J1 Odd	D1 (Master Pod 1)
J1 Even	D2 (Master Pod 2)

Data

Data (DQxx) and Data Strobes (DQSx) can be evaluated with EyeScan by using the DQS0 signal as a clock input to the logic analyzer card.

Load the configuration file for Data eyescan and attach cables as listed below. The configuration file automatically sets up DQS0 as the clock to clock the analyzer.

Embedded Connector	Analyzer Pod
J2 odd	Master Pod 1
J2 even	Master Pod 2
J3 odd	Master Pod 3
J3 even	Master Pod 4
J4 odd	Expander Pod 1
J4 even	Expander Pod 2

Note: The table above refers to customers who have placed connectors onto their target; the “J” numbers correspond to the “J” numbers in the DDR application note.

The target must generate either exclusively Read or Write activity. This is because the edges of the Data Strobes change their position relative to the edges of the Data signals on a Read burst or a Write burst. There are some specialized software programs that can generate this sort of activity.

Symbols

There are symbols that are associated with the **Command** label found in the format specification. These symbols can be used in the trigger sequence and also for store qualification.

SYMBOL	VALUE
NOP	111
Activate	011
Read	101
Write	100
Precharge	010
Refresh	001
Load Mode Register	000

To use these symbols simply choose the label Command and change HEX to SYMBOLS and choose the symbol you want.

When using these symbols for triggering or store qualification you must qualify the command with a chip select(s) and the rising edge of the DDR2 clock because commands are only valid on a rising edge of the clock and when chip select(s) is valid.

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

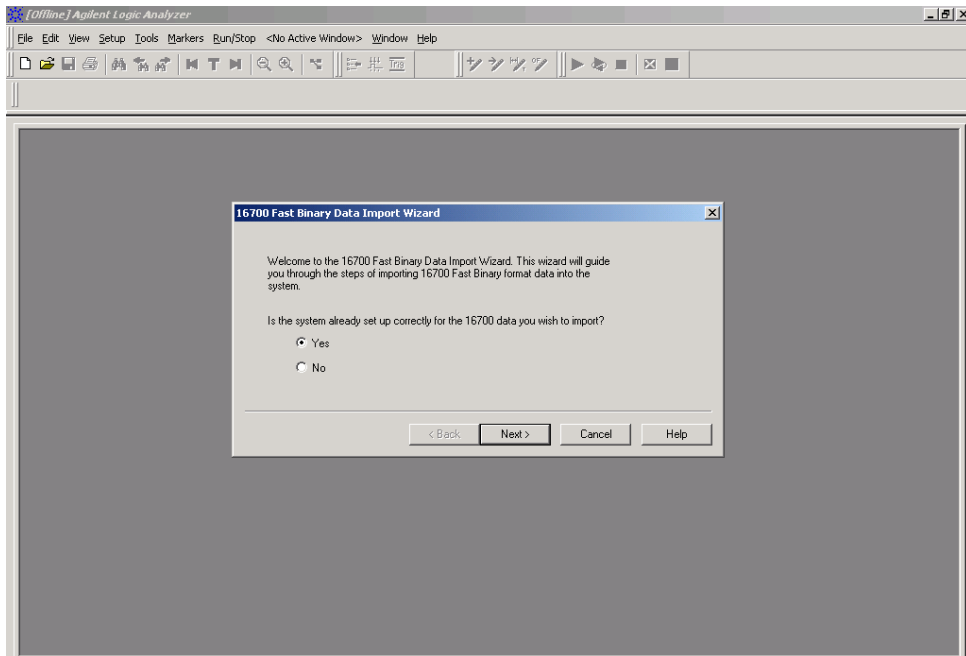
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may buy additional licenses, please contact FuturePlus sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up 16900 analyzer". Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

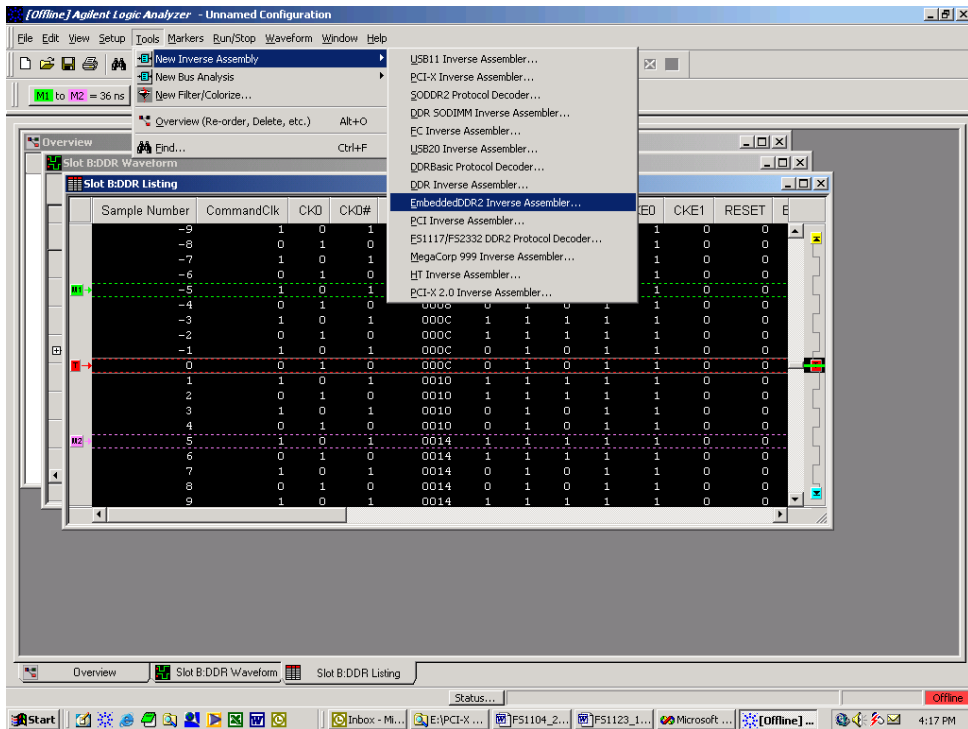
For data from a 16900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select "yes" when it asks if the system is ready to import 16700 data.



After clicking “Next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular trace. See figure below.



After the decoder has loaded, select Preferences from the overview screen and set the preferences to their correct value in order to decode the trace properly.

Timing Analysis

Pod Attachment for Timing Analysis

Please refer to the table below for pod attachment for timing analysis. The configuration assumes 64 bit analysis, 2 cards connected together as 1 machine with the Master in B, expander in A. For 16900 users consult the General Purpose Probe section of the Overview tab.

Embedded Connector	Analyzer Pod
J1 odd	B1 (Master)
J1 even	B2 (Master)
J2 odd	B3 (Master)
J2 even	B4 (Master)
J3 odd	A1 (Expander)
J3 even	A2 (Expander)
J4 odd	A3 (Expander)
J4 even	A4 (Expander)

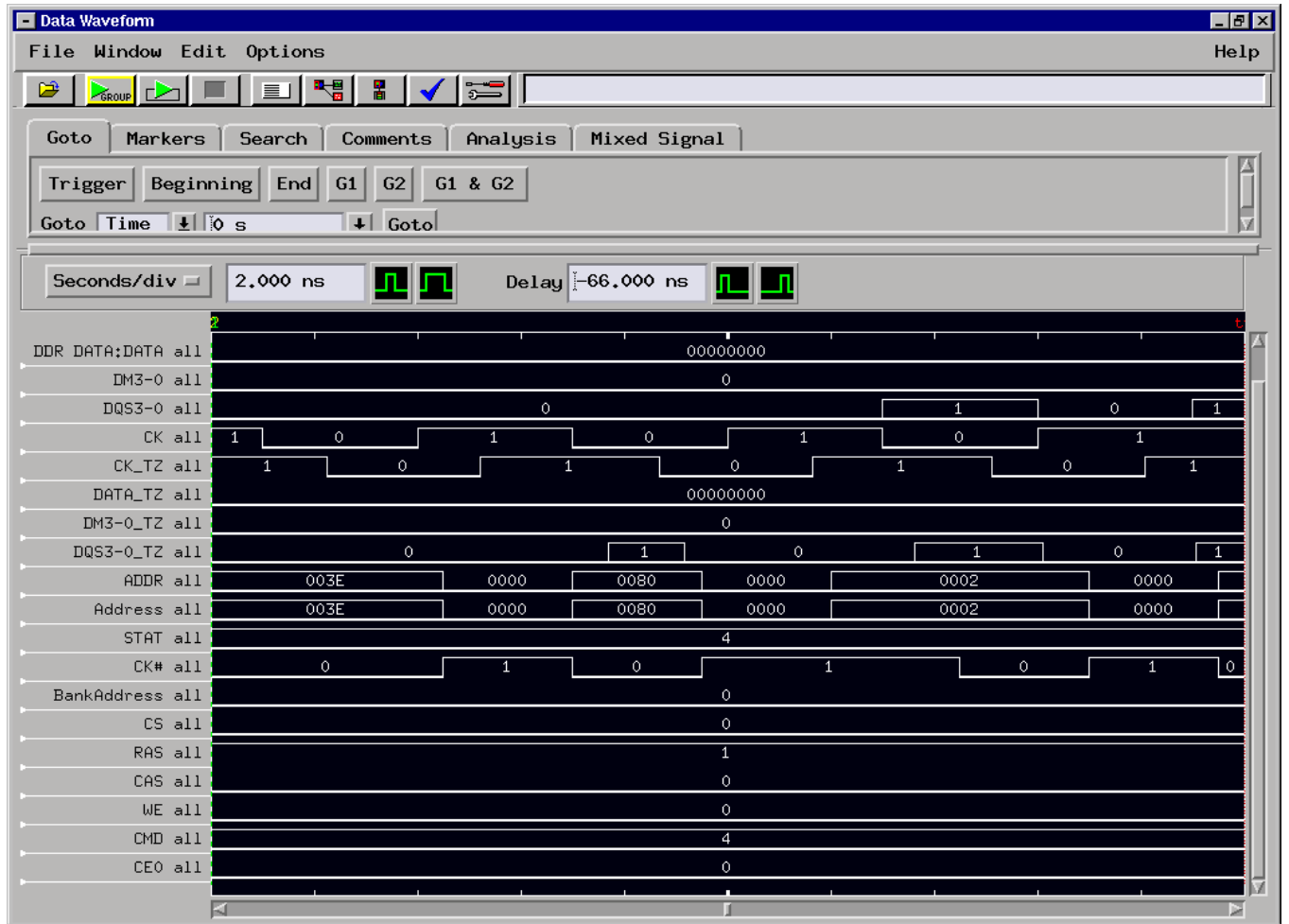
Acquiring Data

Timing analysis is performed by loading the configuration file specified for timing analysis and set up the trigger specification.

Touch RUN and the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE, or when you touch STOP.

The logic analyzer will flash “Waiting for Trigger” or “occurrences remaining in level x” where x is the number of the unsatisfied trigger level if the trigger condition is not satisfied.

Sample Waveform Display



State Analysis

This chapter explains how to use the FS1123/24 to perform state analysis on an embedded DDR2 bus. The software will load the appropriate configuration files assigning all channels, predefine the clocks, and load symbols. The inverse assembler, which is automatically loaded as part of the configuration file, will decode the data and display it as transactions

State capture of the Address and Command lines of the DDR2 bus requires one clock edge for reliable results. CK0 can be used as the clock for the analyzer. It must be properly terminated to CK0# per normal DDR2 requirements. The proper termination is a 120-ohm resistor between CK0 and CK0#. This is required for proper operation of the differential clock. No extra termination is required for probing. Probe as close the termination resistor as possible.

State mode analysis of DDR2 is performed with one machine and is clocked on both the rising and falling edges of the CK0/ CK0# clock. Because the analyzer is clocked on both edges there will be states captured that are invalid, there is a preference in the preference menu of the decoder that will strip out invalid states.

A calibration procedure is required before you can accurately capture and analyze state data that has mixed Reads and Writes, the calibration procedure is outlined later in this section.

Before proceeding you must attach 4 logic analyzer cards together as 1 machine and load the configuration file per the table on page 1. If you are analyzing a bus with less than 32 bits you can use less than 4 cards and adjust the pod attachment accordingly. Do not load the configuration files. for Eyescan.

Pod Attachment for State Analysis

For **168x/169x/169xx** consult the General Purpose Probes section in the Overview tab after loading a configuration file.

The table below shows how the pods need to be attached for state analysis of an embedded 64 bit DDR2 bus on a **167xx** frame. The connection assumes master card in slot C, expanders in slots B, D, E; 4 cards connected together as one analyzer and the pinout is the same as the

Embedded DDR2 application note. If the pinout is not exactly as the application note outlines then you will be required to reorder bits to match your pinout.

Embedded Connector	Analyzer Pod (4 Card dual sample)	Analyzer Pod (3 cards)
J1 odd	C1 (Master)	B1 (Master)
J1 even	C2 (Master)	B2 (Master)
J2 odd	C3 (Master)	B3 (Master)
J2 even	E1 (Expander)	B4 (Master)
J3 odd	E3 (Expander)	C1 (Expander)
J3 even	D1 (Expander)	C2 (Expander)
J4 odd	D3 (Expander)	C3 (Expander)
J4 even	B1 (Expander)	C4 (Expander)

The remaining pods will be left disconnected and cannot be used. The 4 card dual sample is the preferred configuration. A 3 card configuration is also provided for users who do not have 4 cards available. The 3 card configuration only allows the capture of Reads or Writes, you cannot capture Reads and Writes simultaneously.

If you are using the 3 card configuration you still must calibrate for Reads or Writes, if you are calibrating for Reads move only the sample positions for the Read Data labels and vice versa. The 3 card config assumes master is in slot B and expanders are in C and A. Although the card in slot A is not physically attached, it must be connected to the other two cards in order for the machine to run in turbo mode with time tags on.

Missing or slow clock

If the analyzer identifies an error of a missing or slow clock be sure to check the threshold settings for the J clock. If the clock was brought in differentially and you are using soft touch or Samtec connectors along with 16753-16756 cards be sure the threshold is set for “differential”. If the clock was brought in as a single ended signal then the threshold for the clock should be set to 900mv. The threshold for the clock inputs for 16750-16752 cannot be changed independent of the pod thresholds so if you are using those type of cards then the clock signal must be treated as a single ended signal.

Also be sure the pods are attached to the connectors properly and the correct termination adapter is being used.

Calibration

The calibration procedure uses TimingZoom to identify the time difference between the CommandClk (rising and falling edges) and the center of the Read and/or Write eyes. If dual sampling is used there is one set of labels for Reads and another for Writes and the sample position can be set independently for each. The sample position for each label is set to the middle of the data valid region for the burst type the label supports.

State analysis calibration procedure

Before calibration you must load the 4 card configuration file for state analysis. Please refer to page 11 in the “Getting Started” section for the table showing which configuration file to load.

The protocol decoder (IA) requires 4 parameters to be entered by the user in order to decode valid states. These inputs can be seen by selecting Invasm and then choosing Preferences in the state listing window on the 167xx frames, on the 169xx select Preferences from the protocol decoder icon in the overview. The information required is generally available from the spec. sheet of the memory device being used or by querying the BIOS of the target system.

Number of Chip Selects – This is based on which Chip Select is being probed and incorporated into the IA, usually S0 and/or S1. If 2 is selected either chip select S0 or S1 would be used to determine if command is valid.

CAS Latency – Also defined as “CL”, or the delay from a valid Read command to when the Read data is strobed on the bus. Usually either 3, 4, or 2.

Burst Length – Usually fixed at 4, or 8.

Additive Latency- Defaulted to 1.

Data Label Width – Defaulted to 2. If you require up to 64 data bits leave it set to 2, if you require up to 32 bits or less type in a 1 for this preference.

The input screen for this information is shown below in Figure 4. Shown are the default values on a 167xx frame.

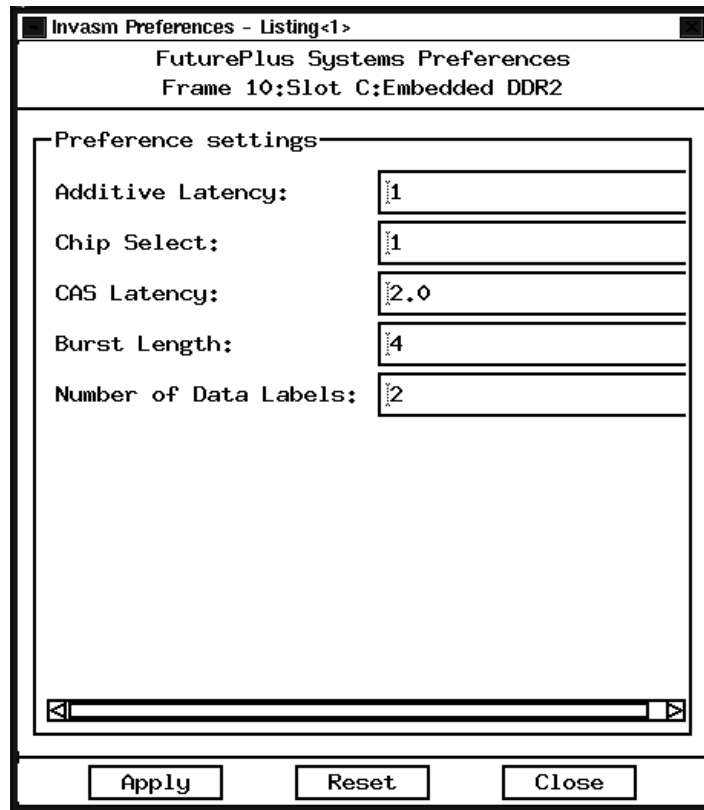


Figure 4

Start a memory test program that creates a good mixture of Reads and Writes, ideally with bursts of both types close enough together to fit several cycles of each type of burst in a single TimingZoom trace.

Trigger the analyzer on a burst. This can be done by using the logic analyzer trigger macro "Find pattern n times" as shown in Figure 5 below:

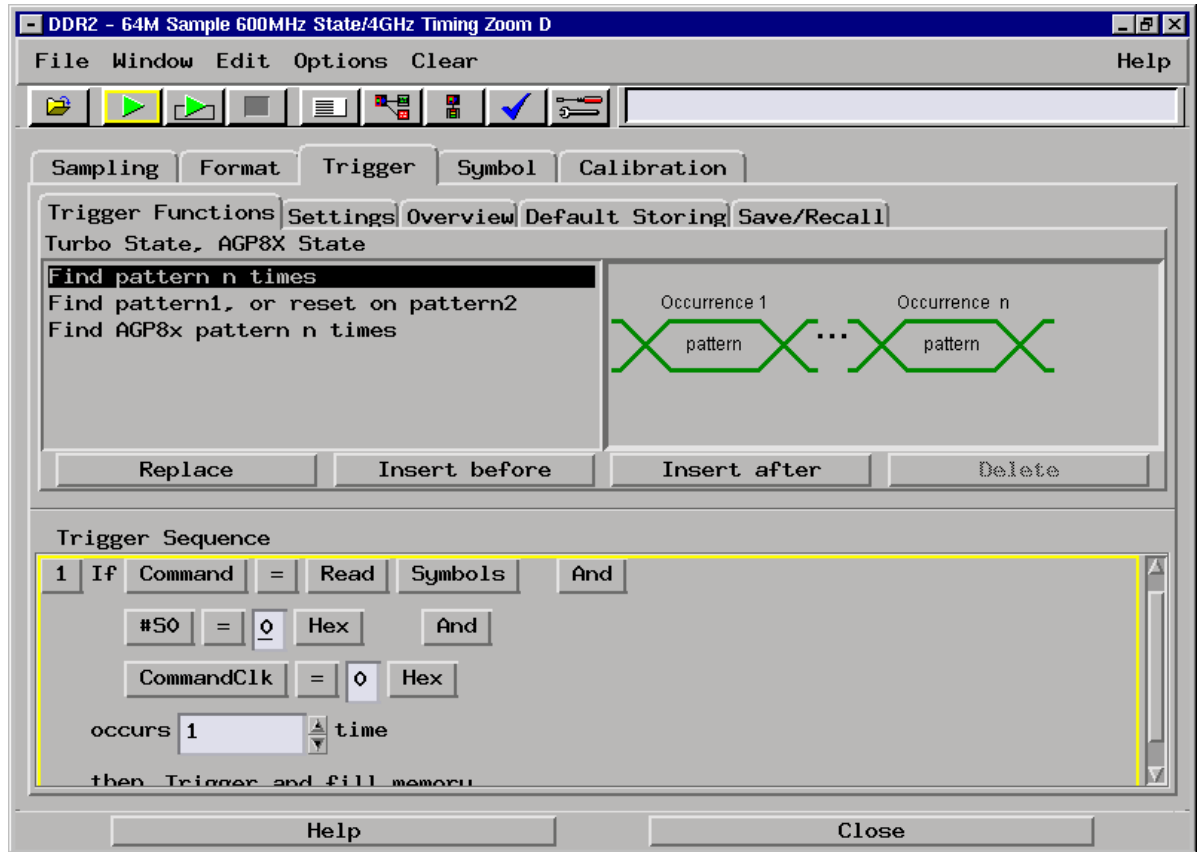


Figure 5 - Trigger on a read

Note that in addition to looking for the DDR2 commands the #S0 signal is used to determine if the command is actually addressing a memory chip and the CommandClk signal is used to make sure the command sampled on the rising edge of the CommandClk is used (since that is when the DDR2 command bus is valid). This example uses #S0 to identify valid commands. Any chip select that addresses an actual rank of memory may be used. If more than one chip select signal is needed (such as when there are several DIMMs on the bus) each of those chip select signals may be 'OR'ed together in the trigger event.

Bring up a waveform display and add the TimingZoom labels for the command clock, chip selects, and DQS0 (CommandClk_TZ, #S0_TZ, DQS_TZ[0]) and the data bus labels for Reads (READdataHi_TZ, READdataLow_TZ, and CB7-0) in the waveform view. Scroll the waveforms to find the start of a Read burst. You will see this by finding where the DQS0 strobe becomes active. Note: in some cases READdataxx_TZ will not contain timing zoom information, in those cases use the dataxx_TZ labels instead.

Figure 6 below shows an example waveform display being used to locate the start of a Read burst.

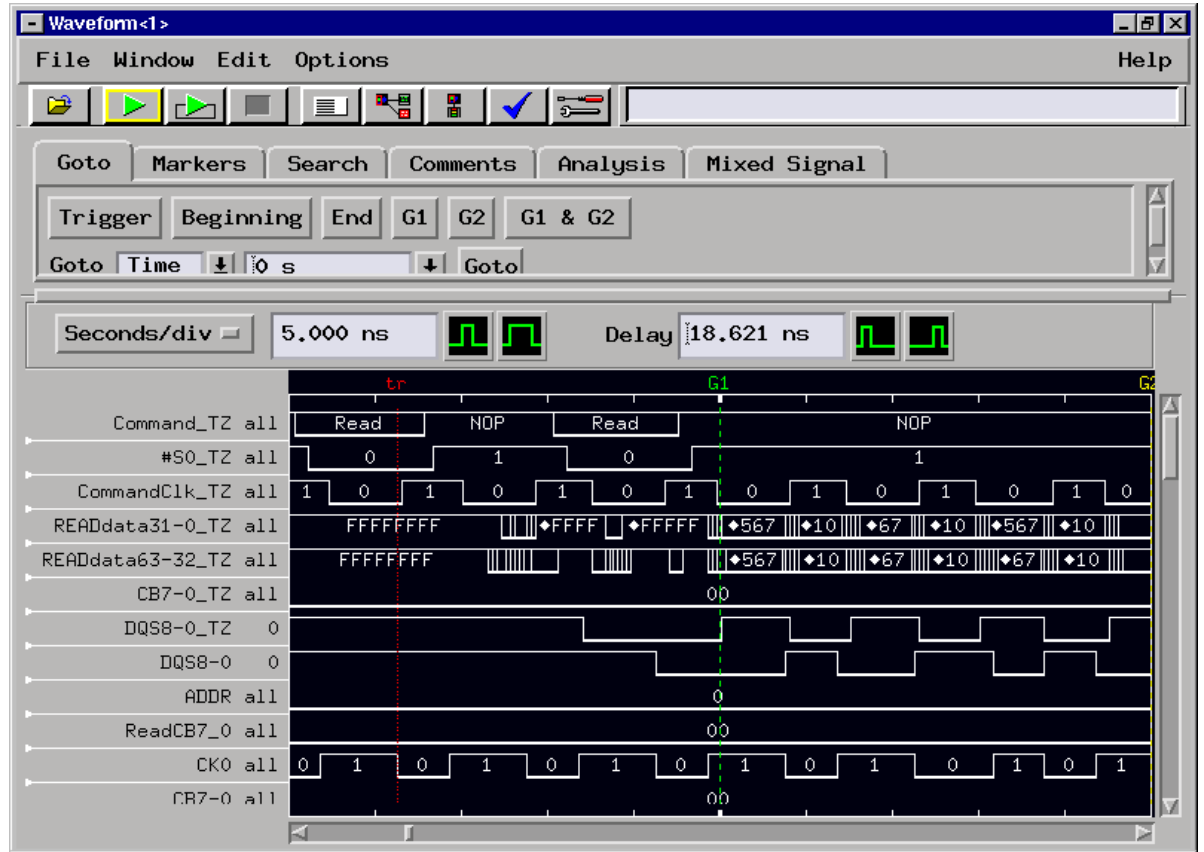


Figure 6 - Locating a Read Burst

Note: READDataLow_TZ refers to READdata31-0_TZ and READDataHi_TZ refers to READdata63-32_TZ in the picture. Also you may not have timing zoom information depending upon the analyzer used; in those cases it is perfectly fine to use the dataxx_TZ labels.

Now the time delay from the closest edge of CommandClk prior to the center of the Read data eyes can be measured. Place the G2 marker on that edge of the CommandClk. Place the G1 marker in the center of the data valid region for the Read data label. You may find it easier to identify this point by locating the point on one of the DQS signals that is equal distances from the edges. Note the delay between the markers as shown in Figure 7.

Repeat this procedure using the next edge of CommandClk and the corresponding data burst cycle (it will be right next to the burst cycle you just looked at).

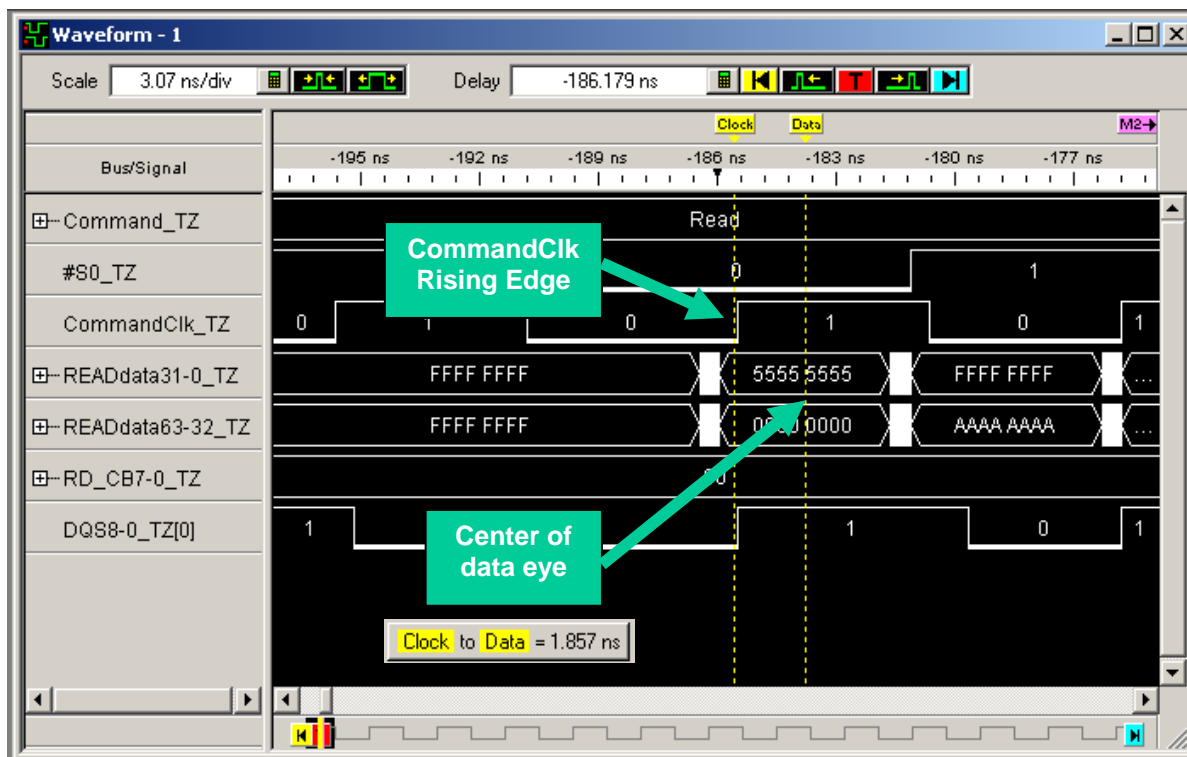


Figure 7 - Command Clk rise to center of Read data eye

Repeat this procedure for several cycles of the burst. You may do this for other Read bursts as well if you wish to cover different types of data burst patterns and account for possible edge jitter sources. Compute the average of the times for all the burst cycles (combining those for the rise of CommandClk and the fall). This will be your sample position delay value, e.g. 1.85ns as shown in Fig. 7.

Now it is time to use this delay information to set the logic analyzer sample position. From the “format” tab of the “DDR2 Data” analyzer window bring up the Eye Finder display, and then select the “Eye Finder Results” tab to bring up the display shown in Figure 8. This display will allow you to set the sample positions for the Read and Write data labels. (The Write data labels are shown)

Set the sample position to be equal to the average time you computed in step 6. The easiest way to do this is to point to the blue vertical sample position bar with the mouse and press and hold the left mouse button while dragging the blue bars as far to the left side of the display as possible. This will cause all the blue bars for that label to be set to the same value. Then you can drag the blue sample position bar back to the right to place it in the position you measured in step 6. The sample position is indicated on the scale at the top of the display as well as on the side under the “Sampling Position” column. Figure 9 shows the DATA31_0 (DATA_{Low}) label sample position set to +1.86ns as an example. This means that if you measured a 1.86ns average delay to the center of the data eye for the READdata_{Low}

bus after a valid Command Clock edge, you would set the analyzer sample position for READdataLow to +1.86ns (as shown in Figure 9).

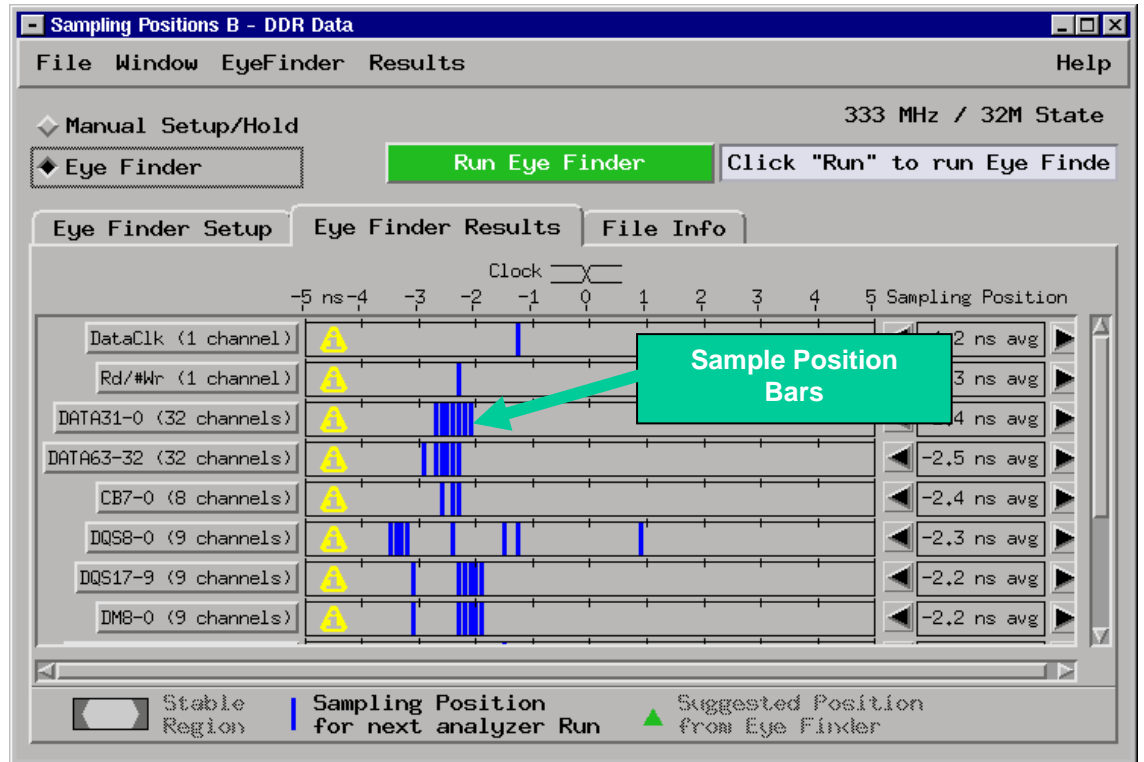


Figure 8 – Setting the Sample positions

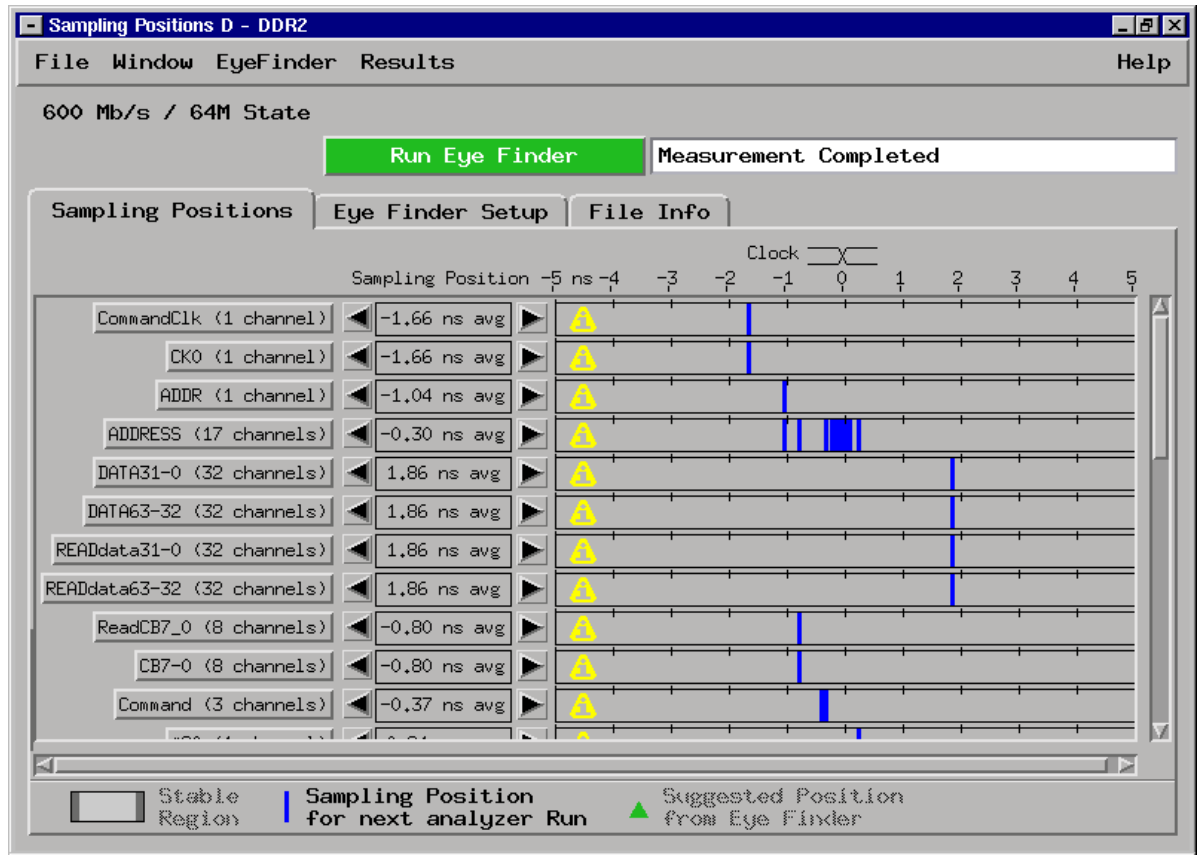


Figure 9 – DATA31-0 set to +1.86ns

Repeat this procedure as well for the ECC bits and the data strobes.

For the DDR2 command/address bus you can repeat this procedure also, except that time is measured only from the rising edge of CommandClk since those signals are only valid at that time.

This completes the procedure for the sampling position for Reads. Use the same procedure using Write bursts and set the sampling position for the Write data labels (DATA0_31, DATA32_64, CB). (Write data eyes are centered on the edge of the strobes whereas Reads straddle the DQS strobes.)

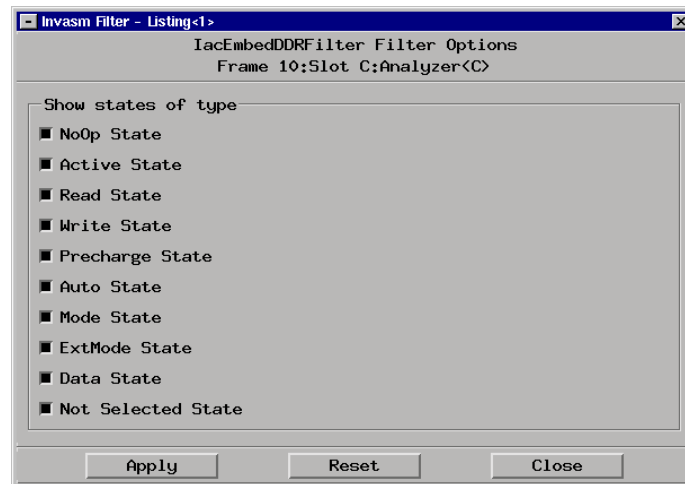
Once you have set the sampling positions for both sets of labels (Read and Writes) you should be ready to take state traces and be confident you will capture bus traffic correctly. For more information on EyeFinder and state mode sampling positions you can consult the on-line help system of the 16700 or 16900.

Acquiring Data in State Mode

Once calibration is complete set the trigger specification to the desired setting, set preferences (see the beginning of the calibration section for info on preferences) and Touch RUN and the logic analyzer will begin to acquire data once the trigger condition has been met. The analyzer will continue to acquire data and will display the data when the analyzer memory is full or when you touch STOP.

The logic analyzer will flash “Waiting for Trigger” or “occurrences remaining in level x” where x is the number of the unsatisfied trigger level if the trigger condition is not satisfied.

There may be many states that are not valid states because the analyzer is clocked on both edges of the DDR2 clock, these can be filtered after the data has been captured. To locate the filter on the 167xx frames go to the listing window and press the INVASM button, choose filter and you should see a window like the one below.



By default nothing is filtered, if you want states that are not valid simply press the box next to “Not Selected State” and press apply and the non valid states will be filtered.

Filtering on the 169xx is configured by the user there are no predetermined filters in the 169xx decoder. To set up a filter in the 169xx environment select tools from the menu bar, then select filter/colorize. You can choose to filter before or after the decoder. If you filter before the decoder, use

caution to not filter any labels needed by the decoder. If you filter after the decoder you can use the label "filter tags" created by the decoder, change hex to symbols and use symbols to remove any command that the user does not want to see.

The user may also create any custom filter they need.

General Information

Signal Connections

DDR2 revision 1.0

J1 Address/Command bus

LA Odd Pod	Signal
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D0	AD0
Gnd	Gnd
Odd D1	AD1
Gnd	Gnd
Odd D2	AD2
Gnd	Gnd
Odd D3	AD3
Gnd	Gnd
Odd D4	AD4
Gnd	Gnd
Odd D5	AD5
Gnd	Gnd
Odd D6	AD6
Gnd	Gnd
Odd D7	AD7
Gnd	Gnd
Odd D8	AD8
Gnd	Gnd
Odd D9	AD9
Gnd	Gnd
Odd D10	AD10
Gnd	Gnd
Odd D11	AD11
Gnd	Gnd
Odd D12	AD12
Gnd	Gnd
Odd D13	AD13

Signal	LA Even Pod
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D0	CKE
Gnd	Gnd
Even D1	#WE
Gnd	Gnd
Even D2	#CAS
Gnd	Gnd
Even D3	#RAS
Gnd	Gnd
Even D4	BA0
Gnd	Gnd
Even D5	BA1
Gnd	Gnd
Even D6	BA2
Gnd	Gnd
Even D7	#S1
Gnd	Gnd
Even D8	#S2
Gnd	Gnd
Even D9	#S3
Gnd	Gnd
Even D10	ODT0
Gnd	Gnd
Even D11	ODT1
Gnd	Gnd
Even D12	NC
Gnd	Gnd
Even D13	NC

Gnd	Gnd
Odd D14	AD14
Gnd	Gnd
Odd D15	AD15
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D16P/CLKP	CK0
Gnd	Gnd
Odd D16N/CLKN	CK0#
Gnd	Gnd
Odd Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

Gnd	Gnd
Even D14	NC
Gnd	Gnd
Even D15	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D16P/CLKP	#S0
Gnd	Gnd
Even D16N/CLKN	Gnd
Gnd	Gnd
Even Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

J2 Lower data bits and strobes

LA Odd Pod	Signal
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D0	DQ0
Gnd	Gnd
Odd D1	DQ1
Gnd	Gnd
Odd D2	DQ2
Gnd	Gnd
Odd D3	DQ3
Gnd	Gnd
Odd D4	DQS0
Gnd	Gnd
Odd D5	DQ4
Gnd	Gnd

Signal	LA Even Pod
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D0	DQ13
Gnd	Gnd
Even D1	DQ14
Gnd	Gnd
Even D2	DQ15
Gnd	Gnd
Even D3	DQS3
Gnd	Gnd
Even D4	DQ16
Gnd	Gnd
Even D5	DQ17
Gnd	Gnd

Odd D6	DQ5
Gnd	Gnd
Odd D7	DQ6
Gnd	Gnd
Odd D8	DQ7
Gnd	Gnd
Odd D9	DQS1
Gnd	Gnd
Odd D10	DQ8
Gnd	Gnd
Odd D11	DQ9
Gnd	Gnd
Odd D12	DQ10
Gnd	Gnd
Odd D13	DQ11
Gnd	Gnd
Odd D14	DQS2
Gnd	Gnd
Odd D15	DQ12
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D16P/CLKP	DQS0
Gnd	Gnd
Odd D16N/CLKN	#DQS0
Gnd	Gnd
Odd Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

Even D6	DQ18
Gnd	Gnd
Even D7	DQ19
Gnd	Gnd
Even D8	DQS4
Gnd	Gnd
Even D9	DQ20
Gnd	Gnd
Even D10	DQ21
Gnd	Gnd
Even D11	DQ22
Gnd	Gnd
Even D12	DQ23
Gnd	Gnd
Even D13	DQS5
Gnd	Gnd
Even D14	DQ24
Gnd	Gnd
Even D15	DQ25
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D16P/CLKP	NC
Gnd	Gnd
Even D16N/CLKN	Gnd
Gnd	Gnd
Even Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

J3 Middle data and strobes

LA Odd Pod	Signal
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D0	DQ26
Gnd	Gnd
Odd D1	DQ27
Gnd	Gnd
Odd D2	DQS6
Gnd	Gnd
Odd D3	DQ28
Gnd	Gnd
Odd D4	DQ29
Gnd	Gnd
Odd D5	DQ30
Gnd	Gnd
Odd D6	DQ31
Gnd	Gnd
Odd D7	DQS7
Gnd	Gnd
Odd D8	DQ32
Gnd	Gnd
Odd D9	DQ33
Gnd	Gnd
Odd D10	DQ34
Gnd	Gnd
Odd D11	DQ35
Gnd	Gnd
Odd D12	DQS8
Gnd	Gnd
Odd D13	DQ36
Gnd	Gnd
Odd D14	DQ37
Gnd	Gnd
Odd D15	DQ38
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd

Signal	LA Even Pod
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D0	DQ39
Gnd	Gnd
Even D1	DQS9
Gnd	Gnd
Even D2	DQ40
Gnd	Gnd
Even D3	DQ41
Gnd	Gnd
Even D4	DQ42
Gnd	Gnd
Even D5	DQ43
Gnd	Gnd
Even D6	DQS10
Gnd	Gnd
Even D7	DQ44
Gnd	Gnd
Even D8	DQ45
Gnd	Gnd
Even D9	DQ46
Gnd	Gnd
Even D10	DQ47
Gnd	Gnd
Even D11	DQS11
Gnd	Gnd
Even D12	DQ48
Gnd	Gnd
Even D13	DQ49
Gnd	Gnd
Even D14	DQ50
Gnd	Gnd
Even D15	DQ51
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd

Odd D16P/CLKP	TEST
Gnd	Gnd
Odd D16N/CLKN	GND
Gnd	Gnd
Odd Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

Even D16P/CLKP	CK2
Gnd	Gnd
Even D16N/CLKN	#CK2
Gnd	Gnd
Even Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

J4 Upper data and strobes

LA Odd Pod	Signal
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D0	DQS12
Gnd	Gnd
Odd D1	DQ52
Gnd	Gnd
Odd D2	DQ53
Gnd	Gnd
Odd D3	DQ54
Gnd	Gnd
Odd D4	DQ55
Gnd	Gnd
Odd D5	DQS13
Gnd	Gnd
Odd D6	DQ56
Gnd	Gnd
Odd D7	DQ57
Gnd	Gnd
Odd D8	DQ58
Gnd	Gnd
Odd D9	DQ59
Gnd	Gnd
Odd D10	DQS14

Signal	LA Even Pod
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D0	DQS16
Gnd	Gnd
Even D1	DQS17
Gnd	Gnd
Even D2	CB0
Gnd	Gnd
Even D3	CB1
Gnd	Gnd
Even D4	CB2
Gnd	Gnd
Even D5	CB3
Gnd	Gnd
Even D6	CB4
Gnd	Gnd
Even D7	CB5
Gnd	Gnd
Even D8	CB6
Gnd	Gnd
Even D9	CB7
Gnd	Gnd
Even D10	SA0

Gnd	Gnd
Odd D11	DQ60
Gnd	Gnd
Odd D12	DQ61
Gnd	Gnd
Odd D13	DQ62
Gnd	Gnd
Odd D14	DQ63
Gnd	Gnd
Odd D15	DQS15
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Odd D16P/CLKP	CK1
Gnd	Gnd
Odd D16N/CLKN	#CK1
Gnd	Gnd
Odd Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC

Gnd	Gnd
Even D11	SA1
Gnd	Gnd
Even D12	SA2
Gnd	Gnd
Even D13	SDA
Gnd	Gnd
Even D14	WP
Gnd	Gnd
Even D15	FETEN
Gnd	Gnd
NC	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Even D16P/CLKP	NC
Gnd	Gnd
Even D16N/CLKN	NC
Gnd	Gnd
Even Ext. Ref.	NC
Gnd	Gnd
NC	NC
Gnd	Gnd
Gnd	Gnd
+5V	NC
+5V	NC