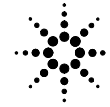


FuturePlus Systems Corporation



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# **FS1106 PCI Performance Consultant Software Users Manual**

**For use with Agilent Logic Analyzers**

**Revision – 1.2**

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# How to reach us

**For Technical Support:**

FuturePlus Systems Corporation

36 Olde English Road

Bedford NH 03110

TEL: 603-471-2734

FAX: 603-471-2738

On the web <http://www.futureplus.com>

**For Sales and Marketing Support:**

FuturePlus Systems Corporation

TEL: 719-278-3540

FAX: 719-278-9586

On the web <http://www.futureplus.com>

FuturePlus Systems has technical sales representatives in several major countries. For an up to date listing please see

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# Introduction

This product is a B4605B Tool Development Kit generated software tool that will take the input labels from the passive PCI configuration file FORMAT menu and generate columns in the listing screen. These columns will decode the PCI bus traffic in an easy to read format and provide additional performance information.

The FS1106 will come with several sample configuration files that match the passive PCI products from FuturePlus Systems. Customers with custom pinouts can use any of these files and modify them for their own custom configuration.

The configuration software on the diskette sets up the format specification menu of the logic analyzer for compatibility with the specified FuturePlus PCI analysis probe. Once installed, the FS1106 PCI Performance Consultant software will appear as an icon in the CUSTOM area of your workspace.

This manual is organized to help you quickly find the information you need.

## How to Use This Manual

- The **Getting Ready** chapter discusses the installation procedure and minimum equipment required to use the FS1106 product.
- The **State Analysis** chapter explains how to configure the logic analyzer and FS1106 software for state analysis.
- The **Timing Analysis** chapter explains how to configure the logic analyzer for timing analysis.

# Getting Ready

This chapter discusses the installation procedure, minimum equipment required to use the FS1106 product and the logic analyzer configuration files.

## Accessories Supplied

The FS1106 product consists of the following accessories:

- Two diskettes containing the configuration files and FS1106 software.
- This operating manual

## Minimum Equipment Required

The minimum equipment required for analysis of a PCI Local Bus using the FS1106 product consists of the following equipment:

- Agilent 16700 analysis frame with the 16715 analyzer card or better.
- Revision 2.0 or better of the Agilent Logic analysis frame software.
- The FS1106 Product
- A PCI target bus

## Signal Naming Conventions

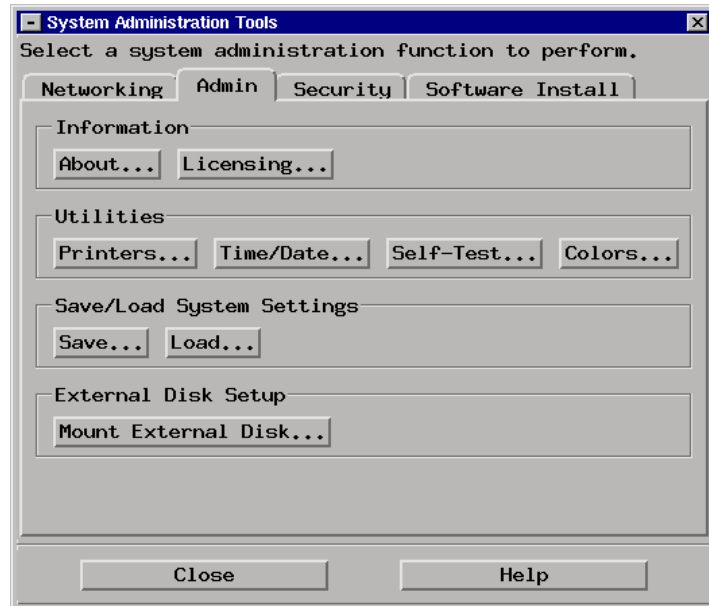
This operating manual uses the same signal notation as the PCI LOCAL BUS SPECIFICATION - REVISION 2.2 That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

## Licensing

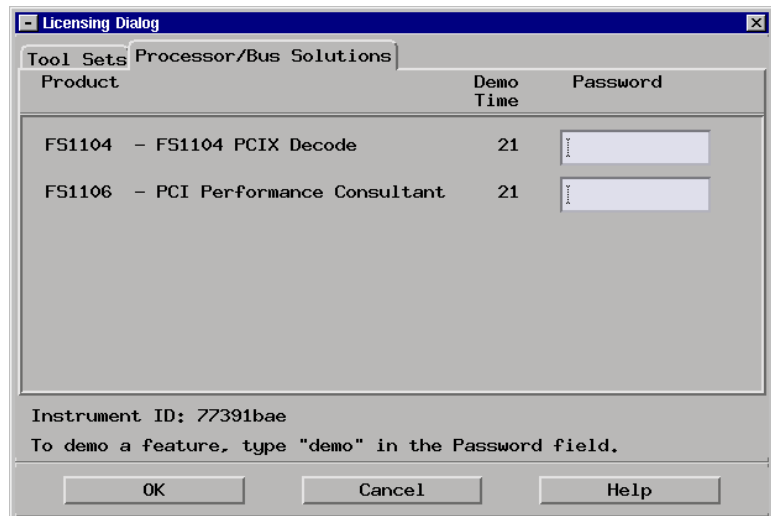
The FS1106 product is a licensed product which is locked to a single Agilent 1670x frame. A demo time is provided by typing the word *demo* into the licensing area next to the product name. The licensing area for the 1670x mainframe is found under System Administration. For use of the FS1106 product beyond the demo time please contact FuturePlus Systems at [www.futureplus.com](http://www.futureplus.com) or 719-278-3540.

## Licensing Area

The following shows the ADMIN tab under System Administration Tools.



Once the FS1106 product is installed the password may be entered in the area shown below.



## Probing your PCI Target

For FuturePlus Systems passive PCI analysis probes follow the installation instructions that came with the product. For custom configurations use one of the provided configuration files and reassign each label in the FORMAT menu to match the custom configuration. Please note that the SYMBOLS provided will not decode properly unless the bits have been reordered to reflect the original assigned order.

For custom probing information refer to the below documents on the FuturePlus Systems web site at [www.futureplus.com](http://www.futureplus.com) under Technical Support

- Designing Your Own Physical Connection To A 32/64-bit Embedded PCI Bus For Use With FS1106 PCI Analysis Tool

## Supported Logic Analyzers

The included FS1106 configuration files only support the 16715 family and above of logic analyzer cards. However, the FS1106 Performance Consultant tool will work when connected to the 1655x or 16710, 16711 and 16712 logic analyzer cards on the 1670x workspace.

## Setting up the Software on the Analyzer

The FS1106 software consists of two diskettes.

- The FS1106 Configuration Software diskette
- The FS1106 PCI Performance Consultant diskette

To install the configuration files insert the diskette labeled **FS1106 PCI Configuration Software** into the Agilent 16700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL*.

To install the FS1106 PCI transactor and performance software insert the diskette labeled **FS1106 PCI Performance Consultant** into the Agilent 16700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL*.

**This procedure does not need to be repeated. It only needs to be done the first time the FS1106 software is used.**

When this has completed load the appropriate configuration file from the /configs/FuturePlus/FS1106 directory. Refer to the below table for a list of analyzers and corresponding configuration files.

The only analyzers supported by the FS1106 configuration files are the 16715 or better.

<b>FuturePlus Product</b>	<b>File name for State/Timing Analysis</b>	<b>Description</b>
FS2000	CP1106_1	32 bit/ 33Mhz PCI w/ extender
FS2001	CP1106_2	32/64 bit 33/66 MHz
FS2005/6	CP1106_3	32/64 bit 33/66 MHz w/ extender
FS2004	CP1106_4	32 bit Cardbus
FS3010	CP1106_5	32 bit 33 MHz CardBus
FS3020	CP1106_6	32/64 bit 33Mhz CompactPCI
FS2007	CP1106_7	PCI/PCI-X 32/64 bit 33/66/133Mhz

Some of the above configuration files require two logic analyzer cards melded for 64 bit analysis. For 32 bit analysis only one logic analyzer card is required. When loading the configuration file into a one card configuration a yellow warning message will appear that notes that the two extra pods are not being loaded. This message will not effect proper operation and is merely for notification purposes.

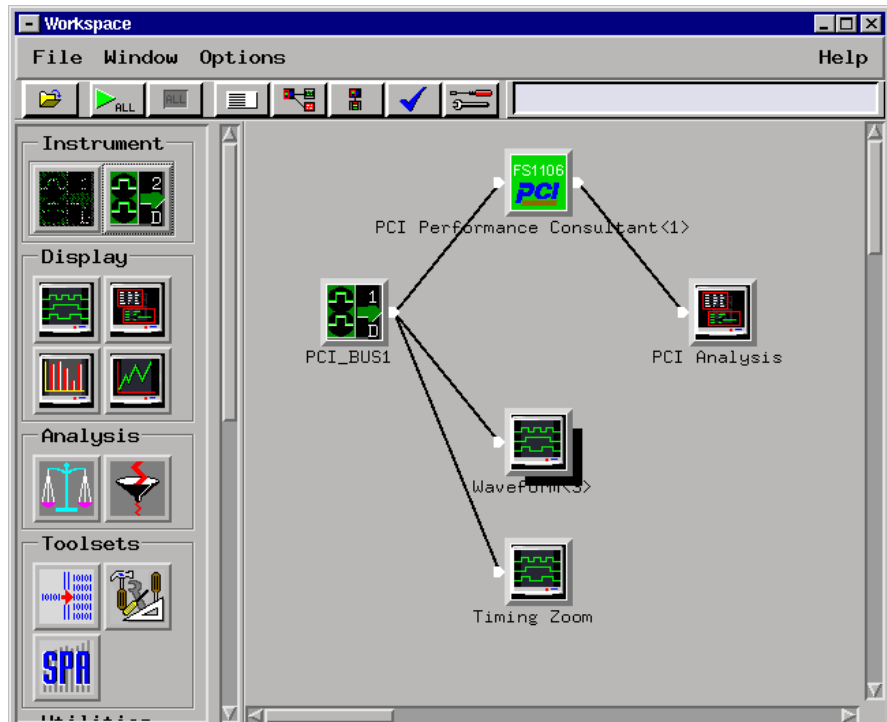
## **Loading the FS1106 Software**

Loading the configuration file will automatically load the FS1106 software onto the workspace. If this does not happen then check to make sure that the FS1106 software was properly installed. To manually place the FS1106 tool onto the workspace follow the steps below.

Load the logic analyzer configuration file.

1. Move the logic analyzer icon onto the workspace.
2. Move the FS1106 icon onto the workspace and attach to the logic analyzer.
3. Attach a lister icon to the output of the FS1106 icon
4. Open the FS1106 icon and press *execute*.

The lister will now contain the PCI transaction decode and performance output.



## Assigning additional signals

Any additional signals can be added to any unused pins in the configuration file and displayed along side the FS1106 generated labels in the state listing screen.

## Timing Mode and the FS1106 software

The FS1106 software should be disabled when the logic analyzer is configured in timing mode. This is because the FS1106 can only operate on state acquired data.

## Custom Configurations

Custom configurations are those where the user has created their own connection between the target bus and the logic analyzer. In these cases the user must use their pinout and modify the FORMAT menu to assign the signal to the matching logic analyzer POD and channel. It is suggested that the user start with the CP1106\_7 configuration file and make the modification from there. The CP1106\_7 format menu is shown here.

Label	Clk Inputs	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
ADDR				15-0	15-0		
ADDR_B		15-0	15-0				
USER	K						
INTA_D						7-4(D,C,B,A)	
RESET						8	
C/B7_4							15-12(C/BE4,6,5,7)
C/B3_0						12,13 (CBE3,2)	5,7(C/BE1,0)
CMD						12,13 (CBE3,2)	5,7(C/BE1,0)
DATA				15-0	15-0		
DEVSEL						15	
STOP							0
LOCK							1
PERR							2
SERR							4
PAR							3
ACK/RQ							11,10
IRDY	L						
FRAME	K						
TRDY						14	
PCICLK	J						
IDSEL						11	
GNT						9	
REQ						10	
CYCLE	L,K,M					15,14,13,12	9,7,5,0
DFRAME*	M						
DDFRAME*							9
PME							8
LCM3_0*						3,2,0,1	

\* These signals are created on the FS2007 and are not part of the actual PCI bus.

## The CYCLE variable

The CYCLE variable in the CP1106\_7 configuration file is made up of the following signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL# ,STOP#. This variable has 31 symbols defined that can be used to help make triggering, timing analysis and pattern filtering easier. The following lists the bit pattern and the corresponding symbol.

Symbol	DFRAME#	IRDY#	FRAME#	TRDY#	DEVSEL#	C/BE(3:0)	DDFRAME#	STOP#
INTACK	1	1	0	1	1	0000	X	1
SPEC CYC	1	1	0	1	1	0001	X	1
I/O RD	1	1	0	1	1	0010	X	1
I/O WR	1	1	0	1	1	0011	X	1
RESVRD	1	1	0	1	1	0100	X	1
RESVRD	1	1	0	1	1	0101	X	1
MEM RD	1	1	0	1	1	0110	X	1
MEM WR	1	1	0	1	1	0111	X	1
RESRVD	1	1	0	1	1	1000	X	1
RESRVD	1	1	0	1	1	1001	X	1
CON RD	1	1	0	1	1	1010	X	1
CON WR	1	1	0	1	1	1011	X	1
MEMRDM	1	1	0	1	1	1100	X	1
DAD CY	1	1	0	1	1	1101	X	1
MEMRDL	1	1	0	1	1	1110	X	1
MEMWRI	1	1	0	1	1	1111	X	1
IO XACTION	1	1	0	1	1	001X	X	1
MEM XACTION	1	1	0	1	1	011X	X	1
CONFIG XACTION	1	1	0	1	1	101X	X	1
ADD CYCLE	1	1	0	1	1	XXXX	X	1
DATA XFER	X	0	0	0	0	XXXX	X	1
WAIT TARGET	X	0	X	1	0	XXXX	X	1
WAIT INITIATOR	X	1	X	0	0	XXXX	X	1
DATA FINALXFER	X	0	1	0	0	XXXX	X	1
STOP NOXFER	X	1	0	X	0	XXXX	X	0
STOP DATAXFER	X	0	X	0	0	XXXX	X	0
STOP RETRY	X	0	1	1	0	XXXX	X	0
TARGET ABORT	X	1	0	1	1	XXXX	X	0
IDLE	X	1	1	X	X	XXXX	X	X
WAIT NODEVSEL	X	0	X	X	1	XXXX	X	1
WAIT NODVSEL/F 0	X	0	0	X	1	XXXX	X	1

## Bit Re-ordering

The included configuration file CP1106\_7 has the following labels that have been re-ordered. The bit re-ordering function can be found in the FORMAT menu. If the sample pinout is not used then the re-ordering will need to be modified to reflect the shown ordering in order for the supplied configuration symbols to be correct.

Below is a list of signals and the corresponding bit re-ordering.

***The Cycle Variable***

<b>Probe Channel</b>	<b>Map to bit</b>
0	0
1	2
2	1
3	4
4	3
5	5
6	6
7	7
8	8

***C/BE3:0***

<b>Probe Channel</b>	<b>Map to bit</b>
0	1
1	0
2	3
3	2

***C/BE7:4***

<b>Probe Channel</b>	<b>Map to bit</b>
0	3
1	1
2	2
3	0

## ***Other labels***

Two other labels are created by the FS1106 Transaction Decode software. These labels can be used by downstream tools such as SPA (System Performance Analysis Tool). These labels should not be used for triggering since they are not valid until AFTER the data has been acquired.

### ***CMD label***

<b>Meaning</b>	<b>Bit Pattern</b>
INTACK	0000
SPECIAL CYCLE	0001
I/O READ	0010
I/O WRITE	0011
RESERVED	0100-0101
MEM READ	0110
MEM WRITE	0111
RESERVED	1000
RESERVED	1001
CONF READ	1010
CONF WRITE	1011
MEMORY READ MULTIPLE	1100
DAC	1101
MEM READ LINE	1110
MEM WRITE AND INVALIDATE	1111
IO XACTION	001X
MEM XACTION	011X
CONFIG XACTION	101X

***TERM CODE***

<b>Meaning</b>	<b>Bit Pattern</b>
INITIATOR	0
STOP W/ DATA	1
STOP NO DATA	2
STOP RETRY	3
MASTER ABORT	4
TARGET ABORT	5

# State Analysis

This chapter explains how to configure the Agilent logic analyzer and FS1106 software to perform state analysis on the PCI Local Bus. The next chapter explains how to configure the FS1106 to perform timing analysis.

## Functionality of the FS1106 Software

The FS1106 Performance Consultant Software will perform the following functions:

- ◆ Decode all PCI command and cycle types
- ◆ Provide insight into the data transfer by indicating burst length, byte enables and number of byte enables. These are all color coded to match the command.
- ◆ Color the transaction per the command for easy correlation. The colors used by the software are as follows:
  - ◆ Memory transactions: Green
  - ◆ I/O transactions: Yellow
  - ◆ Configuration transactions: Blue
  - ◆ Interrupt Acknowledge, Special Cycle transactions and the DAC cycle: Purple
  - ◆ Idle and Wait cycles: White
- ◆ Determine the following performance metrics.
  - ◆ Latency: data to data and address to first data. This label is color coded to indicate spec compliance.
  - ◆ Byte Enable Efficiency
  - ◆ Total Efficiency
  - ◆ Overall Time Efficiency
- ◆ Provide a quick summary of the traffic through the Command/Address and Length/Termination labels.
- ◆ Remove the input data set to present an uncluttered display

## Acquiring Data

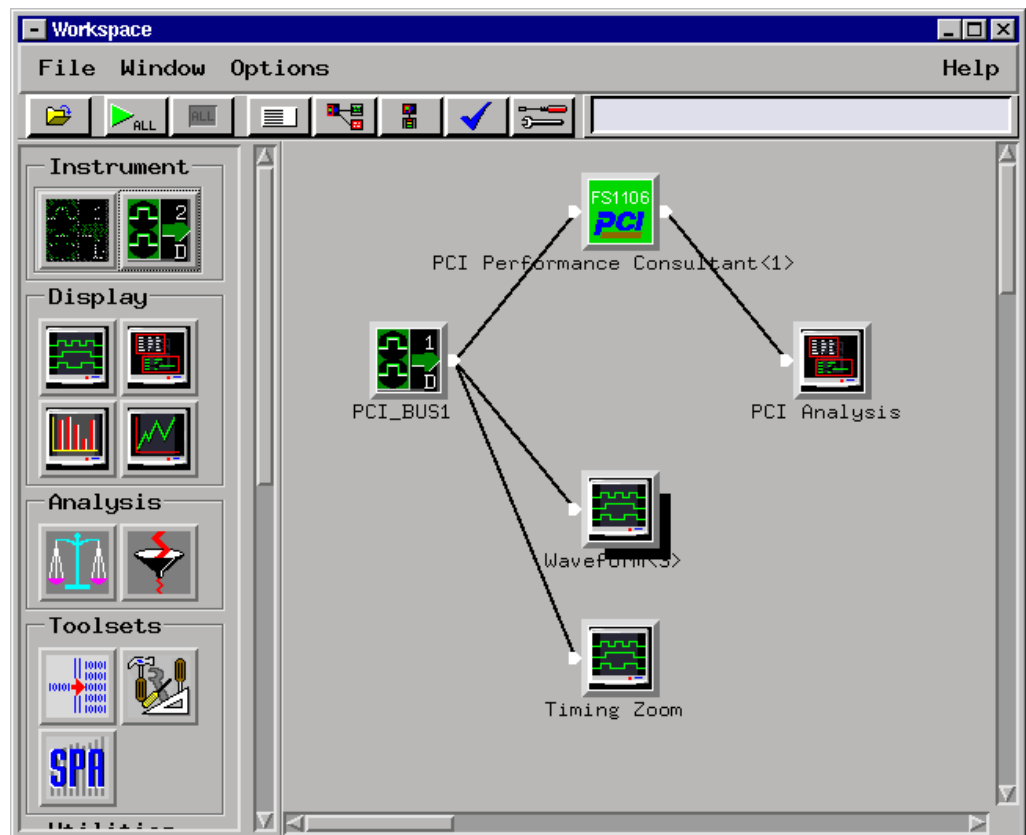
Configure the trigger menu to acquire PCI data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you select STOP.

The logic analyzer will flash “Slow or Missing Clock” if it does not see the PCI signal CLK toggling.

The logic analyzer will flash “Waiting in level 1” if the trigger specification has not been met.

## Configuring the Workspace for PCI Analysis

For full analysis, the PCI workspace should appear as below. Filter tool icons, System Performance icons and others can be copied several times over onto the workspace.



# The State Listing Display

Captured data is as shown in the following figure.

Time	Command	Address_L	Data_L	Termination	Burst Length	Byte Enable	Num
Relative	Text	Hex	Text	Text	Decimal	Hex	Dec
572,392 us	Mem Read						
328,000 ns		07FC0734	07FB08E2	Initiator	0004	0	04
96,000 ns	Mem Read						
328,000 ns		07FB08E0	07FA0C82			0	04
32,000 ns		07FB08E4	07FB0940	Initiator	0008	0	04
88,000 ns	Mem Read						
512,000 ns		07FB0940	07FB0940			0	04
24,000 ns		07FB0944	020007FF			0	04
32,000 ns		07FB0948	FFE080E1			0	04
32,000 ns		07FB094C	00000000	Initiator	0016	0	04
120,000 ns	Mem Read						
328,000 ns		07FA0C80	07FB0982			0	04
32,000 ns		07FA0C84	07FA0CA1	Initiator	0008	0	04
416,000 ns	Mem Read						
336,000 ns		07FB0980	07FB0983			0	04
24,000 ns		07FB0984	07FB0960	Initiator	0008	0	04
96,000 ns	Mem Read						
328,000 ns		07FB0960	07FB0960			0	04
32,000 ns		07FB0964	02000000			0	04
24,000 ns		07FB0968	FFE080E1			0	04
32,000 ns		07FB096C	00000000	Initiator	0016	0	04
996,640 us	Mem Read						
328,000 ns		07FC0738	07FB08E2	Initiator	0004	0	04

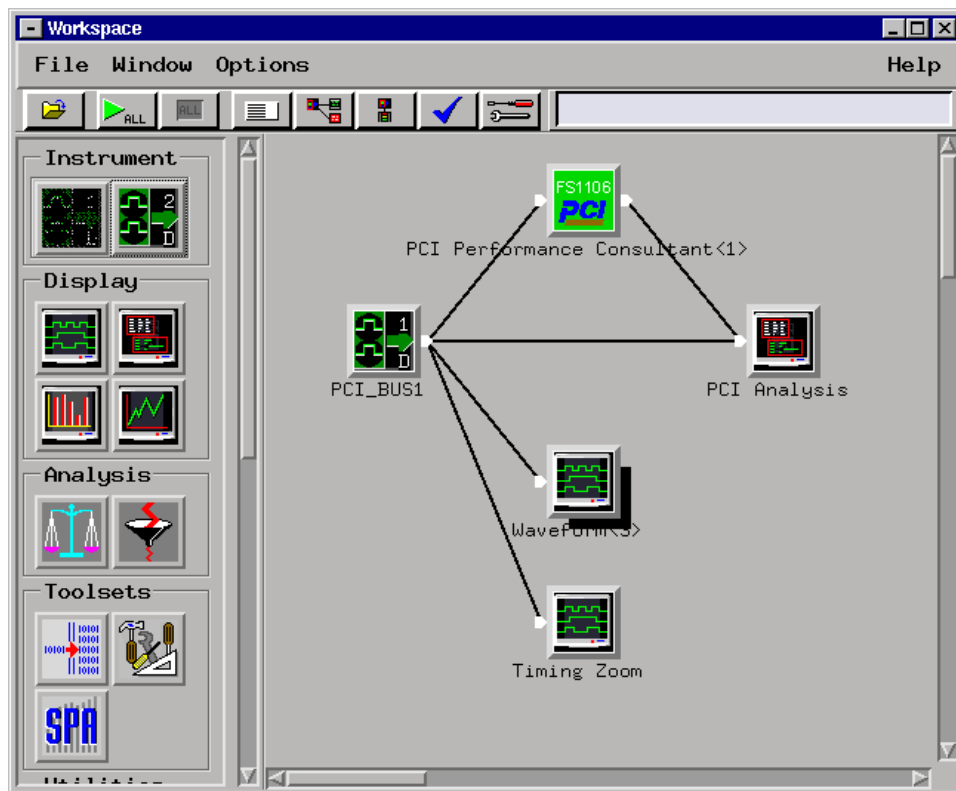
Mbytes/sec	Command/Address	Length/Termination	Clocks	Time
Decimal	Text	Text	Decimal	Relativ
0004	I/O Read, adr = 0x00040344	1 bytes, Initiator	0000047162	3,120
			0000047170	216,000
	I/O Write, adr = 0x00008009	4 bytes, Initiator	0000047704	15,992
0045	Cfg Read, adr = 0x00000CFC	1 bytes, Initiator	0000047708	88,000
			0000047746	1,168
0005	I/O Write, adr = 0x0004030C	4 bytes, Initiator	0000047752	184,000
			0000047844	2,760
0045	Cfg Read, adr = 0x00000CFC	2 bytes, Initiator	0000047848	88,000
			0000047886	1,168
0010	I/O Write, adr = 0x00040344	4 bytes, Initiator	0000047892	184,000
			0000048070	5,312
0045	Cfg Read, adr = 0x00000CFC	1 bytes, Initiator	0000048074	88,000
			0000048112	1,168
0005	I/O Write, adr = 0x0004030C	4 bytes, Initiator	0000048118	184,000
			0000048212	2,824
0045	Cfg Read, adr = 0x00000CFC	1 bytes, Initiator	0000048215	88,000
			0000048254	1,168
0005	Cfg Write, adr = 0x00040384	1 bytes, Initiator	0000048260	184,000
			0000048303	1,256
0005	I/O Write, adr = 0x00040384	4 bytes, Initiator	0000048309	184,000
			0000048450	4,232
0045	Cfg Read, adr = 0x00000CFC	1 bytes, Initiator	0000048453	88,000
			0000048492	1,168

The following is a list of the generated columns from the FS1106 PCI Performance Consultant tool.

<b>Name</b>	<b>Base</b>	<b>Description</b>
Command	TEXT	The command name
Address_H	HEX	The address as it appears during a 64 bit address transfer (as defined by a DAC)
Address_L	HEX	The address as it appears on the lower AD lines (AD[31:0]). This HEX value is incremented during burst transactions
Data_L	HEX	The lower 32 bit AD lines representing data
Data_H	HEX	The upper 32 bit AD lines representing data
BE_H	HEX	High order data byte enables
BE_L	HEX	Low order data byte enables
Latency	Decimal	Number of states between data phases or if the first data phase the number of states between address and first data phase. This label is color coded to indicate spec compliance. Green indicates within spec, yellow indicates marginal, and red indicates out of spec.
Termination	TEXT	Termination type
Command/Address	TEXT	A summary giving the command and starting address
Length/Termination	TEXT	A summary giving the length of the data transfer and the termination
TERM CODE	HEX	Termination type displayed in HEX (for use in SPA and filter tools)
CMD	HEX	The command type displayed in HEX (for use in SPA and filter tools)
Clocks	Decimal	The number of clock tics that have elapsed. This takes into consideration those states filtered out by the Trigger menu store qualification
Burst Length	Decimal	The length of the transaction in bytes and indicated at the end of the transaction
Num Byte Enables	Decimal	Number of byte enables asserted for that data transfer
Byte Enable Efficiency %	Decimal	Byte enable efficiency Data clocks (taking into consideration the Byte enables)/Total clocks in percent
Efficiency %	Decimal	Time efficiency of the transaction. Data Clocks/Busy Clocks.
Total Efficiency %	Decimal	Time efficiency * Byte enable efficiency
Mbytes/sec	Decimal	Burst Length/Transaction time

## The PCI Bus signals in the Lister Display

The FS1106 software removes the raw PCI bus signals from the output display for easy reading. However these signals are important and can quickly be added back into the display by connecting the logic analyzer directly to the lister. Once this is done the output of the FS1106 software will appear alongside the acquired PCI bus signals.



## Using the Filter tool

Since the PCI Performance Consultant tool creates unique columns in the listing window these columns and their contents may be used by the filter tool.

## Using the System Performance tool

The System Performance Analysis tool or SPA can be used to create histogram displays of various PCI metrics. The hex based labels created by the FS1106 software were specifically created for use with the SPA tool.

## Summary of Performance Data

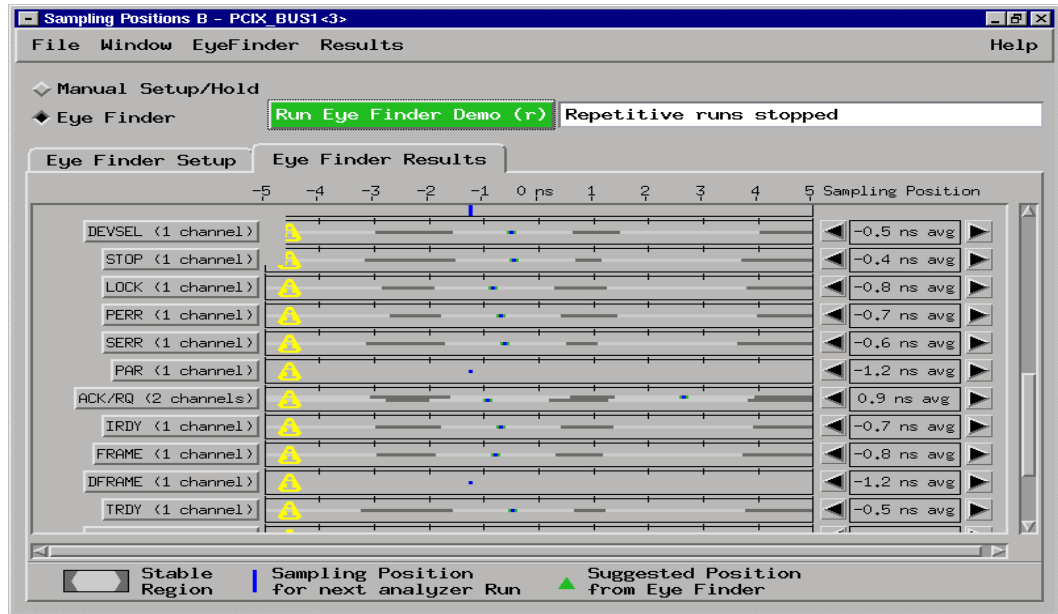
A short summary of the acquired data is written to a text file at logic/pciperf.txt. This file can be viewed on the analyzer or offline on a workstation or PC.

## Transactor Software Decode Time

The current architecture of the 16700 is such that the entire buffer of captured data is decoded all at once. This leads to a long decode time prior to seeing the data decoded in the listing window. Future revisions of the 16700 operating system and a re-write of the FS1106 software will solve this problem. The anticipated date for this revision will be prior to June 2001. All customers will receive free updates. In the interim it is suggested that the acquisition buffer size of the logic analyzer be set to below 64K.

## Use of Eye Finder

Use of Eye Finder can greatly enhance your analysis by helping find the data valid window of every signal on the bus with respect to the clock. You can compare the results of Eye Finder to your simulation and the PCI specification to see if your system operates within expected setup and hold margins. Eye Finder can be found in the setup and hold area of your logic analyzer card FORMAT menu.



# Timing Analysis

## Timing Mode and the FS1106 software

Since the passive FuturePlus PCI analysis probes do not buffer the PCI bus they introduce negligible skew to the PCI Local Bus signals.

The FS1106 software should be disabled when the logic analyzer is configured in timing mode. This is because the FS1106 can only operate on state acquired data.

## Installation Quick Reference

The following procedure describes the major steps required to perform timing analysis measurements on the passively probed PCI target.

1. After removing the probe tip assemblies, plug the logic analyzer PODs into the analysis probe cable headers.
2. Load the logic analyzer configuration file from the logic/configs/FuturePlus/FS1106 directory.
3. Configure the logic analyzer for TIMING mode.
4. **DELETE the FS1106 ICON from the workspace OR open the tool and select DISABLE.**

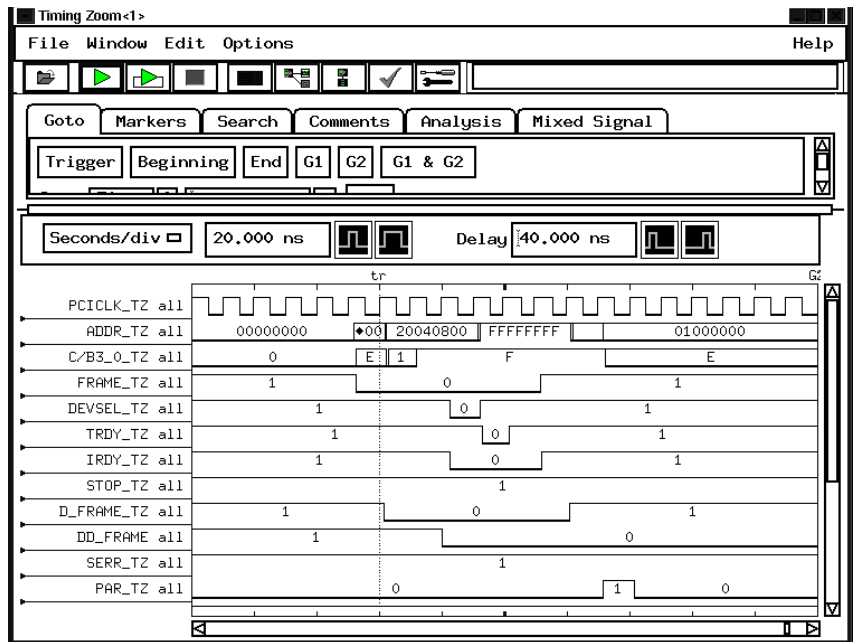
## Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE, or when you touch STOP.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

## The Waveform Display

Captured data is displayed as shown in the following figure.



## Timing Zoom

Most of the analyzers in the 16715 family or above come with Timing Zoom. Timing zoom is especially useful for passively probed busses because it gives the user simultaneous state and timing. The timing zoom acquired signals are indicated by an \_TZ appended onto the signal name. For more information of Timing Zoom please refer to you Agilent logic analyzer documentation.