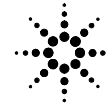


FuturePlus Systems Corporation



**Agilent Technologies**  
Innovating the HP Way

---

Premier Solution Partner



---

# **FS1105 PCI Compliance Consultant Software Users Manual**

**For use with Agilent Logic Analyzers**

**Revision – 1.1**

Copyright 2001 FuturePlus Systems® Corporation  
FuturePlus is a trademark of FuturePlus Systems Corporation

<i>How to reach us</i> .....	4
<i>Software License Agreement</i> .....	5
License Agreement .....	5
Use of the software .....	5
Copies and Adaptations.....	5
Ownership.....	5
Sublicensing and Distribution.....	5
Termination .....	6
Export Clause .....	6
Limitation of warranty .....	6
Exclusive Remedies .....	6
Assistance.....	6
<i>Introduction</i> .....	7
How to Use This Manual .....	7
<i>Getting Ready</i> .....	8
Accessories Supplied .....	8
Minimum Equipment Required.....	8
Signal Naming Conventions .....	8
Licensing .....	8
Licensing Area .....	9
Probing your PCI Target.....	10
Supported Logic Analyzers .....	10
Setting up the Software on the Analyzer.....	10
Loading the FS1105 Software .....	11
Assigning additional signals .....	12
Timing Mode and the FS1105 software .....	12
Custom Configurations.....	12
The CYCLE variable.....	13
Bit Re-ordering .....	13
The Cycle Variable .....	14
C/BE3:0.....	14
C/BE7:4.....	14
Other labels .....	15
CMD label.....	15
TERM CODE.....	16
<i>State Analysis</i> .....	17
Functionality of the FS1105 Software .....	17
Configuring the Workspace for PCI Analysis.....	18
Acquiring Data .....	18

<b>The State Listing Display.....</b>	<b>19</b>
Compliance Violations.....	21
<b>Masking Protocol Errors.....</b>	<b>23</b>
<b>The PCI Bus signals in the Lister Display.....</b>	<b>24</b>
<b>Using the Filter tool.....</b>	<b>24</b>
<b>Using the System Performance tool.....</b>	<b>25</b>
<b>Transactor Software Decode Time .....</b>	<b>25</b>
<b>Use of Eye Finder .....</b>	<b>26</b>
<b><i>Timing Analysis .....</i></b>	<b><i>27</i></b>
<b>Timing Mode and the FS1105 software .....</b>	<b>27</b>
<b>Installation Quick Reference.....</b>	<b>27</b>
<b>Acquiring Data .....</b>	<b>27</b>
<b>The Waveform Display .....</b>	<b>28</b>
<b>Timing Zoom .....</b>	<b>28</b>

# How to reach us

**For Technical Support:**

FuturePlus Systems Corporation  
36 Olde English Road  
Bedford, NH 03110  
TEL: 603-471-2734  
FAX: 603-471-2738  
On the web <http://www.futureplus.com>

**For Sales and Marketing Support:**

FuturePlus Systems Corporation  
TEL: 719-278-3540  
FAX: 719-278-9586  
On the web <http://www.futureplus.com>

FuturePlus Systems has technical sales representatives in several major countries. For an up to date listing please see <http://www.futureplus.com/contact.html>.

Agilent Technologies is also an authorized reseller of many FuturePlus products. Contact any Agilent Technologies sales office for details.

# Software License Agreement

**IMPORTANT Please read carefully this license agreement before opening the media envelope.** Rights in the software are offered only on the condition that the customer agrees to all terms and conditions of the license agreement. Opening the media envelope indicates your acceptance of these terms and conditions. If you do not agree to the licensing agreement, you may return the unopened package for a full refund.

## License Agreement

In return for payment for this product, FuturePlus Systems grants the Customer a SINGLE user LICENSE in the software subject to the following:

## Use of the software

Customer may use the software on any one Agilent 1670x mainframe logic analysis system.

- Customer may not reverse assemble or decompile the software.

## Copies and Adaptations

Customer may make copies or adaptations of the software:

- For archival purpose only
- When copying for adaptation is an essential step in the use of the software with the logic analyzer and/or logic analysis mainframe so long as the copies and adaptations are used in no other manner. Customer has no right to copy software unless it acquires an appropriate license to reproduce from FuturePlus Systems.

## Ownership

- Customer agrees that it does not have any title or ownership of the software, other than the physical media.
- Customer acknowledges and agrees that the software is copyrighted and protected under the copyright laws.
- Transfer of the right of ownership shall only be done with the consent of FuturePlus Systems.

## Sublicensing and Distribution

Customer may not sublicense the software or distribute copies of the software to the public in physical media, or by electronic means, or any other means without the prior written consent of FuturePlus Systems.

**Termination**

FuturePlus systems may terminate this software license for failure to comply with any of these terms provided and FuturePlus Systems has requested the Customer to cure the failure and Customer has failed within 30 days of such notice.

**Export Clause**

Customer agrees not to export or re-export the software or any copy or adaptation in violation of the U.S. Export Administration regulations or other applicable regulation.

**Limitation of warranty**

FuturePlus Systems warrants that its software designated by FuturePlus Systems for use with an instrument will execute its programming instructions when properly installed on that instrument. FuturePlus Systems does not warrant that the operation of the software will be uninterrupted or error-free.

The foregoing warranty shall not apply to defects resulting from improper or inadequate use by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. FUTUREPLUS SYSTEMS SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

***Exclusive Remedies***

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. FUTUREPLUS SYSTEMS SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

**Assistance**

Product maintenance agreements and other customer assistance agreements are available for FuturePlus Systems products. For assistance, contact FuturePlus Systems.

# Introduction

This product is a B4605B Tool Development Kit generated software tool that will take the input labels from the passive PCI configuration file FORMAT menu and generate columns in the listing screen. These columns will decode the PCI bus traffic in an easy to read format and provide additional compliance information.

The FS1105 will come with several sample configuration files that match the passive PCI products from FuturePlus Systems. Customers with custom pinouts can use any of these files and modify them for their own custom configuration.

The configuration software on the diskette sets up the format specification menu of the logic analyzer for compatibility with the specified FuturePlus PCI analysis probe. Once installed, the FS1105 PCI Compliance Consultant software will appear as an icon in the CUSTOM area of your workspace.

This manual is organized to help you quickly find the information you need.

## How to Use This Manual

- The **Getting Ready** chapter discusses the installation procedure and minimum equipment required to use the FS1105 product.
- The **State Analysis** chapter explains how to configure the logic analyzer and FS1105 software for state analysis.
- The **Timing Analysis** chapter explains how to configure the logic analyzer for timing analysis.

# Getting Ready

This chapter discusses the installation procedure, minimum equipment required to use the FS1105 product and the logic analyzer configuration files.

## Accessories Supplied

The FS1105 product consists of the following accessories:

- Two diskettes containing the configuration files and FS1105 software.
- This operating manual

## Minimum Equipment Required

The minimum equipment required for analysis of a PCI Local Bus using the FS1105 product consists of the following equipment:

- Agilent 16700 analysis frame with the 16715 analyzer card or better.
- Revision 2.0 or better of the Agilent Logic analysis frame software.
- The FS1105 Product
- A PCI target bus

## Signal Naming Conventions

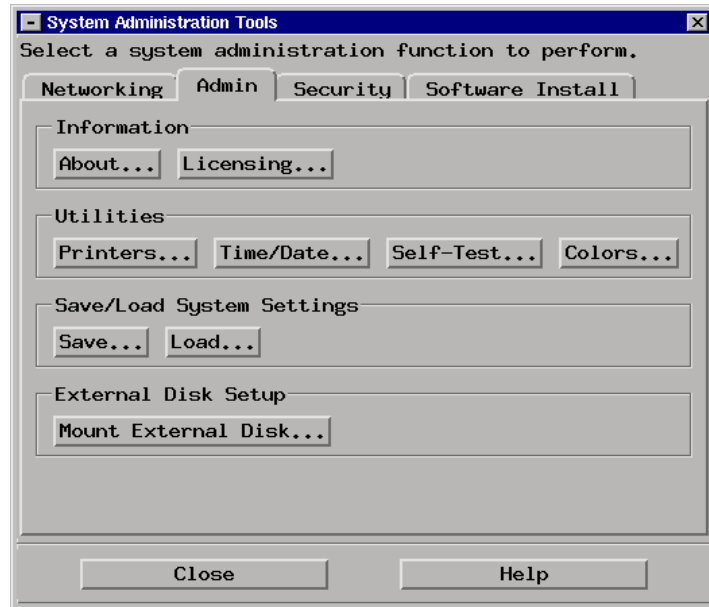
This operating manual uses the same signal notation as the PCI LOCAL BUS SPECIFICATION - REVISION 2.2 That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

## Licensing

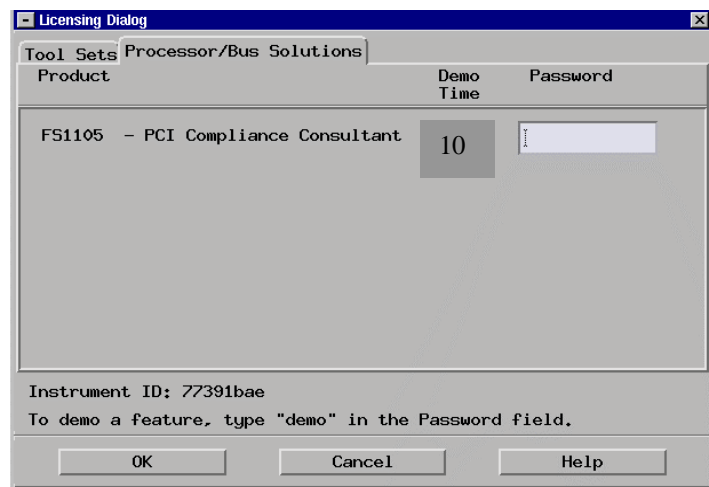
The FS1105 product is a licensed product which is locked to a single Agilent 1670x frame. A demo time is provided by typing the word *demo* into the licensing area next to the product name. The licensing area for the 1670x mainframe is found under System Administration. For use of the FS1105 product beyond the demo time please contact FuturePlus Systems at [www.futureplus.com](http://www.futureplus.com) or 719-278-3540.

## Licensing Area

The following shows the ADMIN tab under System Administration Tools. Select Licensing once the FS1105 software is installed.



Under licensing the Processor/Bus Solutions tab can be selected to yield the following menu. Once the password is entered select OK.



## Probing your PCI Target

For FuturePlus Systems passive PCI analysis probes follow the installation instructions that came with the product. For custom configurations use one of the provided configuration files and reassign each label in the FORMAT menu to match the custom configuration. Please note that the SYMBOLS provided will not decode properly unless the bits have been reordered to reflect the original assigned order.

For custom probing information refer to the below documents on the FuturePlus Systems web site at [www.futureplus.com](http://www.futureplus.com) under Technical Support

- Designing Your Own Physical Connection To A 32/64-bit Embedded PCI Bus For Use With FuturePlus PCI Analysis Tools

## Supported Logic Analyzers

The included FS1105 configuration files only support the 16715 family and above of logic analyzer cards. However, the FS1105 Compliance Consultant tool will work when connected to the 1655x or 16710,16711 and 16712 logic analyzer cards on the 1670x workspace.

## Setting up the Software on the Analyzer

The FS1105 software consists of two diskettes.

- The FS1105 Configuration Software diskette
- The FS1105 PCI Compliance Consultant diskette

To install the configuration files insert the diskette labeled **FS1105 PCI Configuration Software** into the Agilent 16700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL*.

To install the FS1105 PCI transactor and compliance software insert the diskette labeled **FS1105 PCI Compliance Consultant** into the Agilent 16700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL*.

**This procedure does not need to be repeated. It only needs to be done the first time the FS1105 software is used.**

When this has completed load the appropriate configuration file from the /configs/FuturePlus/FS1105 directory. Refer to the below table for a list of analyzers and corresponding configuration files.

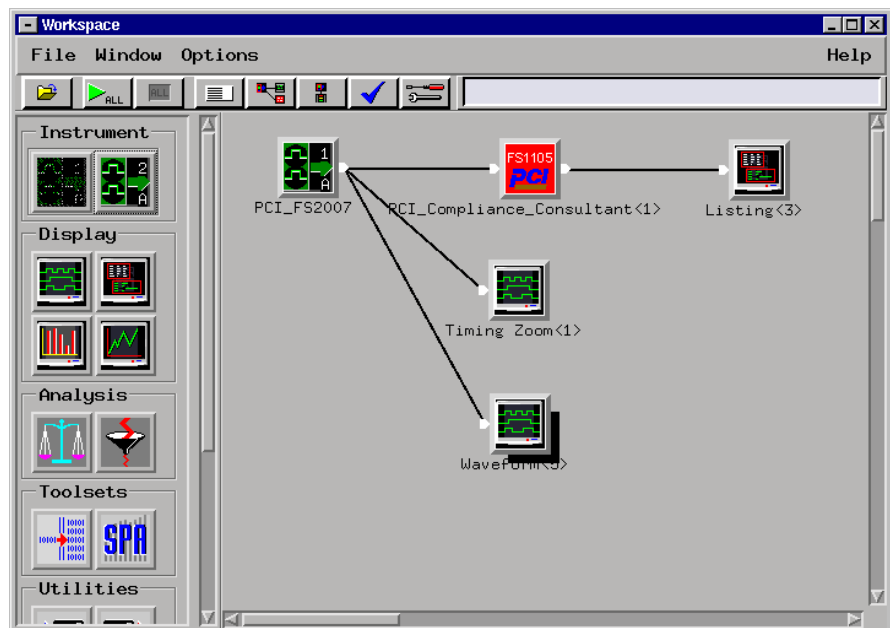
The only analyzers supported by the **supplied** FS1105 configuration files are the 16715 or better.

FuturePlus Product	File name for State/Timing Analysis	Description
FS2000	CP1105_1	32 bit/ 33Mhz PCI w/ extender
FS2001	CP1105_2	32/64 bit 33/66 MHz
FS2005/6	CP1105_3	32/64 bit 33/66 MHz w/ extender
FS2004	CP1105_4	32 bit Cardbus
FS3010	CP1105_5	32 bit 33 MHz PMC
FS3020	CP1105_6	32/64 bit 33Mhz CompactPCI
FS2007	CP1105_7	PCI/PCI-X 32/64 bit 33/66/133Mhz

Some of the above configuration files require two logic analyzer cards melded for 64 bit analysis. For 32 bit analysis only one logic analyzer card is required. When loading the configuration file into a one card configuration a yellow warning message will appear that notes that the two extra pods are not being loaded. This message will not affect proper operation and is merely for notification purposes.

## Loading the FS1105 Software

Loading the configuration file will automatically load the FS1105 icon onto the workspace. Once the configuration file is loaded the workspace should appear as below.



## Assigning additional signals

Any additional signals can be added to any unused pins in the configuration file and displayed along side the FS1105 generated labels in the state listing screen.

## Timing Mode and the FS1105 software

The FS1105 software should be disabled when the logic analyzer is configured in timing mode. This is because the FS1105 can only operate on state acquired data.

## Custom Configurations

Custom configurations are those where the user has created their own connection between the target bus and the logic analyzer. In these cases the user must use their pinout and modify the FORMAT menu to assign the signal to the matching logic analyzer POD and channel. It is suggested that the user start with the CP1105\_7 configuration file and make the modification from there. The CP1105\_7 format menu is shown here.

Label	Clk Inputs	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
ADDR				15-0	15-0		
ADDR_B		15-0	15-0				
USER	K						
INTA_D						7-4(D,C,B,A)	
RESET						8	
C/B7_4							15-12(C/BE4,6,5,7)
C/B3_0						12,13 (CBE3,2)	5,7(C/BE1,0)
CMD						12,13 (CBE3,2)	5,7(C/BE1,0)
DATA				15-0	15-0		
DEVSEL							15
STOP							0
LOCK							1
PERR							2
SERR							4
PAR							3
ACK/RQ							11,10
IRDY	L						
FRAME	K						
TRDY						14	
PCICLK	J						
IDSEL						11	
GNT						9	
REQ						10	
CYCLE	L,K,M					14,13,12	15,9,7,5,0
DFRAME*	M						
DDFRAME*							9
PME							8
LCM3_0*						3,2,0,1	

\* These signals are created on the FS2007 and are not part of the actual PCI bus and are NOT needed for the FS1105 software.

## The CYCLE variable

The CYCLE variable in the CP1105\_7 configuration file is made up of the following signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL#, STOP#. This variable has 31 symbols defined that can be used to help make triggering, timing analysis and pattern filtering easier. The following lists the bit pattern and the corresponding symbol.

Symbol	DFRAME#	IRDY#	FRAME#	TRDY#	DEVSEL#	C/BE(3:0)	DDFRAME#	STOP#
INTACK	1	1	0	1	1	0000	X	1
SPEC CYC	1	1	0	1	1	0001	X	1
I/O RD	1	1	0	1	1	0010	X	1
I/O WR	1	1	0	1	1	0011	X	1
RESVRD	1	1	0	1	1	0100	X	1
RESVRD	1	1	0	1	1	0101	X	1
MEM RD	1	1	0	1	1	0110	X	1
MEM WR	1	1	0	1	1	0111	X	1
RESRVD	1	1	0	1	1	1000	X	1
RESRVD	1	1	0	1	1	1001	X	1
CON RD	1	1	0	1	1	1010	X	1
CON WR	1	1	0	1	1	1011	X	1
MEMRDM	1	1	0	1	1	1100	X	1
DAD CY	1	1	0	1	1	1101	X	1
MEMRDL	1	1	0	1	1	1110	X	1
MEMWRI	1	1	0	1	1	1111	X	1
IO XACTION	1	1	0	1	1	001X	X	1
MEM XACTION	1	1	0	1	1	011X	X	1
CONFIG XACTION	1	1	0	1	1	101X	X	1
ADD CYCLE	1	1	0	1	1	XXXX	X	1
DATA XFER	X	0	0	0	0	XXXX	X	1
WAIT TARGET	X	0	X	1	0	XXXX	X	1
WAIT INITIATOR	X	1	X	0	0	XXXX	X	1
DATA FINALXFER	X	0	1	0	0	XXXX	X	1
STOP NOXFER	X	1	0	X	0	XXXX	X	0
STOP DATAXFER	X	0	X	0	0	XXXX	X	0
STOP RETRY	X	0	1	1	0	XXXX	X	0
TARGET ABORT	X	1	0	1	1	XXXX	X	0
IDLE	X	1	1	X	X	XXXX	X	X
WAIT NODEVSEL	X	0	X	X	1	XXXX	X	1
WAIT NODVSEL/F 0	X	0	0	X	1	XXXX	X	1

## Bit Re-ordering

The included configuration file CP1105\_7 has the following labels that have been re-ordered. The bit re-ordering function can be found in the FORMAT menu. If the sample pinout is not used then the re-ordering will need to be modified to reflect the shown ordering in order for the supplied configuration symbols to be correct.

Below is a list of signals and the corresponding bit re-ordering.

***The Cycle Variable***

<b>Probe Channel</b>	<b>Map to bit</b>
0	0
1	2
2	1
3	4
4	3
5	5
6	6
7	7
8	8

***C/BE3:0***

<b>Probe Channel</b>	<b>Map to bit</b>
0	1
1	0
2	3
3	2

***C/BE7:4***

<b>Probe Channel</b>	<b>Map to bit</b>
0	3
1	1
2	2
3	0

## ***Other labels***

Two other labels are created by the FS1105 Transaction Decode software. These labels can be used by downstream tools such as SPA (System Performance Analysis Tool). These labels should not be used for triggering since they are not valid until AFTER the data has been acquired.

### ***CMD label***

<b>Meaning</b>	<b>Bit Pattern</b>
INTACK	0000
SPECIAL CYCLE	0001
I/O READ	0010
I/O WRITE	0011
RESERVED	0100-0101
MEM READ	0110
MEM WRITE	0111
RESERVED	1000
RESERVED	1001
CONF READ	1010
CONF WRITE	1011
MEMORY READ MULTIPLE	1100
DAC	1101
MEM READ LINE	1110
MEM WRITE AND INVALIDATE	1111
IO XACTION	001X
MEM XACTION	011X
CONFIG XACTION	101X

***TERM CODE***

<b>Meaning</b>	<b>Bit Pattern</b>
INITIATOR	0
STOP W/ DATA	1
STOP NO DATA	2
STOP RETRY	3
MASTER ABORT	4
TARGET ABORT	5

# State Analysis

This chapter explains how to configure the Agilent logic analyzer and FS1105 software to perform state analysis on the PCI Local Bus. The next chapter explains how to configure the FS1105 to perform timing analysis.

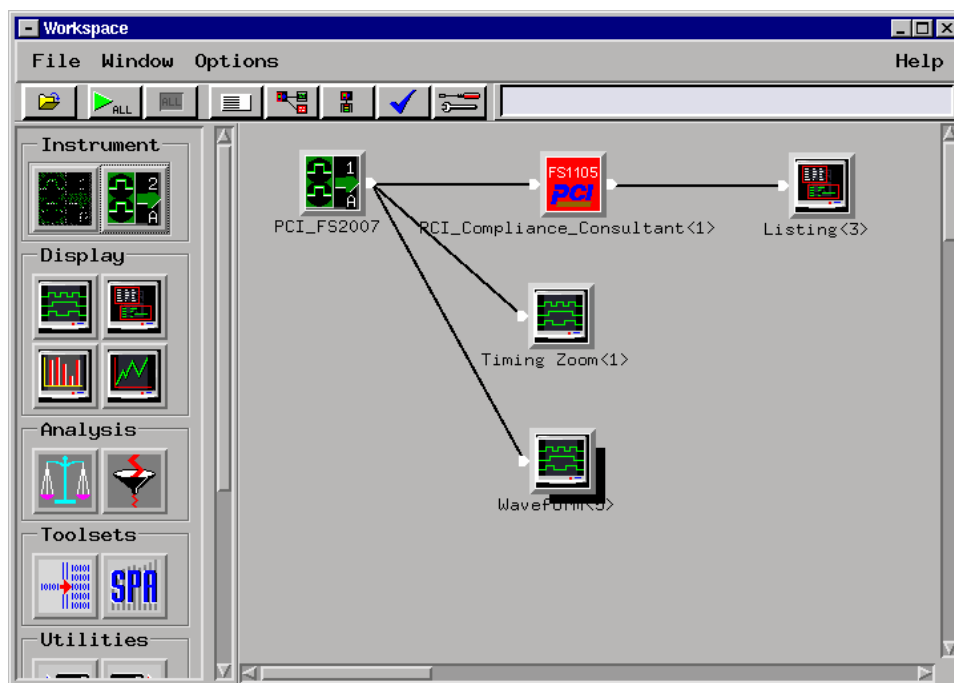
## Functionality of the FS1105 Software

The FS1105 compliance Consultant Software will perform the following functions:

- Decode all PCI command and cycle types
- Color the transaction per the command for easy correlation. The colors used by the software are as follows:
  - Memory transactions: Green
  - I/O transactions: Yellow
  - Configuration transactions: Blue
  - Interrupt Acknowledge, Special Cycle transactions and the DAC cycle: Purple
  - Idle and Wait cycles: White
- Verify 26 different compliance rules
- Provide a quick method of masking each compliance rule
- Remove the input data set to present an uncluttered display

## Configuring the Workspace for PCI Analysis

For full analysis, the PCI workspace should appear as below. Filter tool icons, System Performance icons and others can be copied several times over onto the workspace.



## Acquiring Data

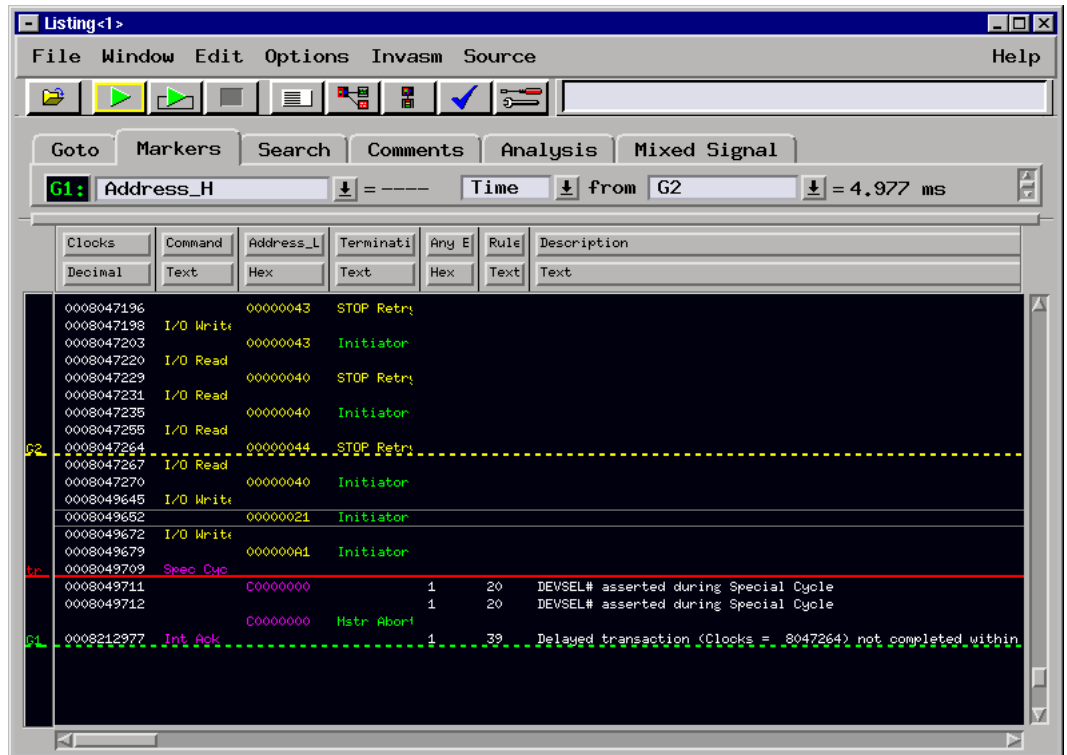
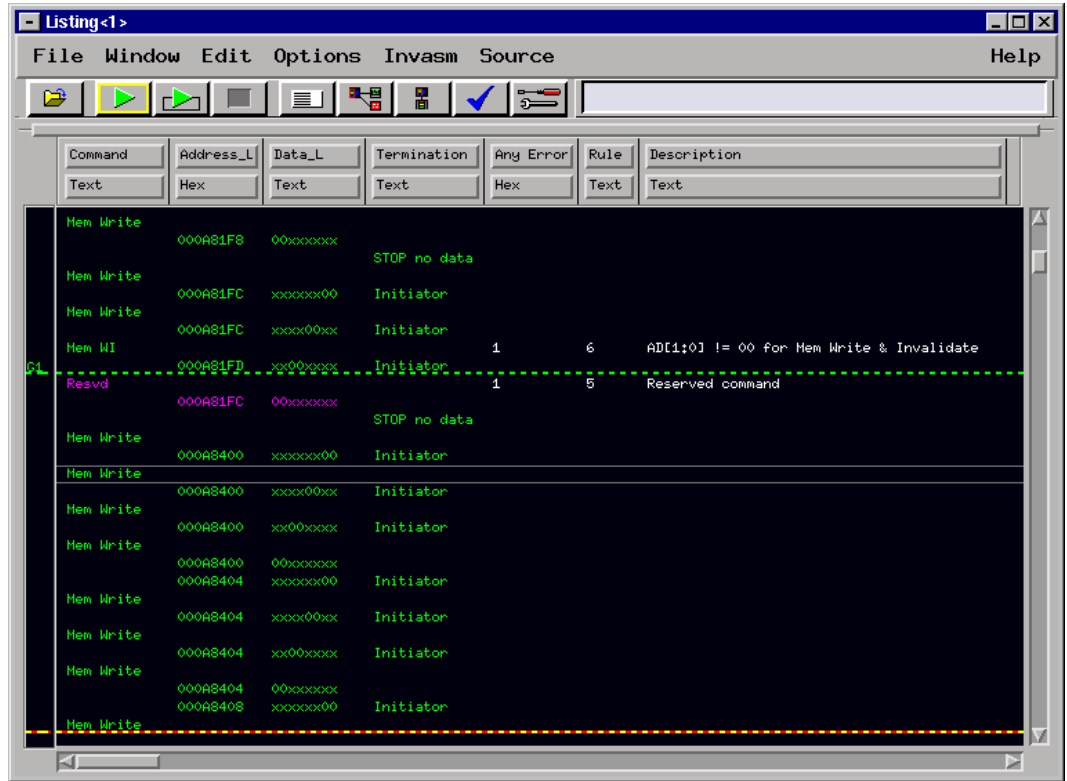
Configure the trigger menu to acquire PCI data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you select STOP.

The logic analyzer will flash "Slow or Missing Clock" if it does not see the PCI signal CLK toggling.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

# The State Listing Display

Captured data is as shown in the following figure.



The following is a list of the generated columns from the FS1105 PCI Compliance Consultant tool.

<b>Name</b>	<b>Base</b>	<b>Description</b>
Command	TEXT	The command name
Address_H	HEX	The address as it appears during a 64 bit address transfer (as defined by a DAC)
Address_L	HEX	The address as it appears on the lower AD lines (AD[31:0]). This HEX value is incremented during burst transactions
Data_L	HEX	The lower 32 bit AD lines representing data
Data_H	HEX	The upper 32 bit AD lines representing data
Byte_Enable_H	HEX	High order data byte enables
Byte_Enable	HEX	Low order data byte enables
Termination	TEXT	Termination type
TERM CODE	HEX	Termination type displayed in HEX (for use in SPA and filter tools)
CMD	HEX	The command type displayed in HEX (for use in SPA and filter tools)
Clocks	Decimal	The number of clock tics that have elapsed. This takes into consideration those states filtered out by the Trigger menu store qualification
Num Byte Enables	Decimal	Number of byte enables asserted for that data transfer
Rule	Text	The rule number corresponding to the violation seen
Description	Text	A description of the violation found
Any Error	HEX	Can be used by the search function in the lister to quickly locate an error.

## Compliance Violations

The following is a list of the compliance rules checked by the FS1105 PCI Compliance Consultant tool.

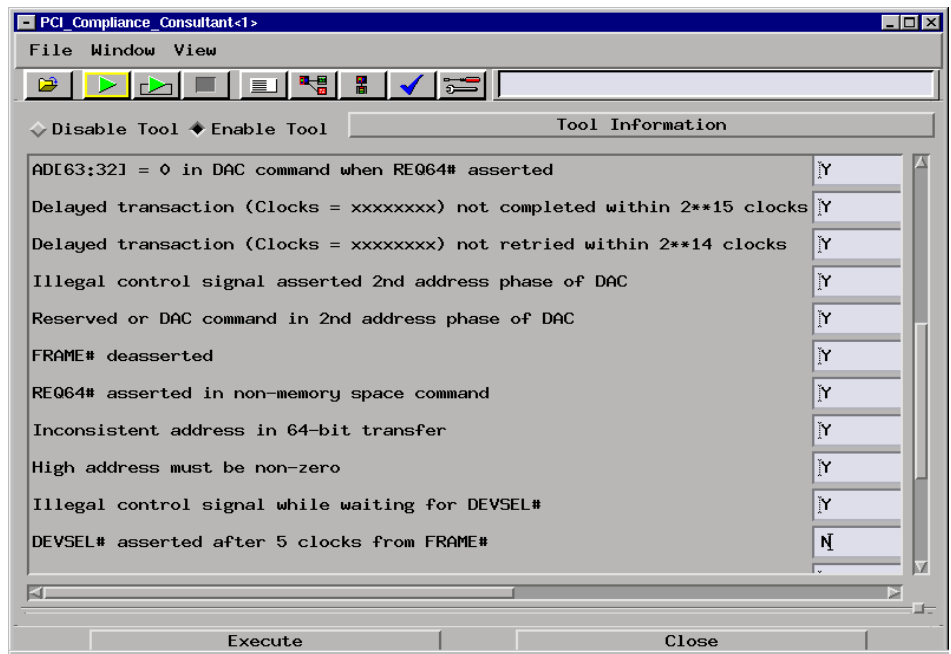
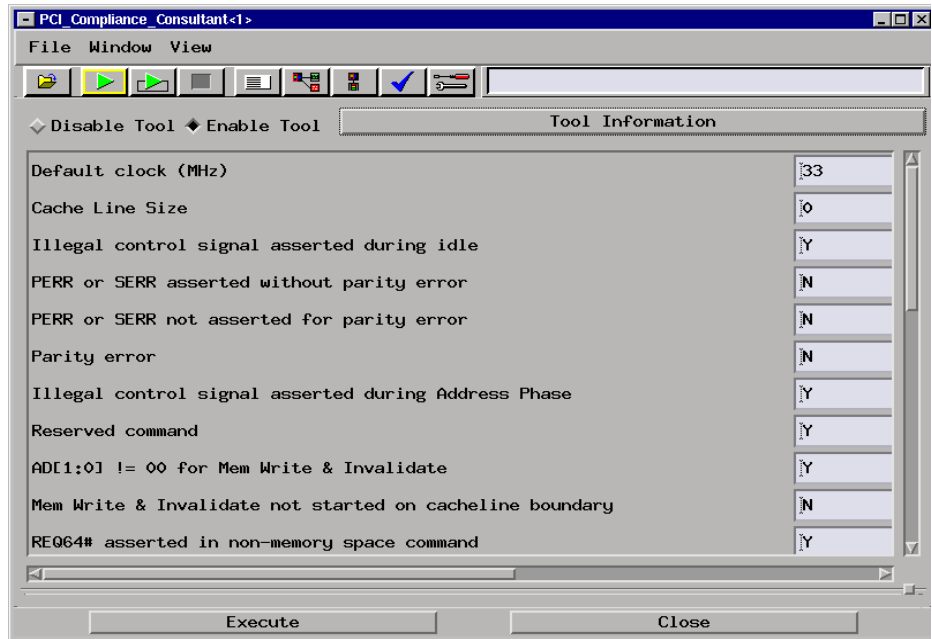
Name	Rule number	Description
Illegal control signal asserted during IDLE	1	Section 3.2.1 Basic Transfer Control
Parity error	2	Appendix C Rule 32b and c
PERR# or SERR# not asserted for parity error	3	Section 3.7.4.1 Data Parity Error Signaling
Illegal control signal asserted during Address Phase	4	Section 3.2.1 Basic Transfer Control
Reserved Command	5	Section 3.1.1 Command Definition
AD[1:0] !=00 for Mem Write and Memory Write Invalidate	6	The FS1105 checks for linear incrementing Section 3.2.2.2 Memory Space Decoding
Mem Write and Invalidate not started on cacheline boundary	7	The FS1105 checks for cache aligned accesses per the input given by the user. Section 3.2.2.2 Memory Space Decoding
REQ64# asserted w/o DAC in non-memory space command	8	Section 3.8. 64 bit bus extensions
AD[63:32]=0 in DAC command when REQ64# asserted	9	Section 3.10.1 64 bit Addressing on PCI
PERR# or SERR# asserted without a parity error	10	Section 3.7.4.1 Data Parity Error signaling on PERR#
Illegal control signal asserted 2 <sup>nd</sup> address phase of DAC	12	Section 3.9 64 bit addressing on PCI
Reserved or DAC command in the 2 <sup>nd</sup> address phase of a DAC	13	Section 3.9 64 bit addressing on PCI

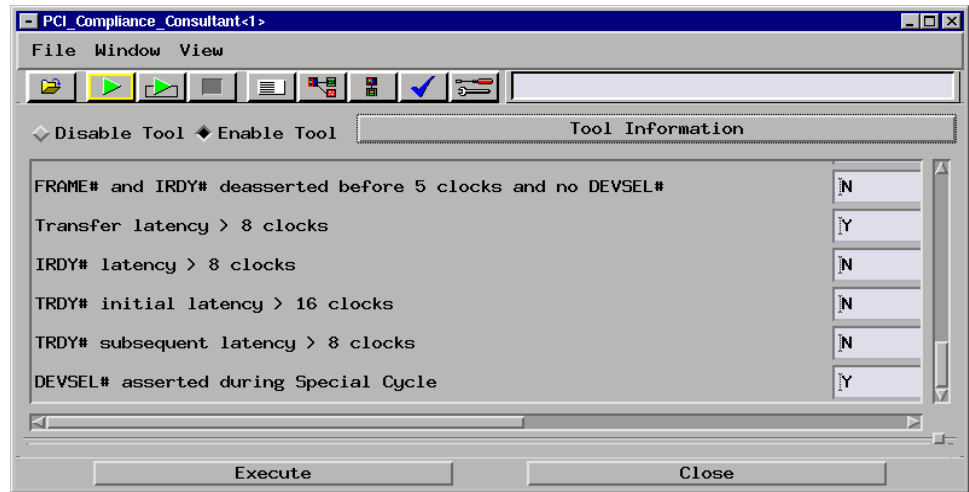
FRAME# deasserted illegally.	14	FRAME# cannot be deasserted unless IRDY# is asserted. Appendix C rule 8c
REQ64# asserted w/ DAC in non-memory space command	15	Section 3.9 64-bit Bus Extensions
Inconsistent address in 64-bit transfer	16	"Inconsistent address" means that AD[63:32] does not equal AD[31:0] in the first address phase. 3.9 64 bit addressing on PCI
High address must be non-zero	17	In a DAC the upper address must be non zero. 3.9 64-bit addressing on PCI
Illegal control signal while waiting for DEVSEL#	19	Appendix C Rule 14 and 29
DEVSEL# asserted during a special cycle	20	Section 3.6.2 Special Cycle
DEVSEL# asserted after 5 clocks from FRAME#	21	Section 3.3.3.1 Master Initiated Termination
FRAME# and IRDY# deasserted before 5 clocks and no DEVSEL#	22	Section 3.3.3.1 Master Initiated Termination
Transfer latency > 8 clocks	23	Appendix C Rule 25 Waits states are filtered
IRDY# latency > 8 clocks	24	Appendix C Rule 27
TRDY# initial latency > 16 clocks	25	Appendix C Rule 25
TRDY# subsequent latency > 8 clocks	34	Appendix C Rule 26
Delayed transaction (Clocks = xxxxxxxx) not retried within 2**14 clocks	38	Agilent Rule to detect potential deadlocks
Delayed transaction (Clocks = xxxxxxxx) not completed within 2**15 clocks	39	Agilent Rule to detect potential deadlocks

## Masking Protocol Errors

The FS1105 contains a mask menu that allows the user to turn off or mask protocol violations that the user does not want the software to flag as errors. This menu can be invoked by placing the cursor on the tool and using the right mouse button to select DISPLAY. Once the desired masking has been selected the user must hit EXECUTE for the tool to run using the updated selections.

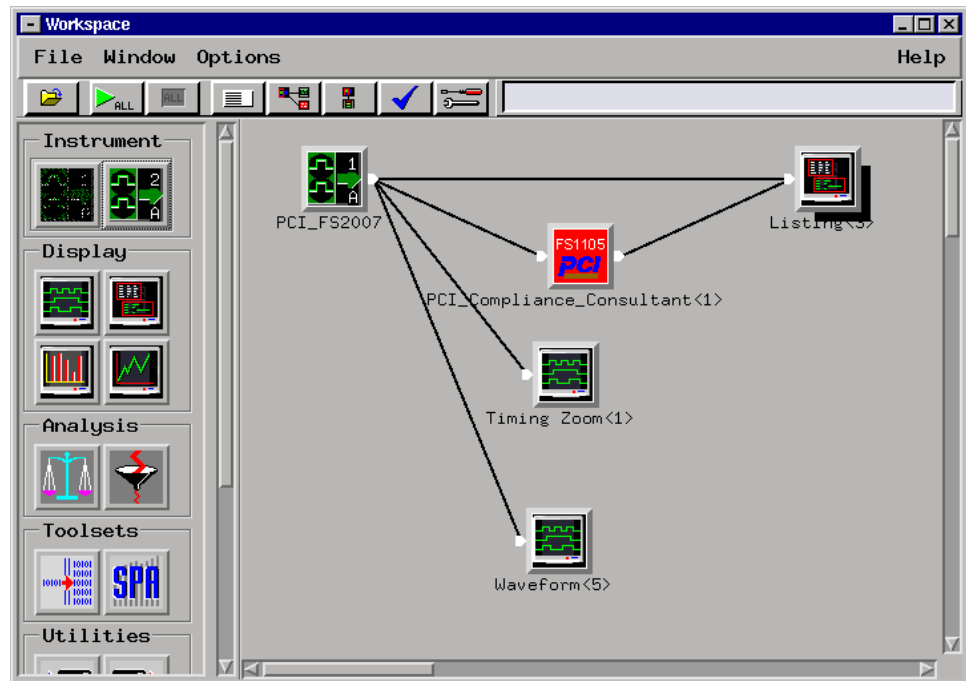
The default masking is shown in the screen shots below.





## The PCI Bus signals in the Lister Display

The FS1105 software removes the raw PCI bus signals from the output display for easy reading. However these signals are important and can quickly be added back into the display by connecting the logic analyzer icon directly to the lister. Once this is done the output of the FS1105 software will appear alongside the acquired PCI bus signals.



## Using the Filter tool

Since the PCI Compliance Consultant tool creates unique columns in the listing window these columns and their contents may be used by the filter tool.

## **Using the System Performance tool**

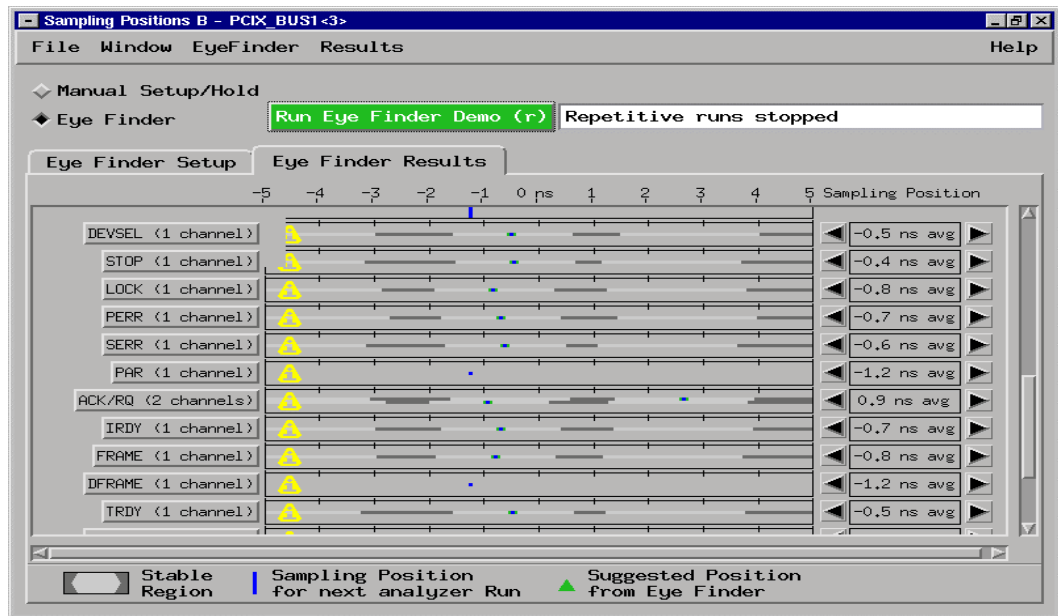
The System Performance Analysis tool or SPA can be used to create histogram displays of various PCI metrics. The hex based labels created by the FS1105 software were specifically created for use with the SPA tool.

## **Transactor Software Decode Time**

The current architecture of the 16700 is such that the entire buffer of captured data is decoded all at once. This leads to a long decode time prior to seeing the data decoded in the listing window. Future revisions of the 16700 operating system and a re-write of the FS1105 software will solve this problem. The anticipated date for this revision will be Q4 2001. All customers will receive free updates. In the interim it is suggested that the acquisition buffer size of the logic analyzer be set to below 64K.

## Use of Eye Finder

Use of Eye Finder can greatly enhance your analysis by helping find the data valid window of every signal on the bus with respect to the clock. You can compare the results of Eye Finder to your simulation and the PCI specification to see if your system operates within expected setup and hold margins. Eye Finder can be found in the setup and hold area of your logic analysis card FORMAT menu.



# Timing Analysis

## Timing Mode and the FS1105 software

Since the passive FuturePlus PCI analysis probes do not buffer the PCI bus they introduce negligible skew to the PCI Local Bus signals.

The FS1105 software should be disabled when the logic analyzer is configured in timing mode. This is because the FS1105 can only operate on state acquired data.

## Installation Quick Reference

The following procedure describes the major steps required to perform timing analysis measurements on the passively probed PCI target.

1. After removing the probe tip assemblies, plug the logic analyzer PODs into the analysis probe cable headers.
2. Load the logic analyzer configuration file from the logic/configs/FuturePlus/FS1105 directory.
3. Configure the logic analyzer for TIMING mode.
4. **DELETE the FS1105 ICON from the workspace OR open the tool and select DISABLE.**

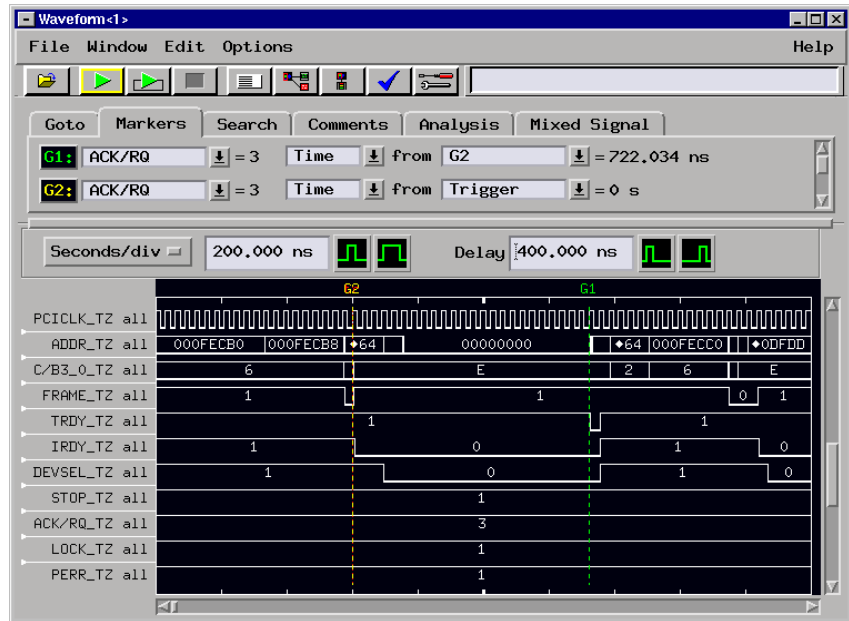
## Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE, or when you touch STOP.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

## The Waveform Display

Captured data is displayed as shown in the following figure.



## Timing Zoom

Most of the analyzers in the 16715 family or above come with Timing Zoom. Timing zoom is especially useful for passively probed busses because it gives the user simultaneous state and timing. The timing zoom acquired signals are indicated by an \_TZ appended onto the signal name. For more information of on Timing Zoom please refer to your Agilent logic analyzer documentation.