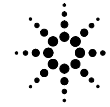


FuturePlus® Systems Corporation



Agilent Technologies
Innovating the HP Way

Premier Solution Partner



FS1104 Users Manual

For use with Agilent Logic Analyzers

Revision – 2.0

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Introduction

How to Use This Manual

The FS1104 decoder will decode the PCIX bus traffic in an easy to read format and provide additional performance information.

This manual is organized to help you quickly find the information you need.

- The **Getting Ready** chapter discusses the minimum equipment required to use the FS1104 product.
- **Probing Your Embedded PCI-X Target** describes how to probe your embedded PCI-X target using the AMP MICTOR-38 connectors for compatibility with the FS1104 software product.
- The **State Analysis** chapter explains how to configure the logic analyzer and FS1104 software for state analysis.
- The **Timing Analysis** chapter explains how to configure the logic analyzer for timing analysis.

Getting Ready

This chapter discusses the minimum equipment required to use the FS1104 product.

Accessories Supplied

The FS1104 product consists of the following accessories:

- One diskette containing the configuration file and FS1104 decoder software.
- This operating manual on CD.

Minimum Equipment Required

The minimum equipment required for analysis of a PCI - X Local Bus using the FS1104 product consists of the following equipment:

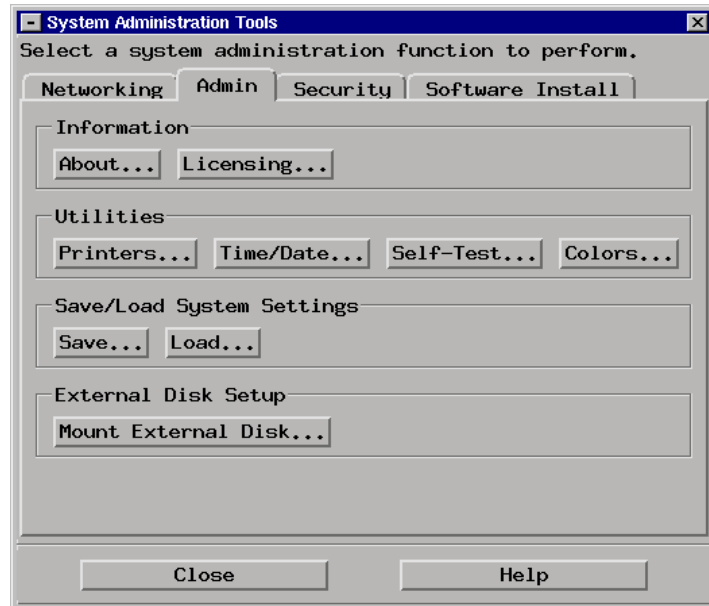
- Agilent 1670x analysis frame with the 16715 analyzer card or better.
- Revision 2.0 or better of the Agilent Logic analysis frame software.
- The FS1104 Product
- A probed PCI-X target bus

Licensing

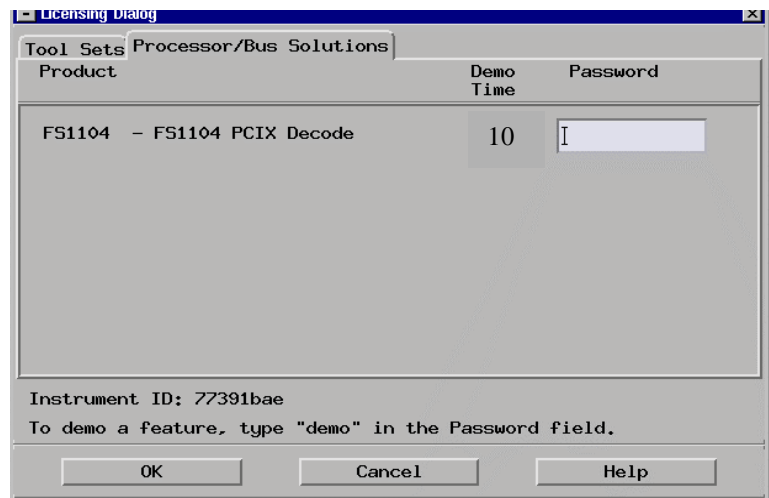
The FS1104 product is a licensed product which is locked to a single Agilent 1670x frame. A demo time is provided by typing the word *demo* into the licensing area next to the product name. The licensing area for the 1670x mainframe is found under System Administration. For use of the FS1104 product beyond the demo time please contact FuturePlus Systems at www.futureplus.com or 719-278-3540.

Licensing Area

The following shows the ADMIN tab under System Administration Tools.



Once the FS1104 product is installed the password may be entered in the area shown below.



Signal Naming Conventions

This operating manual uses the same signal notation as the PCI -X LOCAL BUS SPECIFICATION - REVISION 1.0 That is, a # symbol at the end of a signal name indicates that the signal's active state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is active at a high voltage.

Probing your Embedded PCI-X Target

What you will need to Analyze PCI-X

This chapter describes the probing method for the AMP Mictor-38 pin connector to a 32/64 bit PCI-X local bus. Following this method will allow the user to use the Agilent E5346A or E5351A High-Density Termination Adapter Cables and the FuturePlus Systems PCI-X software FS1104 for PCI-X analysis with an Agilent logic analyzer.

64 bit PCI-X

- 3 AMP MICTOR-38 (part number 2-767004-2) surface mount connectors mounted on the target board and routed to the PCI-X Local bus
- 3 Agilent E5346A or E5351A High-Density Adapter Cables available from FuturePlus Systems or Agilent Technologies
- 6 logic analyzer PODS
- FS1104 Software from FuturePlus Systems

32 bit PCI-X

- 2 AMP MICTOR-38 (part number 2-767004-2) surface mount connectors mounted on the target board and routed to the PCI-X Local bus
- 2 Agilent E5346A or E5351A High-Density Adapter Cables from FuturePlus Systems or Agilent Technologies
- 4 logic analyzer PODS
- FS1104 Software from FuturePlus Systems

The Mictor-38 connectors will be referred to as #1, #2 and #3 (#3 for 64 bit only). Each Mictor-38 connector connects two logic analyzer PODS, an EVEN numbered POD and an ODD numbered POD. Pins 1,2 and 4 on the Mictor-38 connectors are no connects. Pin 3 and pins 39-43 should be connected to GROUND.

PCI-X setup and hold time

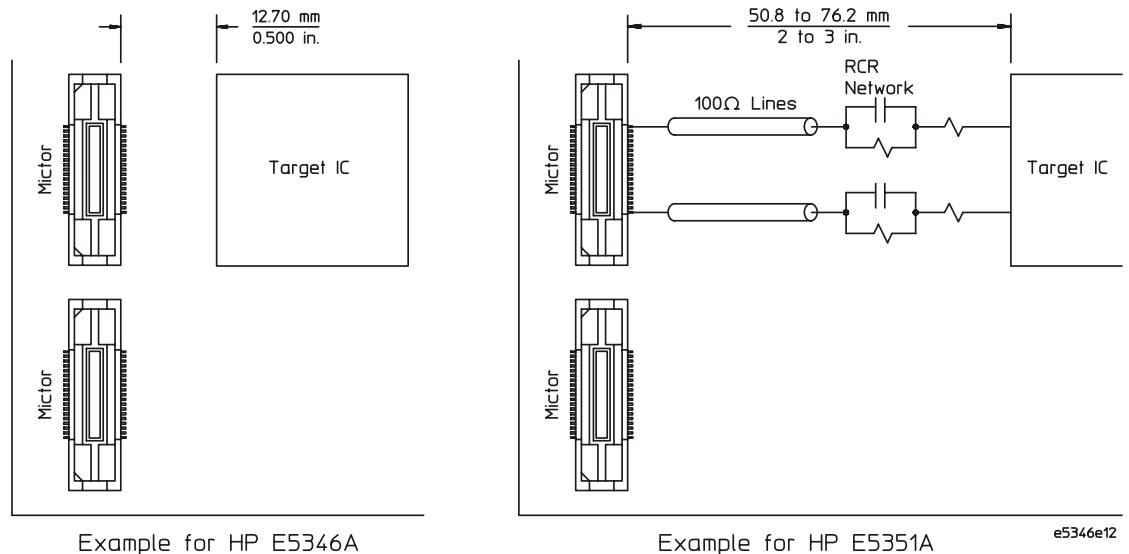
The PCI-X specification allows for a worse case setup/hold time of :

- 100/133Mhz – 1.2/0.5 total window=1.7ns
- 66Mhz – 1.7/0.5 total window=2.2ns

The total setup/hold window of the current generation of logic analyzer cards is 2.5 ns. For systems that demonstrate worse case setup/hold or setup/hold less than 2.5 ns, Eye Finder can be used to adjust individual bit setup/hold so that the overall setup and hold can be as low as 1.25 ns.

Where to place the MICTOR connectors on the target

The recommended placement of the MICTOR-38 connectors is at either end of the bus segment. To connect to the bus segment the mictors should be placed at the end of as short a stub as possible. If there is not enough room to place the mictors such that the stub is less than or equal to **0.5 inches** from the bus segment then an alternate method may be used. That is, to place the logic analyzer termination circuitry on the target and then extend the etch from the end of the termination circuitry over to the MICTOR-38 connectors. The connection from the mictors to the logic analyzer must then be done with the **E5351A**. The E5346A contains the logic analyzer termination circuitry, the E5351A does not.



The Termination Network

The termination network consists of a 249 ohm resistor in series with the parallel combination of a 90K ohm resistor and a 8.2pF capacitor. The components are placed as shown in the drawing above. If the etch from the network to the connector is less than one inch, the impedance of the etch can be in the 60-75 ohm range. If it is longer, it should be controlled at 100 ohms.

If the termination network is placed on the target then the stub should be 0.5" or less. In general, the stub must be << 50% of the wavelength of the rise time of the signal for it to be treated as a lumped C rather than a transmission line.

When the network is on the board before the mictor, the impedance of that trace should be as high as possible, ideally 120 ohm (the cable impedance). Since it is really hard to get impedances that high, 100 ohm is recommended as a practical maximum. If you can get to 120 ohm then the trace can be made as long as you like. However, just as with the E5346A/E5351A cables, the parasitic C will cause the divider ratio to fall below 10:1, and this will be more pronounced the longer the trace. About a foot at 120 ohm is a practical maximum before the thresholds set in the FORMAT menu needs to be adjusted.

PCI-X Signal Assignment

FuturePlus Systems will supply a configuration file with the FS1104 product that matches the following pinout. However it should be noted that the pinout could be re-pinned by the user in order to match etch lengths and control skew.

LOGIC ANALYZER POD 1

Mictor-38 #1 Pin Number ODD POD	Logic Analyzer channel number	PCI-X Signal name
6	CLK/16	CLK
8	15	C/BE4
10	14	C/BE6
12	13	C/BE5
14	12	C/BE7
16	11	ACK64
18	10	REQ64
20	9	UNUSED*
22	8	PME
24	7	C/BE0
26	6	M66EN
28	5	C/BE1
30	4	SERR
32	3	PAR
34	2	PERR
36	1	LOCK
38	0	STOP

LOGIC ANALYZER POD 2

Mictor-38 #1 Pin Number EVEN POD	Logic Analyzer channel number	PCI-X Signal name
5	CLK/16	FRAME
7	15	DEVSEL
9	14	TRDY
11	13	C/BE2
13	12	C/BE3
15	11	IDSEL
17	10	REQ
19	9	GNT
21	8	RST
23	7	INTD
25	6	INTC
27	5	INTB
29	4	INTA
31	3	UNUSED*
33	2	UNUSED*
35	1	UNUSED*
37	0	UNUSED*

*These pins are unused and can be connected to any signal and assigned by the user in the Format menu.

LOGIC ANALYZER POD 3

Mictor-38 #2 Pin Number ODD POD	Logic Analyzer channel number	PCI-X Signal name
6	CLK/16	IRDY#
8	15	AD15
10	14	AD14
12	13	AD13
14	12	AD12
16	11	AD11
18	10	AD10
20	9	AD09
22	8	AD08
24	7	AD07
26	6	AD06
28	5	AD05
30	4	AD04
32	3	AD03
34	2	AD02
36	1	AD01
38	0	AD00

LOGIC ANALYZER POD 4

Mictor-38 #2 Pin Number EVEN POD	Logic Analyzer channel number	PCI-X Signal name
5	CLK/16	UNUSED*
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

***This pin is unused and can be connected to any signal and assigned by the user in the Format menu.**

LOGIC ANALYZER POD 5

Mictor-38 #3 Pin Number ODD POD	Logic Analyzer channel number	PCI-X Signal name
6	CLK/16	PAR64
8	15	AD47
10	14	AD46
12	13	AD45
14	12	AD44
16	11	AD43
18	10	AD42
20	9	AD41
22	8	AD40
24	7	AD39
26	6	AD38
28	5	AD37
30	4	AD36
32	3	AD35
34	2	AD34
36	1	AD33
38	0	AD32

LOGIC ANALYZER POD 6

Mictor-38 #3 Pin Number EVEN POD	Logic Analyzer channel number	PCI-X Signal name
5	CLK/16	UNUSED*
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48

***This pin is unused and can be connected to any signal and assigned by the user in the Format menu.**

Routing and Re-pinning Information

In order to control skew all etch lengths should be near equal. If it makes sense from a layout point of view, the signals may be re-pinned on the MICTOR-38 connectors. The user would then only need to modify the included configuration file to match the actual layout. The following restrictions apply.

- The clock cannot be re-pinned to a signal pin
- Bit re-ordering can be used to put the command/AD signals back in order. If the AD signals are RE-ORDERED then the user will not be able to use the IN RANGE feature in the triggering menu for address range triggering.
- The CYCLE variable will need to be bit re-ordered to match the supplied symbols in the configuration file. (This is not a difficult task).

GNT#, REQ# and IDSEL signals

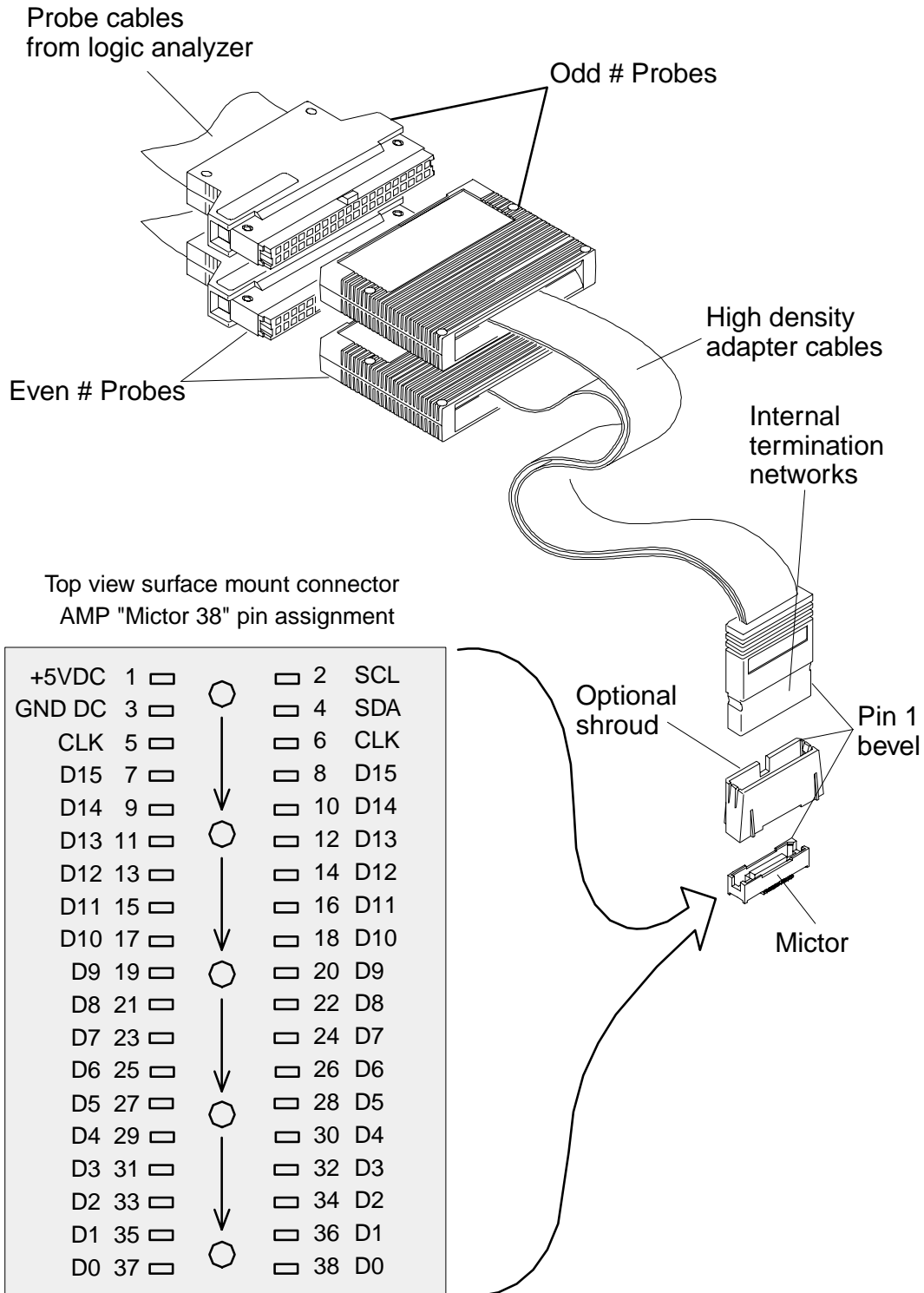
This pinout contains the signals GNT#, REQ# and IDSEL# for whatever PCI-X device the user connects. Since these are radially routed signals it is recommended that the remaining target system GNT# lines and optionally the REQ# and IDSEL signals be connected to the unused pins. This may make debugging and performance analysis easier.

Assigning additional signals

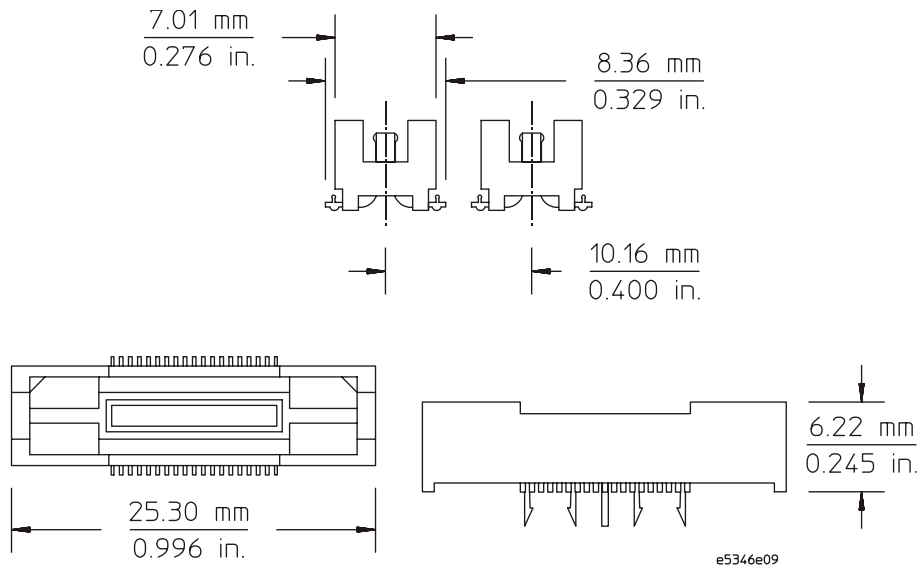
Any additional signals can be added to any unused pins in the configuration file and displayed along side the FS1104 generated labels in the state listing screen.

Agilent E5346A/E5351A

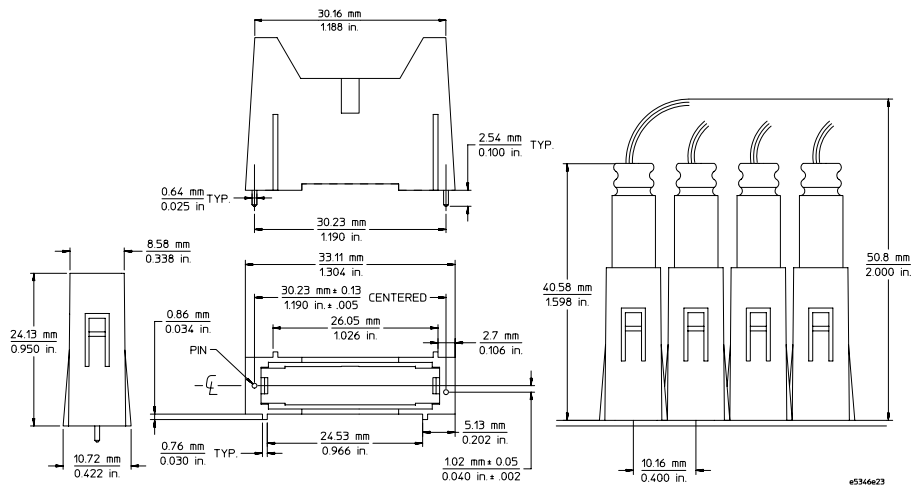
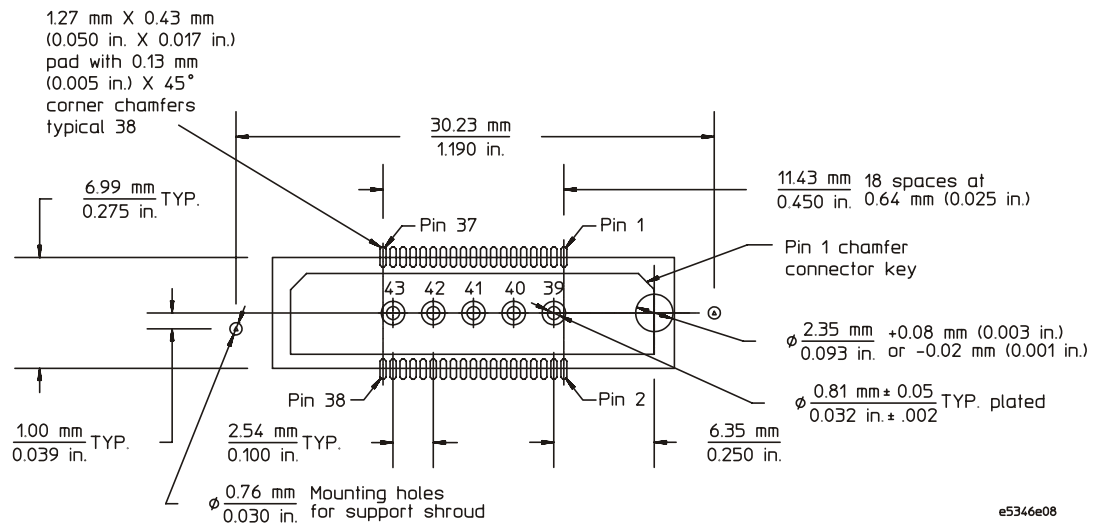
The connection from the target MICTOR-38 connectors to the Agilent logic analyzer is made using either the E5346A or the E5351A .



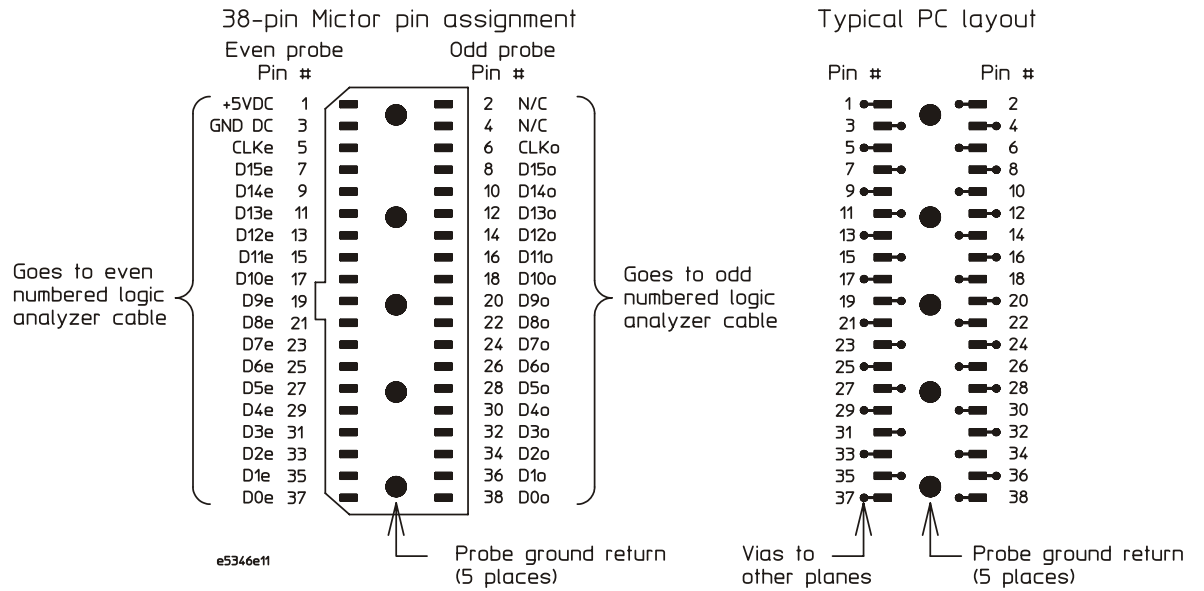
MICTOR-38 Connector Mechanical Dimensions



Shroud Mechanical Information



MICTOR-38 Layout Footprint



State Analysis

This chapter explains how to configure the Agilent logic analyzer and FS1104 software to perform state analysis on the PCI-X Local Bus. The next chapter explains how to configure the FS1104 to perform timing analysis.

Connecting the Agilent logic analyzer to the target PCI-X bus

The following explains how to connect the logic analyzer to the target PCI-X bus for either state or timing analysis:

1. Remove the probe tip assemblies from the logic analyzer cables.
2. Install the E5346A or the E5351A high density termination adapters into the target MICTOR-38 connectors.
3. Plug the logic analyzer PODs into the target cable headers as shown in the following table.

Logic Analyzer	PCI-X Target Probe	Comment
Master POD 1	Header 1	J CLK
Master POD 2	Header 2	
Master POD 3	Header 3	
Master POD 4	Header 4	
Expander POD 1	Header 1	optional 64 bit
Expander POD 2	Header 2	optional 64 bit

Setting up the Software on the Analyzer

The FS1104 software consists of one diskette.

- The FS1104 PCI-X Decode diskette

To install the FS1104 PCI-X transactor software insert the diskette labeled 16700/702 Installation disk for the **FS1104 PCI-X Software** into the Agilent 16700 diskette drive. From the SYSTEM ADMINISTRATION TOOLS select *INSTALL* under *SOFTWARE*. From the SOFTWARE INSTALL screen select the *FLEXIBLE DISK* and *APPLY*. Once the title appears select it and then select *INSTALL*.

This procedure does not need to be repeated. It only needs to be done the first time the FS1104 product is used.

When this has completed load the appropriate configuration file from the /configs/FuturePlus/FS1104 directory. Refer to the below table for a list of analyzers and corresponding configuration files.

The only analyzers supported by the FS1104 configuration files are the 16715 or better.

Logic Analyzer	File name for State/Timing Analysis	Description
16715/6/7/9, 1674X 16750/1/2	CP1104_1	32/64 bit analysis

The CP1104_1 configuration file requires two logic analyzer cards melded for 64 bit analysis. For 32 bit analysis only one logic analyzer card is required. When loading the CP1104_1 file into a one card configuration a yellow warning message will appear that notes that the two extra pods are not being loaded. This message will not effect proper operation and is merely for notification purposes.

The PCI-X Transaction Decode Software

Loading the configuration file will automatically load the inverse assembler. If this does not happen then check to make sure that the PCI-X transaction decode software was properly installed and licensed.

State Number	PCI-X 1.0									
Decimal	CMD	Wait	Addr_High	Addr_Low	Attribute	Data High	Data Low	Termination	CBE7_0	CBE3_0
5										
6	Mem Rd Blk		05020080						0000	0000
7					Requester					
					Bus: 97					
					Dev: 1					
					Fun: 0					
					Tag: 1					
					Count: 16					
8		Wait-No	DevSel							
9		Wait-No	DevSel							
10		Wait-No	TRDY							
11		Wait-No	TRDY							
12		Wait-No	TRDY							
13		Wait-No	TRDY							
14								Split Resp		
15										
16	Split Complete			Mem Rd Blk	Requester					
					Bus: 97					
					Dev: 1					
					Fun: 0					
					Tag: 1					
					Low Addr					

***Transactor Software
Decode Time***

This version of the FS1104 software does not have limitation that the previous releases had. Any buffer size can be used with this version without experiencing the long decode time of previous versions.

***Timing Mode and the
FS1104 Transactor
Decode software***

The FS1104 Transactor Decode software should NOT be run when the logic analyzer is configured in timing mode. This will cause the system to hang.

***The ADDR, ADDR_B
variables***

The ADDR variable in the FORMAT menu is assigned to the AD[31:0] signals on the PCI-X bus. The ADDR_B is the AD[63:32] signals on the PCI-X bus.

The CYCLE variable

The CYCLE variable is made up of the following signals: TRDY#, FRAME#, IRDY#, C/BE(3,0), DEVSEL#, STOP#. This variable has 30 symbols defined that can be used to help make triggering, timing analysis and pattern filtering easier. The following lists the bit pattern and the corresponding symbol.

Symbol	IRDY#	FRAME#	DEVSEL#	TRDY#	C/BE(3:0)	STOP#
INTACK	1	0	1	1	0000	1
SPECIAL CYCLE	1	0	1	1	0001	1
I/O READ	1	0	1	1	0010	1
I/O WRITE	1	0	1	1	0011	1
RESERVED	1	0	1	1	0100	1
RESERVED1	1	0	1	1	0101	1
MEM RD DWORD	1	0	1	1	0110	1
MEM WRITE	1	0	1	1	0111	1
MEM RD BL	1	0	1	1	1000	1
MEM WR BL	1	0	1	1	1001	1
CONF READ	1	0	1	1	1010	1
CONF WRITE	1	0	1	1	1011	1
SPLIT_COMPLETION	1	0	1	1	1100	1
DAC	1	0	1	1	1101	1
MEM RD BLOCK	1	0	1	1	1110	1
MEM WR BLOCK	1	0	1	1	1111	1
IO XACTION	1	0	1	1	001X	1
MEM XACTION	1	0	1	1	011X	1
CONFIG XACTION	1	0	1	1	101X	1
ADDR CYCLE	1	0	1	1	XXXX	1
DATA XFER	0	X	0	0	XXXX	1
INITIATOR TERM	0	0	1	1	XXXX	1
SINGLE DATA XFER	0	X	1	0	XXXX	0
STOP NXT ADB	0	X	0	0	XXXX	0
RETRY	0	X	0	1	XXXX	0
TARGET ABORT	1	X	1	1	XXXX	0

Symbol	IRDY#	FRAME#	DEVSEL#	TRDY#	C/BE(3:0)	STOP#
IDLE	1	1	X	X	XXXX	X
SINGLE DATA DISCON	0	0	1	0	XXXX	0
TARGET RESPONSE	0	0	0	1	XXXX	1
SPLIT RESPONSE	0	0	1	0	XXXX	1

Bit Re-ordering

The included configuration file CP1104_1 has the following labels that have been re-ordered. The bit re-ordering function can be found in the FORMAT menu. If the sample pinout is not used then the re-ordering will need to be modified to reflect the shown ordering in order for the supplied configuration symbols to be correct.

Below is a list of signals and the corresponding bit re-ordering.

The Cycle Variable

Probe Channel	Map to bit
0	0
1	2
2	1
3	4
4	3
5	5
6	6
7	7
8	8

C/BE3:0

Probe Channel	Map to bit
0	1
1	0
2	3
3	2

C/BE7:4

Probe Channel	Map to bit
0	3
1	1
2	2
3	0

Acquiring Data

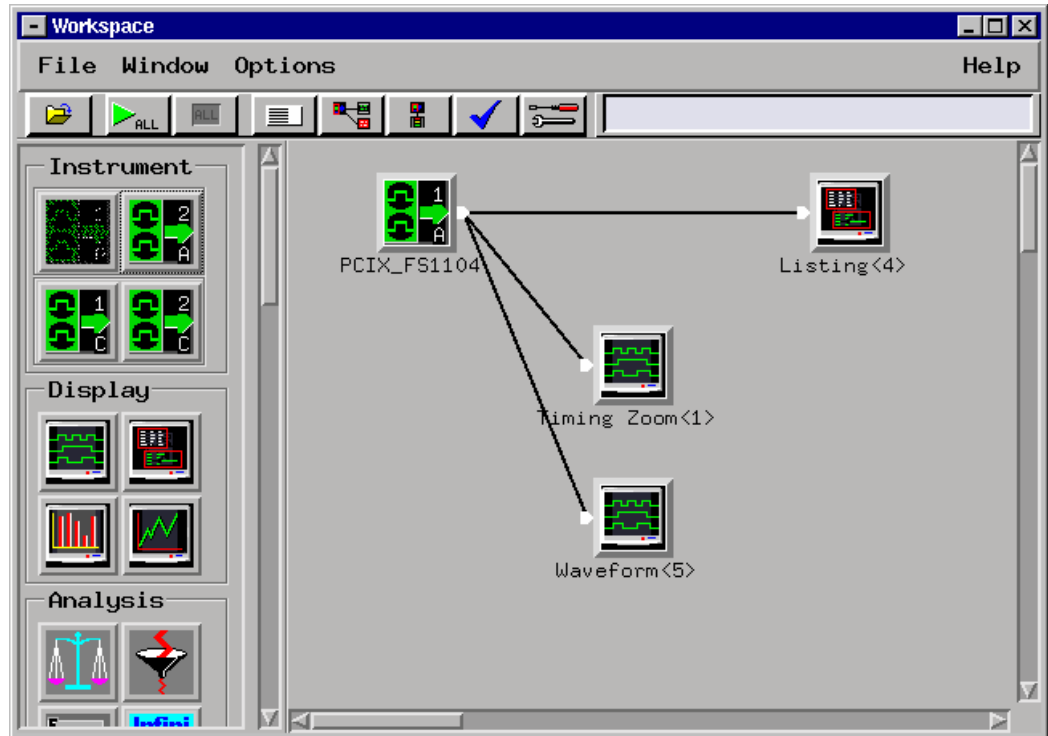
Configure the trigger menu to acquire PCI-X data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you select STOP.

The logic analyzer will flash "Slow or Missing Clock" if it does not see the PCI-X signal CLK toggling.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

Configuring the Workspace for PCI-X Analysis

For full analysis, the PCI-X workspace should appear as below. Filter tool icons, System Performance icons and others can be copied several times over onto the workspace.



The State Listing Display

Captured data is as shown in the following figure. The below figure displays the PCI-X transactor decode.

State Number	PCI-X 1.0									
Decimal	CMD	Wait	Addr_High	Addr_Low	Attribute	Data_High	Data_Low	Termination	CBE7_0	CBE3_0
5										
6	Mem Rd Blk			05020080						
7					Requester				0000	0000
					Bus: 97					
					Dev: 1					
					Fun: 0					
					Tag: 1					
					Count: 16					
8		Wait-No	DevSel							
9		Wait-No	DevSel							
10		Wait-No	TRDY							
11		Wait-No	TRDY							
12		Wait-No	TRDY							
13		Wait-No	TRDY							
14									Split Resp	
15										
16	Split Complete				Mem Rd Blk					
					Requester					
					Bus: 97					
					Dev: 1					
					Fun: 0					
					Tag: 1					
					Low Addr					

The FS1104 creates one output label that is sub-divided into several sub-columns. They are:

Name	Base	Description
CMD	HEX	The command type displayed in HEX (for use in SPA and filter tools)
ADDR_H	TEXT	The address as it appears during a 64 bit address transfer (as defined by a DAC)
ADDR_L	HEX	The address as it appears on the lower AD lines (AD[31:0]). This HEX value is incremented during burst transactions
Data_L	TEXT	The lower 32 bit AD lines representing data
Data_H	TEXT	The upper 32 bit AD lines representing data
BE_L	HEX	Data byte enables for the lower 32 bit AD lines (AD[31:0]).
BE_H	HEX	Data byte enables for the upper 32 bit AD lines (AD[63:32]).
Termination	TEXT	Termination type

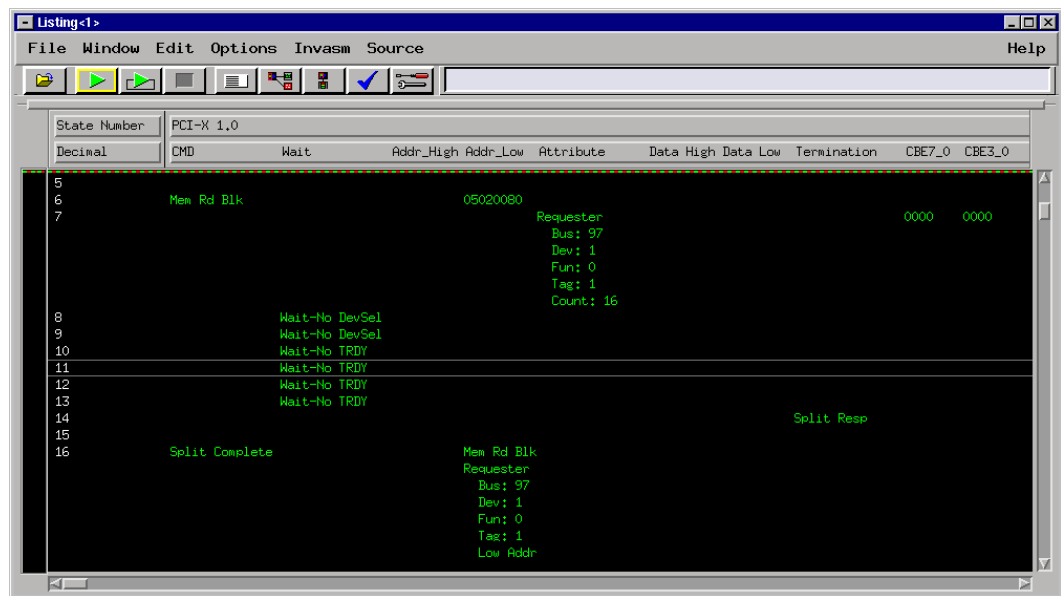
Functionality of the FS1104 Transaction Decode Software

The FS1104 Decode Software will perform the following functions:

- ◆ Decode all PCI-X command and cycle types
- ◆ Decode Attribute and Split Address fields for easy reading
- ◆ Color code the data and attribute to match the transaction type (command). The colors used by the software are as follows:
 - ◆ Memory and Split Completion transactions: Green
 - ◆ I/O transactions: Yellow
 - ◆ Configuration transactions: Blue
 - ◆ Interrupt Acknowledge, Special Cycle transactions and the DAC cycle: Purple
 - ◆ Idle and Wait cycles: White
- ◆ Match the Request to the Response by printing the corresponding address aligned with the data on a Split Response. In addition the original command will be printed with the Split Response to indicate which command was originally requested.

The PCI-X Bus signals in the Lister Display

The output of the FS1104 Transaction Decode software will appear alongside the acquired PCI-X bus signals.



Using the Filter tool

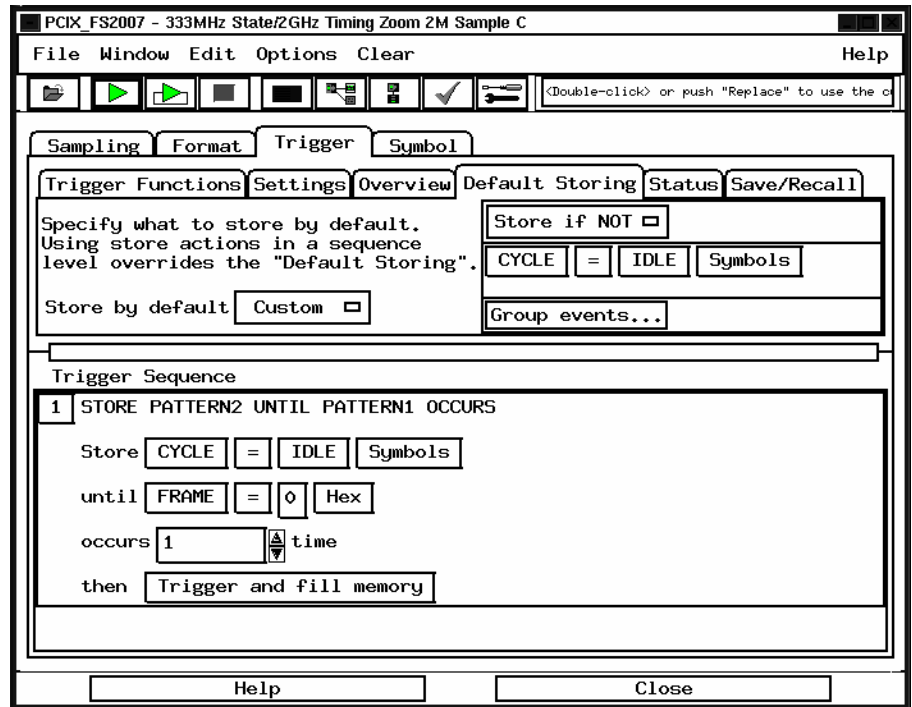
Since the PCI-X transactor tool creates only one unique column in the listing window, this column and its contents may not be used by the filter tool.

Using the System Performance tool

The System Performance Analysis tool or SPA can be used to create histogram displays of various PCI-X metrics.

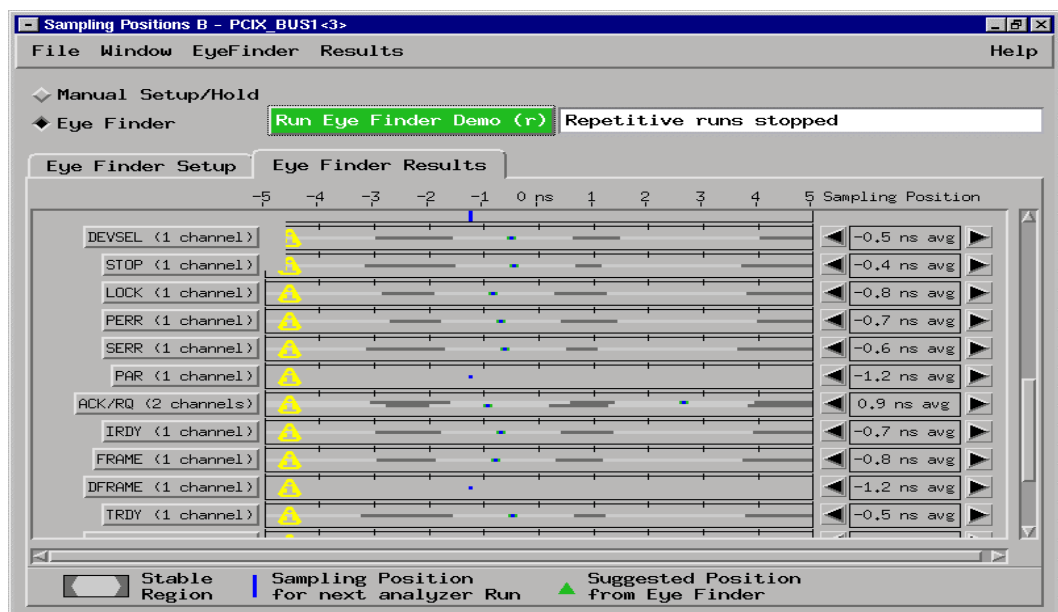
The Default Trigger

The FS1104 configuration file sets up a simple default trigger with a store qualification that filters out most of the IDLE states. For software synchronization an IDLE state is acquired between transactions.



Use of Eye Finder

Use of Eye Finder can greatly enhance your analysis by helping find the data valid window of every signal on the bus with respect to the clock. You can compare the results of Eye Finder to your simulation and the PCI-X specification to see if your system operates within expected setup and hold margins. Eye Finder can be found in the setup and hold area of your logic analysis card FORMAT menu.



Timing Analysis

Installation Quick Reference

Since the MICTOR-38 interface does not buffer the PCI-X bus it introduces negligible skew to the PCI-X Local Bus signals.

The following procedure describes the major steps required to perform timing analysis measurements of your probed PCI-X target.

1. After removing the probe tip assemblies, plug the logic analyzer PODs into the E5346A cable headers
2. Install the E5346A or the E5351A high density termination adapters into the target MICTOR-38 connectors.
3. Load the logic analyzer configuration file CP1104_1 from the logic/configs/FuturePlus/FS1104 directory.
4. Configure the logic analyzer for TIMING mode.

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

The Waveform Display

Captured data is displayed as shown in the following figure.

