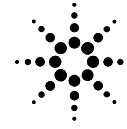


FuturePlus Systems Corporation



Agilent Technologies
Innovating the HP Way

Premier Solution Partner



FS1103 or FS1110 Manual
32/64 bit PCI Pinout

For use with Agilent Technologies Logic Analyzers
and FuturePlus Systems Software

REV 1.3

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Agilent Technologies is also an authorized reseller of many FuturePlus products. Contact any Agilent Technologies sales office for details.

Product Warranty

Due to wide variety of possible customer target implementations, the FS1103 software has a 30 day acceptance period by the customer from the date of receipt. If the customer does not contact FuturePlus Systems within 30 days of the receipt of the product it will be said that the customer has accepted the product. If the customer is not satisfied with the FS1103, they may return it within 30 days for a refund.

This FuturePlus Systems product has a warranty against defects in material and workmanship for a period of 1 year from the date of shipment. During the warranty period, FuturePlus Systems will, at its option, either replace or repair products proven to be defective. For warranty service or repair, this product must be returned to the factory.

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In return for payment for this product, FuturePlus Systems grants the Customer a SINGLE user LICENSE in the software subject to the following:

- Customer may use the software on any one Agilent 1670x mainframe logic analysis system.
- Customer may make copies or adaptations of the software.
- Customer may not reverse assemble or decompile the software.

Copies and Adaptations

- Are allowed for archival purpose only.
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Customer agrees that it does not have any title or ownership of the software, other than the physical media.

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- Customer may not sublicense the software or distribute copies of the software to the public in physical media or by electronic means or any other means without the prior written consent of FuturePlus Systems.

Product Introduction

This manual covers two products, the FS1103 and FS1110. If you have purchased the FS1103 then refer to the 167xx sections, if you have purchased the FS1110 then refer to the 1680/90/900 sections.

The FS1103 is software product that provides the following functionality on a 16700/702 frame

- Provide configuration and Protocol Decode software for embedded probing of a 32 or 64 bit PCI bus using Mictor 38 pin connectors.
- Provide PCI State analysis using the FS2009 PCI-X 2.0 probe, FS2007 PCI-X probe, FS2010 PCI-X 2.0.

The FS1110 is software that provides the above functionality and is for the 1680/90/900 analyzers.

Embedded Probing of PCI

About the Pinout

This document describes the pinout for the AMP Mictor 38 pin header to a 32 or 64 bit PCI local bus. Following this pinout will allow the user to use the E5346A High-Density Termination Adapter Cable and the FuturePlus Systems 64 bit PCI software for PCI analysis with an Agilent logic analyzer.

What you will need to analyze PCI

64 bit PCI

- 3 AMP 2-767004-2 surface mount connectors mounted on the target board and routed to the PCI Local bus.
- 3 E5346A High-Density Adapter Cables from FuturePlus Systems or Agilent, 6 logic analyzer PODS required.
- A software license from FuturePlus Systems for **16700/702** Agilent logic analyzers or a software license for the **1680/90/900** Agilent logic analyzer.

32 bit PCI

- 2 AMP 2-767004-2 surface mount connectors mounted on the target board and routed to the PCI Local bus.
- 2 E5346A High-Density Adapter Cables from FuturePlus Systems or Agilent, 4 logic analyzer PODS required.
- A software license from FuturePlus Systems for **16700/702** Agilent logic analyzers or a software license for the **1680/90/900** (FS1110) Agilent logic analyzer.

The Mictor-38 connectors will be referred to as #1 and #2 and #3 (#3 for 64 bit only). Each Mictor-38 connector connects to two logic analyzer PODS, an EVEN numbered POD and an ODD numbered POD. Pins 1,2 and 4 on both Mictor-38 connectors are no connects. Pin 3 and pins 39-43 should be connected to GROUND.

The FuturePlus Systems software FS1103 or FS1110 consists of configuration files and a Protocol Decoder. The protocol decoder software performs the following functions:

- ◆ Decode all PCI command and cycle types
- ◆ Provide insight into the data transfer by indicating burst length, byte enables and number of byte enables. These are all color coded to match the command.
- ◆ Color the transaction per the command for easy correlation. The colors used by the software are as follows:
 - Memory transactions: Green
 - I/O transactions: Yellow
 - Configuration transactions: Blue
 - Interrupt Acknowledge, Special Cycle transactions and the DAC cycle: Purple
 - Idle and Wait cycles: White

Installing the software on 16700/702

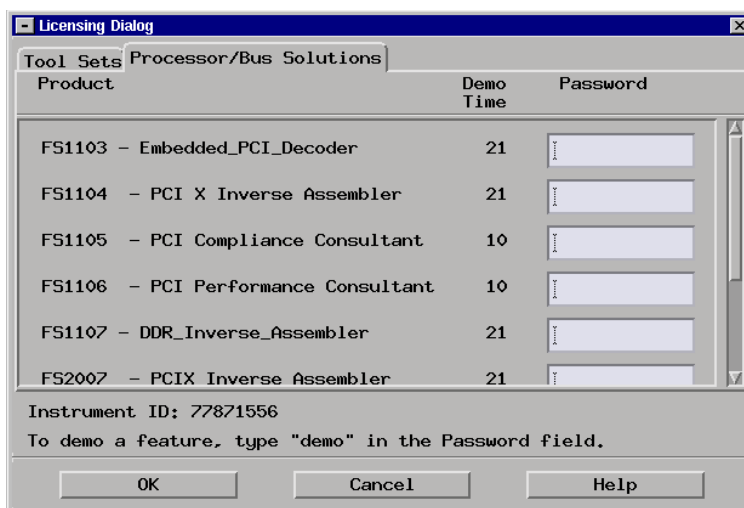
Place the disk labeled "16700/702 Installation disk for the FS1103" into the flexible disk of the 16700/702 frame and go to the system administration. From the install software tab of the system administration window press install. After pressing install another window will pop up, when the window pops up choose flexible disk and select apply. The system should access the flexible drive and a package name should appear in the lower portion of the window. Place the mouse pointer on the package name and press the left mouse button, the package name should now be highlighted, select install. The above procedure only needs to be done the first time the software is used. After several minutes the system should reply with "installation complete" restart the session and proceed with the licensing procedure below.

Licensing the software

The FS1103 product is a licensed product which is locked to a single Agilent 1670x frame. Complete instructions for licensing this software are detailed on the Entitlement Certificate that is enclosed with this product.

The licensing area for the 1670x mainframe is found under System Administration. Once you are at the licensing area choose the Processor/Bus Solutions tab, in here you will find the FS1103 listed. Type your password (you must use the entitlement certificate that came with the product to get the password) in the space provided to enable the use of the protocol decoder. A demo period is provided by typing the word demo into the password space next to the product name.

The following picture shows the licensing area after pressing the licensing button on the previous screen. This is where you would enter the password you will receive after following the instructions on the SW License Entitlement Certificate.



16700/702 Configuration files – including FS2009, FS2007, FS2010

Configuration files are loaded from the directory logic/configs/futureplus/FS1103 once the software has been installed successfully. For 64 bit configurations 2 cards must be configured as 1 logic analyzer consisting of a master and expander, only 1 card is required for 32 bit configurations. Load the configuration file that matches the type of logic analyzer card that is installed in your frame per the table below. The configuration file will set up labels and channel assignments based on the pinout in the back of the manual.

Logic Analyzer	File name for Analysis	Comment
167xx (requires 2 cards)	PC103_1	64 bit analysis
167xx	PC103_2	32 bit analysis
16554/5/6/7 (requires 2 cards)	PC103_3	64 bit analysis
16554/5/6/7	PC103_4	32 bit analysis
167xx (requires 2 cards)	*PC103_5	For use with FS2009 probe
167xx (requires 2 cards for 64 bit)	PC103_6	For use with FS2007 probe
167xx (requires 2 cards for 64 bit)	*PC103_7	For use with the FS2010 probe

*Users who own an FS2009 probe can use this configuration file along with the FS2009 probe to analyze a 3.3 volt PCI bus, the probe cannot be used in 5 volt PCI buses. **If you are loading this configuration file into 16753/4/5/6 cards you must change the threshold setting for the J1 master clock from 750mv to differential, otherwise you will not get a PCI clock to the analyzer.**

** Users who own an FS2010 probe can use this configuration file along with the FS2010 probe to analyze a 3.3 volt PCI bus, the probe cannot be used in 5 volt PCI buses.

Setting up the 1680/90/900 Analyzer Using FS1110 Software

The 1680/90/900 Analyzer is a PC based application that requires a PC running the Windows OS or a 16900 frame.

Before installing the protocol decoder for the PCI protocol on a PC you must install the Agilent logic analyzer software. Once the Agilent logic analyzer software is installed, you can install the FS1110 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the .exe file on the CD-ROM disk and then double click the .exe file name from within the File Explorer navigation panel.

1680/90/900 Licensing

The PCI Inverse Assembler is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

Loading 1680/90/900 Configuration Files

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it

should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

1680/90/900 Configuration Files

Logic Analyzer	File Name for Analysis	Comments
1675x, 1691x, 1695x, 1680/90	CP200_4	For use with FS2000, 32 bit
1675x, 1691x, 1695x, 1680/90	CP201_6	For use with FS2001 or embedded solution, 32 bit
1675x, 1691x, 1695x, 1680/90	CP201_7	For use with FS2001 or embedded solution, 64 bit
1675x, 1691x, 1695x, 1680/90	CP204_4	For use with FS2004, 32 bit
1675x, 1691x, 1695x, 1680/90	CP207_1	For use with FS2007, 32 bit
1675x, 1691x, 1695x, 1680/90	CP207_2	For use with FS2007, 64 bit
1675x, 1691x, 1695x, 1680/90	CP256_8s	For use with FS2005/6, 32 bit
1675x, 1691x, 1695x, 1680/90	CP256_9s	For use with FS2005/6, 64 bit
1675x, 1691x, 1695x, 1680/90	CP302_9	For use with FS3020, 64 bit
1675x, 1691x, 1695x, 1680/90	CP302_10	For use with FS3020, 32 bit
1675x, 1691x, 1695x, 1680/90	CP311_6	For use with FS3011, 32 bit
1675x, 1691x, 1695x, 1680/90	CP311_7	For use with FS3011, 64 bit
1671x, 1675x, 1691x, 1695x, 1680/90	*CP103_5	2 Card config. for use with the FS2009
1671x, 1675x, 1691x, 1695x, 1680/90	**CP210_1	2 Card config. for use with the FS2010

*Users who own an FS2009 probe can use this configuration file along with the FS2009 probe to analyze a 3.3 volt PCI bus, the probe cannot be used in 5 volt PCI buses. **If you are loading this configuration file into 16753/4/5/6 cards you must change the threshold setting for the J1 master clock from 750mv to differential, otherwise you will not get a PCI clock to the analyzer.**

** Users who own an FS2010 probe can use this configuration file along with the FS2010 probe to analyze a 3.3 volt PCI bus, the probe cannot be used in 5 volt PCI buses.

Attaching logic analyzer cables

The following table shows how to attach the logic analyzer cables to the adapter cables, a pinout of the channel assignments to each pod is shown in the “format menu” section of this manual. For 16900 users the cable connections can be found using the General Purpose Probe Add-In feature from the overview window. After loading the configuration file click on the properties button on the General Purpose Probe Add-In icon, highlight the connection and press the edit button. A diagram will be displayed showing the signal name on each input to the analyzer as well as what connector the analyzer cable should go to.

Connector	16554/6/7 & 167xx analyzers	1680/90 analyzer	Comments
Mictor 1 odd	Master pod 1	Pod 1	
Mictor 1 even	Master pod 2	Pod 2	
Mictor 2 odd	Master pod 3	Pod 3	
Mictor 2 even	Master pod 4	Pod 4	
Mictor 3 odd	Expander pod 1	Pod 5	Optional 64 bit
Mictor 3 even	Expander pod 2	Pod 6	Optional 64 bit

For FS2009 users use the following table:

Connector	16554/6/7 & 167xx, 169xx analyzers	Comments
J1 odd	Master pod 1	
J1 even	Master pod 2	
J2 odd	Master pod 3	
J2 even	Master pod 4	
J3 odd	Expander pod 1	Optional 64 bit
J3 even	Expander pod 2	Optional 64 bit

For FS2007 users use the following table:

Connector	16554/6/7 & 167xx, 169xx analyzers	1680/90 analyzers	Comments
Header 1	Master pod 1	Pod 1	
Header 2	Master pod 2	Pod 2	
Header 3	Master pod 3	Pod 3	
Header 4	Master pod 4	Pod 4	
Header 5	Expander pod 1	Pod 5	Optional 64 bit
Header 6	Expander pod 2	Pod 6	Optional 64 bit

For FS2010 users use the following table:

Connector	16554/6/7 & 167xx, 169xx analyzers	Comments
J2 odd	Master pod 1	
J2 even	Master pod 2	
J3 odd	Master pod 3	
J3 even	Master pod 4	
J4 odd	Expander pod 1	Optional 64 bit
J4 even	Expander pod 2	Optional 64 bit

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

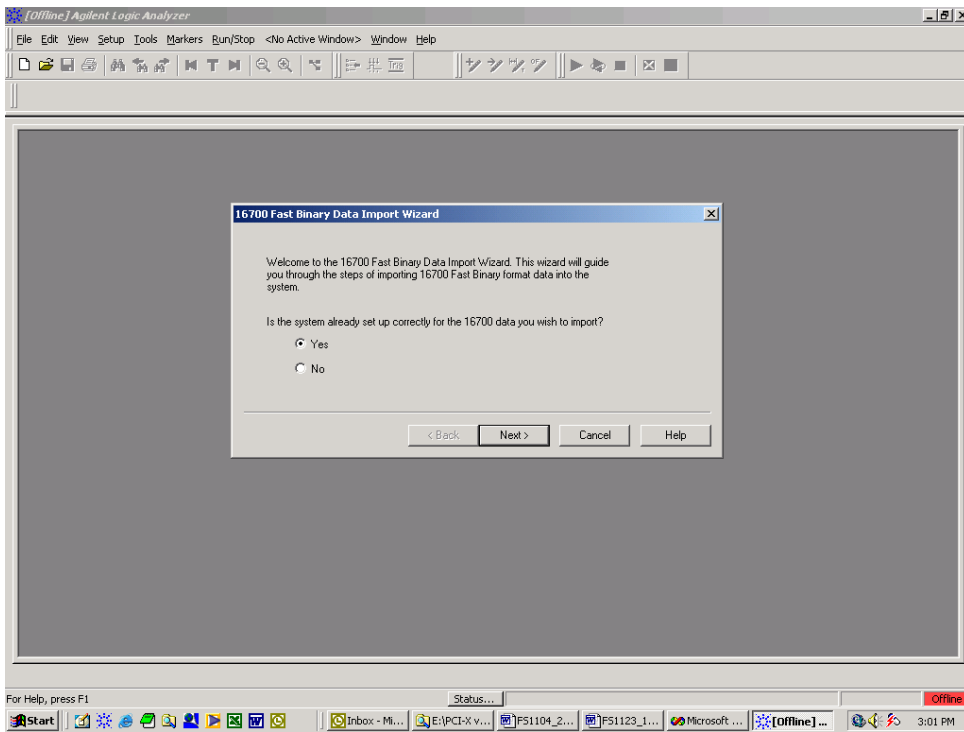
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may buy additional licenses, please contact FuturePlus sales department.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up 1680/90/900 analyzer". Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

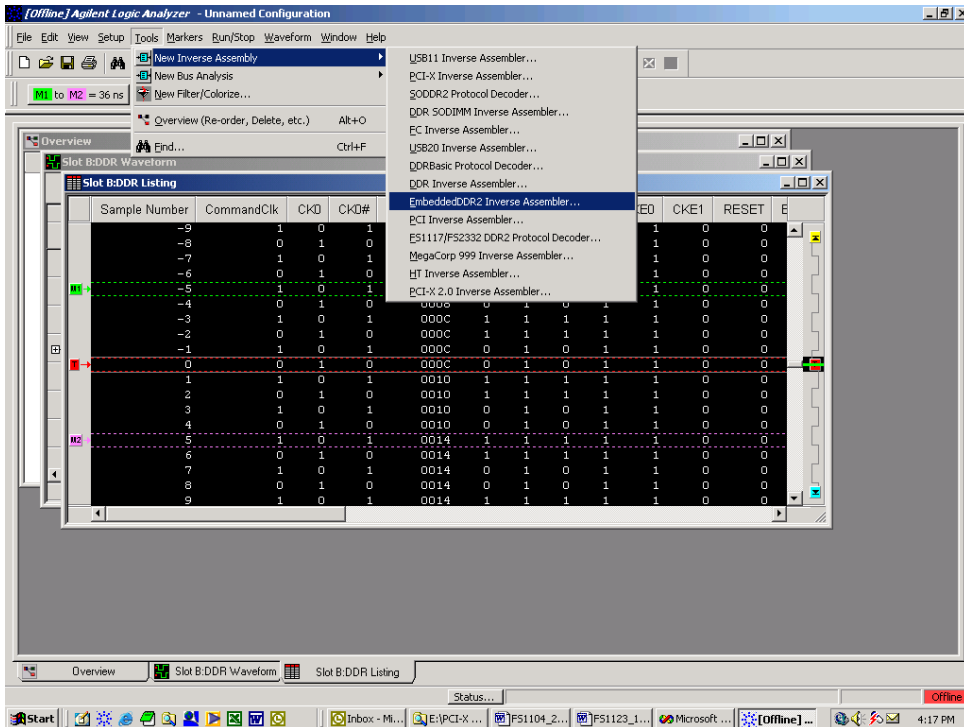
For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select "yes" when it asks if the system is ready to import 16700 data.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.



After the decoder has loaded, select Preferences if required, from the overview screen and set the preferences to their correct value in order to decode the trace properly. This is a general requirement, some decoders do not have preferences, if this is the case then no preference setting is necessary.

Format Menu*

The PCI Analysis Probe diskette sets up the format menu as shown in the following table. This format is the same for both Timing and State Analysis.

Label	Clk Inputs	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
STAT	M,K,J			8-0	14-0		
ADDR						15-0	15-0
ADDR_B		15-0	15-0				
USER7_1				15-9			
INTD_A					14-11		
RESET					10		
C/B7_0					9-6		
DATA						15-0	15-0
DEVSEL					5		
STOP					4		
LOCK					3		
PERR					2		
SERR					1		
PAR					0		
SD/SB0				8-7			
PAR64				2			
ACK/RQ				1-0			
IRDY	J			9			
FRAME	K			10			
TRDY	M			11			
PCICLK	L						

**This is a sample format menu. The configuration you choose may be different. Please refer to the analyzer or your actual hardware information for your correct format.*

The STAT variable

The STAT variable is used by the PCI inverse assembler to decode PCI bus transactions. *It should not be changed or deleted from the format menu.* The signals that make up the STAT variable are listed in the following table. The STAT variable can be useful to set up SYMBOLS since it contains all of the key PCI control and status signals.

STAT Variable	PCI Bus Signal Name
Bit 26	TRDY#
Bit 25	FRAME#
Bit 24	IRDY#
Bit 23	SDONE
Bit 22	SB0#
Bit 21	C/BE7#
Bit 20	C/BE6#
Bit 19	C/BE5#
Bit 18	C/BE4#
Bit 17	PAR64#
Bit 16	ACK64#
Bit 15	REQ64#
Bit 14	INTD#
Bit 13	INTC#
Bit 12	INTB#
Bit 11	INTA#
Bit 10	RESET#
Bit 9	C/BE3#
Bit 8	C/BE2#
Bit 7	C/BE1#
Bit 6	C/BE0#
Bit 5	DEVSEL#
Bit 4	STOP#
Bit 3	LOCK#
Bit 2	PERR#
Bit 1	SERR#
Bit 0	PAR

ADDR, ADDR_B, DATA labels

The ADDR variable is the lower 32 bits of the PCI AD bus. The ADDR_B is the upper 32 bits of the PCI AD bus. The DATA variable is a dummy variable that needs to be defined for the PCI protocol decoder. *These variables should not be changed or deleted from the format Menu.*

The CYCLE variable

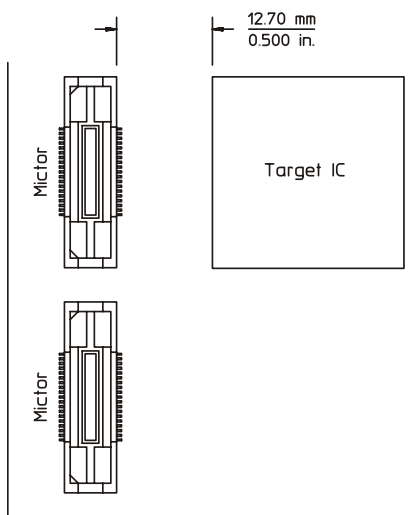
The CYCLE variable is made up of the following PCI signals: TRDY#, FRAME#, IRDY#, C/BE(3:0), DEVSEL# and STOP#. This variable has 30 symbols defined that can be used to help make triggering, timing analysis and pattern filtering easier. The following lists the bit pattern and the corresponding symbol.

Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP#
INTACK	1	0	1	0000	1	1
SPEC_CYC	1	0	1	0001	1	1
I/O_RD	1	0	1	0010	1	1
I/O_WR	1	0	1	0011	1	1
RESVRD	1	0	1	0100	1	1
RESVRD	1	0	1	0101	1	1
MEM_RD	1	0	1	0110	1	1
MEM_WR	1	0	1	0111	1	1
RESRVD	1	0	1	1000	1	1
RESRVD	1	0	1	1001	1	1
CON_RD	1	0	1	1010	1	1
CON_WR	1	0	1	1011	1	1
MEMRDM	1	0	1	1100	1	1
DAD_CY	1	0	1	1101	1	1
MEMRDL	1	0	1	1110	1	1
MEMWRI	1	0	1	1111	1	1
IO_XACTION	1	0	1	001X	1	1
MEM_XACTION	1	0	1	011X	1	1
CONFIG_XACTION	1	0	1	101X	1	1
ADD_CYCLE	1	0	1	XXXX	1	1

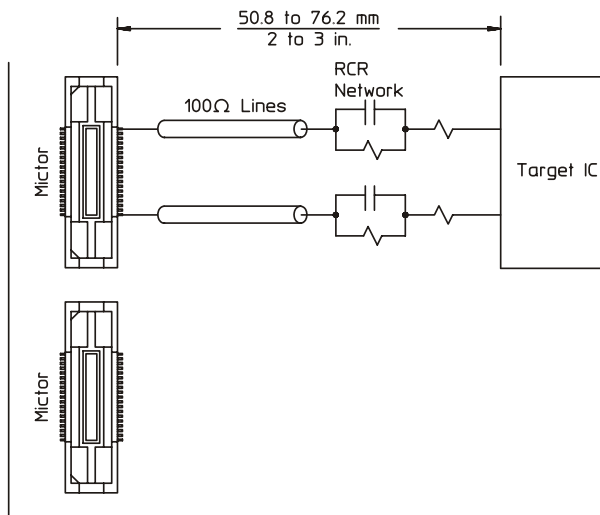
Symbol	TRDY#	FRAME#	IRDY#	C/BE(3:0)	DEVSEL#	STOP#
DATA_XFER	0	0	0	XXXX	0	1
WAIT_TARGET	1	X	0	XXXX	0	1
WAIT_INITIATOR	0	X	1	XXXX	0	1
DATA_FINALXFER	0	1	0	XXXX	0	1
STOP_NOXFER	X	0	1	XXXX	0	0
STOP_DATAXFER	0	X	0	XXXX	0	0
STOP_RETRY	1	1	0	XXXX	0	0
TARGET_ABORT	1	0	1	XXXX	1	0
IDLE	X	1	1	XXXX	X	X
WAIT_NODEVSEL	X	X	0	XXXX	1	1

Where to place the MICTOR connectors on the target

The recommended placement of the mictor connectors is at either end of the bus segment. The mictors should be placed at the end of as short a stub as possible daisy chained off either end of the bus. If there is not enough room to place the mictors **0.5 inches** from the target then an alternate method may be used. That is, to place the logic analyzer termination circuitry on the target and then extend the etch from the end of the termination circuitry over to the mictor connectors. The connection from the mictors to the logic analyzer must then be done with the **E5351A**. The E5346A contains the logic analyzer termination circuitry, the E5351A does not.



Example for HP E5346A



Example for HP E5351A

e5346e12

The Termination Network

The termination network consists of a 249 ohm resistor in series with the parallel combination of a 90K ohm resistor and a 8.2pF capacitor. The components are placed as shown in the drawing above. If the etch from the network to the mictor connector is less than one inch, the impedance of the etch can be in the 60-75 ohm range. If it is longer, it should be controlled at 100 ohms.

If the termination network is placed on the target then the stub should be 0.5" or less. In general, the stub must be \ll 50% of the wavelength of the rise time of the signal for it to be treated as a lumped C rather than a transmission line.

PCI Signal Assignment

FuturePlus Systems will supply a configuration file with the FS1103 product that matches the following pinout. However it should be noted that the pinout could be re-pinned by the user for **16700/702 systems** in order to match etch lengths and control skew.

Routing and Re-pinning Information

In order to control skew all etch lengths should be near equal. If it makes sense from a layout point of view, the signals may be re-pinned on the mictor connectors. The user would then only need to modify the included configuration file to match the actual layout. The following restrictions apply.

- The clock cannot be re-pinned to a signal pin
- Bit re-ordering can be used to put the command/AD signals back in order. If the AD signals are RE-ORDERED then the user will not be able to use the IN RANGE feature in the triggering menu for address range triggering.
- The CYCLE variable will need to be bit re-ordered to match the supplied symbols in the configuration file. (This is not a difficult task).

GNT#, REQ# and IDSEL signals

It is recommended that the target system GNT# lines and optionally the REQ# and IDSEL signals of the target PCI local bus be connected to the unused or user pins. This may make debugging and performance analysis easier.

State Analysis

Acquiring Data on 16700/702

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full, the trigger specification is TRUE or when you touch STOP.

The logic analyzer will flash “Slow or Missing Clock” when the data is not being transmitted across the bus.

Acquiring Data on 1680/90/900 analyzer

Execute the Agilent Logic Analyzer software on the PC and then load the appropriate configuration file.

To load the configuration file go to the desktop, double click the FS1110 folder icon, select the appropriate configuration file for your situation by double clicking on the name of the file. Refer to the table under “1680/90/900 configuration files” for more details on the configuration files.

To capture PCI data, depress the F5 key or click the green arrow (run) button that is located on the tool bar at the top of the screen after setting up a trigger.

If you are analyzing a 32 bit bus you only need to attach pods 1 through 4 and leave pods 5 and 6 disconnected. Use the table listed under “Attaching logic analyzer cables” for proper cable attachment.

State Display

Captured data is as shown in the following figure. The figure below displays the state listing after disassembly. The protocol decoder is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

Listing<3>

File Edit Options Invasm Source Help

Navigate Run

Search Goto Markers Comments Analysis Mixed Signal

Label ACK/RQ Value when Present Next Prev

Advanced searching... Set G1 Set G2

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	INTD.
Decimal	PCI BUS TRANSACTIONS REV 2.8	Symbols	Relative	Hex
27	FUNC=0 REG OFFSET=4C TYPE=00 D32=xxxx00xx	DATA_FINALXF	188,000 ns	F
28	CONFG WR ADR=0000404C FUNC=0 REG OFFSET=4C TYPE=00	CON_WR	312,000 ns	F
30	D32=xxxxxx48	DATA_FINALXF	184,000 ns	F
31	CONFG READ ADR=0000404C FUNC=0 REG OFFSET=4C TYPE=00	CON_RD	220,000 ns	F
33	D32=xxxxxx48	DATA_FINALXF	156,000 ns	F
34	I/O WRITE ADR=00008020	I/O_WR	252,000 ns	F
38	D32=xxxxxx18	DATA_FINALXF	656,000 ns	F
39	I/O WRITE ADR=00008021	I/O_WR	220,000 ns	F
43	D32=xxxx6Axx	DATA_FINALXF	780,000 ns	F
44	I/O WRITE ADR=00008022	I/O_WR	188,000 ns	F
48	D32=xx29xxxx	DATA_FINALXF	812,000 ns	F
49	I/O WRITE ADR=00002400	I/O_WR	312,000 ns	F
53	D32=xxxxxx37	DATA_FINALXF	688,000 ns	F
54	I/O WRITE ADR=00006008	I/O_WR	6,262 ms	F
58	D32=xxxxxx0C	DATA_FINALXF	656,000 ns	F

16700 Display

[Offline] Agilent Logic Analyzer - [L:\stored data\CP200_4.ala] - [Listing - 1]

File Edit View Setup Tools Markers Run/Stop Window Help

M1 to M2 = 4.95 ns

LE	CMD	COMMAND	WAIT	AddressH	AddressL	DataH	DataL	Termination	Term_Code
48	0002	I/O Read							
B8	0002		Wait-No DEVSEL						
B9	0002					xxxxxx36		Initiator	0
48	0002	I/O Read		00000040					
B8	0002		Wait-No DEVSEL					STOP Retry	3
48	0002	I/O Read		00000040					
B8	0002		Wait-No DEVSEL						
B9	0002					xxxxxx17		Initiator	0
4F	0003	I/O Write		00000021					
B7	0003		Wait-No DEVSEL						
B5	0003					xxxxFCxx		Initiator	0
4F	0003	I/O Write		000000A1					
B7	0003		Wait-No DEVSEL						
B5	0003					xxxxFDxx		Initiator	0
M2	47	0001	Spec Cyc						
83	0001	Cmd=Halt, M		00000001					
83	0001		Wait-No DEVSEL						
83	0001		Wait-No DEVSEL						
83	0001		Wait-No DEVSEL					Master Abort	4
49	0000	Int Ack		00000000					
90	0000		Wait-No DEVSEL			50xxxx50		Initiator	0
90	0000								
4F	0003	I/O Write		00000021					
B7	0003		Wait-No DEVSEL						
B5	0003					xxxxFDxx		Initiator	0
4F	0003	I/O Write		00000020					
B8	0003		Wait-No DEVSEL						
B9	0003					xxxxxx60		Initiator	0
4F	0003	I/O Write		00000021					
B7	0003		Wait-No DEVSEL						

Listing - 1

For Help, press F1

Offline NUM 3:11 PM

1680/90/900 display

Error Messages

The following error messages are reported by the PCI protocol decoder

ERROR-NO DEVICE SELECTED

This error is displayed during a non special cycle data phase when IRDY and TRDY are asserted and DEVSEL is not asserted.

ERROR DEVSEL ASSERTED

This error is displayed during a special cycle data phase if DEVSEL is asserted.

SYSTEM ERROR

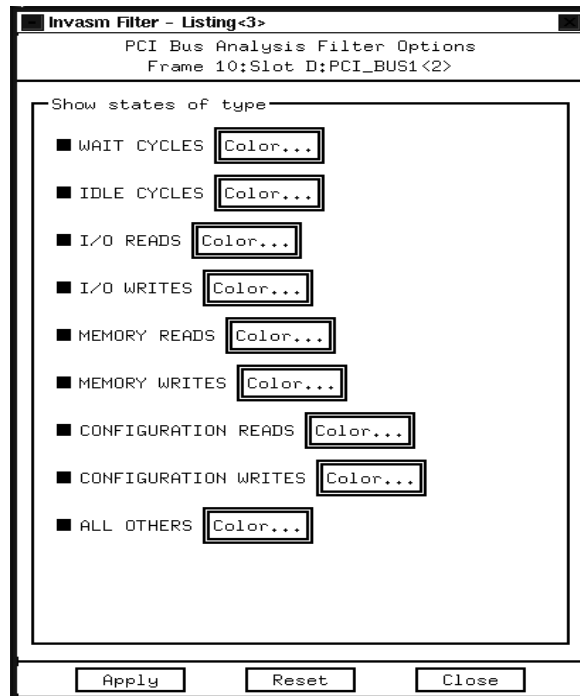
This error is displayed anytime SERR# is asserted.

INVASM options

INVASM OPTIONS is available with the 16700/702 logic analyzer frames.

1680/90 does not implement an INVASM Options menu.

INVASM OPTIONS can be invoked on the 16700/702 by selecting filter under INVASM in the state listing.



The acquired state listing display can be modified to filter out any combination of the above transactions or cycles by selecting the show/suppress button to the right of the transaction cycle list.

For 1680/90/900 users, select the Filter/Colorization pull down menus in the state listing and create a filter (downstream) tool.

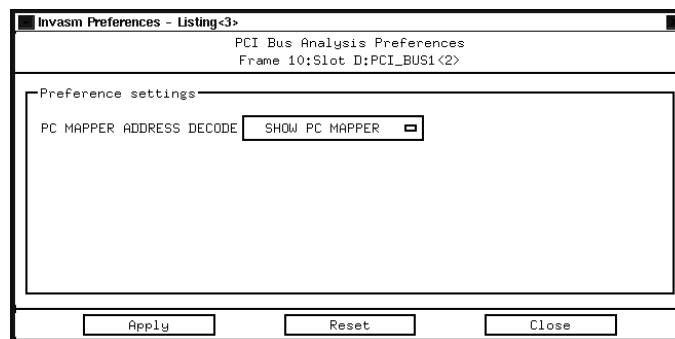
The 1680/90/900 IA filtering provides similar filtering capabilities as is provided in the 16700/702 environments. You may filter on any label, when using the filter tags label you can select symbols to make choosing transactions easier. To create a filter, choose Tools->New->Filter/Colorize. Then fill in the information on the window that opens up. You must create a new filter for each item you want filtered. To remove filters that you no longer want, go to Tools->Overview and then choose the filter you want removed and click Delete.

Using the PC Mapper Protocol Decoder

The PCI Analysis Probe PC Mapper software is an enhanced version of the PCI Analysis Probe Protocol Decoder and is for use only with PCI Analysis Probe from FuturePlus Systems Corporation. The enhancement includes PCI I/O and memory address decode to indicate common PC access.

PC Mapper is not available on the 1680/90/900.

To select PC Mapper function on the 16700, select INVASM from the state listing display then select PREFERENCES. When you select PREFERENCES it will come up with a box and there you can choose to turn on PC Mapper or suppress PC Mapper. The picture below displays PC Mapper function enabled on the 16700.



The state display with PC Mapper

Captured data is as shown in the following figure. The first figure displays the state listing after disassembly. The PCI PC Mapper is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages and phases specified in the PCI Local Bus specification. Symbols have also been defined to help aid in analysis. The non-disassembled state listing displays PCI bus mnemonics in addition to data. All data is displayed in hex. One exception is the decode of the address for a CONFIGURATION READ or a CONFIGURATION WRITE transaction. The Function (FUNC=) and Bus (BUS=) data is displayed in decimal.

Listing-4- File Window Edit Options Invasm Source Help

Goto Markers Search Comments Analysis Mixed Signal

Label ACK/RQ Hex X when Present Next Prev

Advanced searching Set G1 Set G2

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	USR7_1
Decimal	PCI BUS TRANSACTIONS REV 2,8	Symbols	Absolute	Hex
0	SYSTEM MEMORY MEM READ ADR=F3FC0000	MEM_RD	0 s	00
1	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	16,000 ns	00
2	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	28,000 ns	00
3	D32=12345678	DATA_FINALXF	88,000 ns	00
4	SYSTEM MEMORY MEM WRITE ADR=F3FC0004	MEM_WR	111,687 ms	00
5	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111,687 ms	00
6	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111,687 ms	00
7	D32=9ABCDEF0	DATA_FINALXF	111,687 ms	00
8	SYSTEM MEMORY MEM READ ADR=F3FC0004	MEM_RD	223,194 ms	00
9	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223,194 ms	00
10	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223,194 ms	00
11	D32=9ABCDEF0	DATA_FINALXF	223,195 ms	00

With PC Mapper

Listing-4- File Window Edit Options Invasm Source Help

Goto Markers Search Comments Analysis Mixed Signal

Label ACK/RQ Hex X when Present Next Prev

Advanced searching Set G1 Set G2

State Number	FUTUREPLUS SYSTEMS c 2000	CYCLE	Time	USR7_1
Decimal	PCI BUS TRANSACTIONS REV 2,8	Symbols	Absolute	Hex
0	MEM READ ADR=F3FC0000	MEM_RD	0 s	00
1	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	16,000 ns	00
2	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	28,000 ns	00
3	D32=12345678	DATA_FINALXF	88,000 ns	00
4	MEM WRITE ADR=F3FC0004	MEM_WR	111,687 ms	00
5	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111,687 ms	00
6	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	111,687 ms	00
7	D32=9ABCDEF0	DATA_FINALXF	111,687 ms	00
8	MEM READ ADR=F3FC0004	MEM_RD	223,194 ms	00
9	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223,194 ms	00
10	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	223,194 ms	00
11	D32=9ABCDEF0	DATA_FINALXF	223,195 ms	00
12	MEM WRITE ADR=F3FC0008	MEM_WR	334,826 ms	00
13	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	334,826 ms	00
14	WAIT-NO DEVICE SELECT	WAIT_NODEVSE	334,826 ms	00

Without PC Mapper

PCI PC Mapping for memory transactions

This section lists the addresses, commands and the corresponding mapping done by the PCI PC Mapper software. For information on the standard PCI configuration register mapping please refer to the PCI Local Bus Specification Rev 2.0.

Address bits 23-0	PC Mapper output
greater than 0FFFFFFH	System Memory
0FFFFFF-0E0000H	System BIOS
0DFFFF-0C0000H	ROM Scan
0BFFFF-0A0000H	Video Memory
09FFFF-000400H	System Memory
0003FF-000000H	See Interrupt Vector Table

Interrupt Vector Table

Address bits 23-0	PC Mapper output
0003C4H	INT #F1-FF USER PROGRAMS
000200H	INT #80-F0 BASIC
0001E0H	INT #78-7F USER PROGRAMS
0001DCH	INT #77 IRQ15
0001D8H	INT #76 IRQ14
0001D4H	INT #75 IRQ13
0001D0H	INT #74 IRQ12
0001CCH	INT #73 IRQ11
0001C8H	INT #72 IRQ10
0001C4H	INT #71 IRQ9
0001C0H	INT #70 IRQ8
0001A0H	INT #68-6F RESERVED
00019CH	INT #67 EXP MEM MANG
000180H	INT #60-66 USER PROGRAMS
00012CH	INT #4B-5F RESERVED
000128H	INT #4A USER RTC ALARM
00011CH	INT #47-49 RESERVED
000118H	INT #46 HD DISK #1 PARAM
000110H	INT #44-45 RESERVED
00010CH	INT #43 VIDEO CHAR TABLE
000108H	INT #42 EGA BIOS
000104H	INT #41 HD DISK #0 PARAM
000100H	INT #40 FLOPPY DISK ISR
000080H	INT #20-3F RESERVED DOS
00007CH	INT #1F VIDEO CHAR TABLE
000078H	INT #1E FLOPPY PARAMS
000074H	INT #1D AVAILABLE
000070H	INT #1C AVAILABLE
00006CH	INT #1B KEYBOARD BREAK
000068H	INT #1A RTC ISR

Address bits 23-0	PC Mapper output
000064H	INT #19 BOOSTRAP LOADER
000060H	INT #18 ROM BASIC
00005CH	INT #17 LPT PRINTER BIOS
000058H	INT #16 KEYBOARD BIOS
000054H	INT #15 SYS SERVICE BIOS
000050H	INT #14 SERIAL PORT BIOS
00004CH	INT #13 FLOPPY DISK BIOS
000048H	INT #12 MEM SIZE INT
000044H	INT #11 EQUIP LIST
000040H	INT #10 VIDEO BIOS
00003CH	INT #0F IRQ7 LPT1
000038H	INT #0E IRQ6 FLOPPY DISK
000034H	INT #0D IRQ5 LPT2
000030H	INT #0C IRQ4 SERIAL #1
00002CH	INT #0B IRQ3 SERIAL #2
000028H	INT #0A IRQ2 SLAVE INT
000024H	INT #09 KEYBOARD
000020H	INT #08 IRQ0 SYS TIMER
00001CH	INT #07 NUM COPROCESSOR
000018H	INT #06 INVALID OPCODE
000014H	INT #05 PRINT SCREEN
000010H	INT #04 OVERFLOW DETECT
00000CH	INT #03 BREAKPOINT TRACE
000008H	INT #02 NMI
000004H	INT #01 SINGLE STEP
000000H	INT #00 DIVIDE BY ZERO

PCI PC Mapping - I/O Transactions

Address bits 23-0	PC Mapper output
0000H	MSTR DMA CH 0
0001H	MSTR DMA CH 0
0002H	MSTR DMA CH 1
0003H	MSTR DMA CH 1
0004H	MSTR DMA CH 2
0005H	MSTR DMA CH 2
0006H	MSTR DMA CH 3
0007H	MSTR DMA CH 3
0008H	MSTR DMA STAT REG
0009H	UNKNOWN IO DEVICE
000AH	MSTR DMA MASK REG
000BH	MSTR DMA MODE REG
000CH	MSTR DMA CLR BYTE PTR
000DH	MSTR DMA MSTR CLEAR
000EH	MSTR DMA CLEAR MASK
000FH	MSTR DMA WRT MASK
0018H	MSTR DMA CH EXT FUNCT REG
001AH	MSTR DMA EXT FUNCT
0020H	MSTR INT REQ REG
0021H	MSTR INT REQ REG2
0040H	INTERVAL TIMER TIMER 0
0042H	INTERVAL TIMER SPKR TIMER
0043H	INTRVAL TIMER #1 CNTRL
0044H	INTERVL TIMER #2 WATCHDOG
0047H	INTERVAL TIMER #2 CNTRL
0060H	KEYBOARD/MOUSE DATA PORT
0061H	SYSTEM CONTOL PORT B
0064H	KEYBOARD/MOUSE CMD PORT
0070H	RTC/CMOS RAM ADDR PORT
0071H	RTC/CMOS RAM DATA PORT
0074H	EXT CMOS RAM ADDR PORT
0075H	EXT CMOS RAM ADDR PORT
0076H	EXT CMOS RAM DATA PORT
0081H	CH 2 DMA PAGE REGISTER
0082H	CH 3 DMA PAGE REGISTER
0083H	CH 1 DMA PAGE REGISTER
0087H	CH 0 DMA PAGE REGISTER
0089H	CH 6 DMA PAGE REGISTER
008AH	CH 7 DMA PAGE REGISTER
008BH	CH 5 DMA PAGE REGISTER
008FH	CH 4 DMA PAGE REGISTER
0090H	ARB CNTRL POINT REG
0091H	FEEDBACK REG
0092H	SYSTEM CONTROL PORT A
0094H	SYS SETUP/CARD ENABLE REG
0096H	ADAPTOR SETUP/ENABLE REG
00A0H	SLAVE INTERRUPT CNTRLR
00A1H	SLAVE INTERRUPT CNTRLR
00C0H	SLAVE DMA CH4 MEM ADDR
00C2H	SLAVE DMA CH4 TRANS COUNT

Address bits 23-0	PC Mapper output
00C4H	SLAVE DMA CH5 MEM ADDR
00C6H	SLAVE DMA CH5 TRANS COUNT
00C8H	SLAVE DMA CH6 MEM ADDR
00CAH	SLV DMA CH6 TRANS COUNT
00CCH	SLAVE DMA CH7 MEM ADDR
00CEH	SLAVE DMA CH7 TRANS COUNT
00D0H	SLV DMA STATUS REG CH 4-7
00D4H	SLV DMA MASK REG CH 4-7
00D6H	SLAVE DMA MODE REG CH 4-7
00D8H	SLAVE DMA CLEAR BYTE PNTR
00DAH	SLAVE DMA MASTER CLEAR
00DCH	SLV DMA CLR MASK CH 4-7
00DEH	SLAVE DMA WRITE MASK REG
00E0H	IBM MODELS - ENCODE REG
00E1H	IBM MODELS - ENCODE REG
00F1H	NUMERIC COPROCESSOR RESET
00F8H	NUMERIC COPROCESSOR PORT
00F9H	NUMERIC COPROCESSOR PORT
00FAH	NUMERIC COPROCESSOR PORT
00FBH	NUMERIC COPROCESSOR PORT
00FCH	NUMERIC COPROCESSOR PORT
0100H	ADAPTER CARD POS REG 0
0101H	ADAPTER CARD POS REG 1
0102H	SYS BD/ADP CD POS REG 2
0103H	SYS BD/ADP CD POS REG 3
0104H	ADAPTER CARD POS REG 4
0105H	ADAPTER CARD POS REG 5
0106H	ADAPTER CARD POS REG 6
0107H	ADAPTER CARD POS REG 6
0278H	PARALLEL PORT 3 DATA PORT
0279H	PARALLEL PORT 3 STAT PORT
027AH	PARALLEL PORT 3 CMD PORT
02F8H	SERIAL PORT 2 XMIT/REC
02F9H	SER PORT 2 DIV LATCH/INT
02FAH	SERIAL PORT 2 INT ID REG
02FBH	SERIAL PORT 2 CNTRL REG
02FDH	SERIAL PORT 2 MODEM CNTRL
02FEH	SERIAL PORT 2 MODEM STAT
02FFH	SERIAL PORT 2 SCRTCH REG
0378H	PARALLEL PORT 2 DATA PORT
0379H	PARALLEL PORT 2 STAT PORT
037AH	PARALLEL PORT 2 CMD PORT
03B4H	VGA CRT CNTRLR ADDR REG
03B5H	VGA CRT CNTRLR DATA REG
03BAH	VGA STAT 1/FEATURE CNTRL
03BCH	PARALLEL PORT 1 DATA PORT
03BDH	PARALLEL PORT 1 STAT PORT

Address bits 23-0	PC Mapper output
03BEH	PARALLEL PORT 1 CMD PORT
03C0H	VGA ATTRIBUTE CNTRLR ADDR
03C1H	VGA ATTRIBUTE CNTRLR DATA
03C2H	VGA OUTPUT/STAT REG
03C3H	VGA VIDEO SUBSYSTEM ENABLE
03C4H	VGA SEQUENCER ADDR REG
03C5H	VGA SEQUENCER DATA REG
03C6H	VIDEO DAC PEL MASK
03C7H	VIDEO DAC PAL ADDR/STAT
03C8H	VIDEO DAC PAL ADDR/WRITE
03C9H	VIDEO DAC PALETTE DATA
03CAH	VGA FEATURE CONTROL REG
03CCH	VGA MISC OUTPUT REG
03CEH	VGA GRAPHICS CNTRLR ADDR
03CFH	VGA GRAPHICS CNTRLR ADDR
03D4H	VGA CRT CNTRLR ADDR REG
03D5H	VGA GRAPHICS CNTRLR DATA
03DAH	VGA COLOR STAT 1/FEATURE
03F0H	FLOPPY STATUS REG A
03F1H	FLOPPY STATUS REG B
03F2H	FLOPPY DIGITAL OUTPUT REG
03F4H	FLOPPY DISK CNTRLR STAT
03F5H	FLOPPY DISK CNTRLR DATA
03F7H	FLOPPY CONFIG CONTROL REG
03F8H	SERIAL PORT 1 XMIT/RCV BUF
03F9H	SER PORT 1 DIV LATCH/INT
03FAH	SERIAL PORT 1 INT ID/FIFO
03FBH	SERIAL PORT 1 LINE CNTRL
03FCH	SERIAL PORT 1 MODEM CNTRL
03FDH	SERIAL PORT 1 STAT REG
03FEH	SERIAL PORT 1 MODEM STAT
03FFH	SERIAL PORT 1 SCRATCH REG
0680H	MANUFACTURING CHECKPOINT PORT

Timing Analysis

If timing analysis is preferred, load the configuration file for the card you are using and in the sampling tab of the logic analyzer change from state mode to timing mode. In timing mode the protocol decoder is not used.

Once in timing mode set the trigger to the desired setting, press the green run button and the analyzer is ready to capture data.

Timing analysis is not possible when using the FS2009 probe to capture PCI data, the FS2009 is a state only probe.

LOGIC ANALYZER POD 1

Mictor-38 #1 Pin Number ODD POD	Logic Analyzer channel number	PCI Signal name
6	CLK/16	IRDY#
8	15	AD15
10	14	AD14
12	13	AD13
14	12	AD12
16	11	AD11
18	10	AD10
20	9	AD09
22	8	AD08
24	7	AD07
26	6	AD06
28	5	AD05
30	4	AD04
32	3	AD03
34	2	AD02
36	1	AD01
38	0	AD00

LOGIC ANALYZER POD 2

Mictor-38 #1 Pin Number EVEN POD	Logic Analyzer channel number	PCI Signal name
5	CLK/16	FRAME#
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

LOGIC ANALYZER POD 3

Mictor-38 #2 Pin Number ODD POD	Logic Analyzer channel number	PCI Signal name
6	CLK/16	PCI Clock
8	15	unused*
10	14	INTD#
12	13	INTC#
14	12	INTB#
16	11	INTA#
18	10	RST#
20	9	C/BE3#
22	8	C/BE2#
24	7	C/BE1#
26	6	C/BE0#
28	5	DEVSEL#
30	4	STOP#
32	3	LOCK#
34	2	PERR#
36	1	SERR#
38	0	PAR

*This pin is unused and can be connected to any signal and assigned by the user in the Format menu.

LOGIC ANALYZER POD 4

Mictor-38 #2 Pin Number EVEN POD	Logic Analyzer channel number	PCI Signal name
5	CLK/16	TRDY#
7	15	USER7
9	14	USER6
11	13	USER5
13	12	USER4
15	11	USER3
17	10	USER2
19	9	USER1
21	8	SDONE
23	7	SBO#
25	6	C/BE7#
27	5	C/BE6#
29	4	C/BE5#
31	3	C/BE4#
33	2	PAR64
35	1	ACK64#
37	0	REQ64#

LOGIC ANALYZER POD 5

Mictor-38 #3 Pin Number ODD POD	Logic Analyzer channel number	PCI Signal name
6	CLK/16	unused*
8	15	AD47
10	14	AD46
12	13	AD45
14	12	AD44
16	11	AD43
18	10	AD42
20	9	AD41
22	8	AD40
24	7	AD39
26	6	AD38
28	5	AD37
30	4	AD36
32	3	AD35
34	2	AD34
36	1	AD33
38	0	AD32

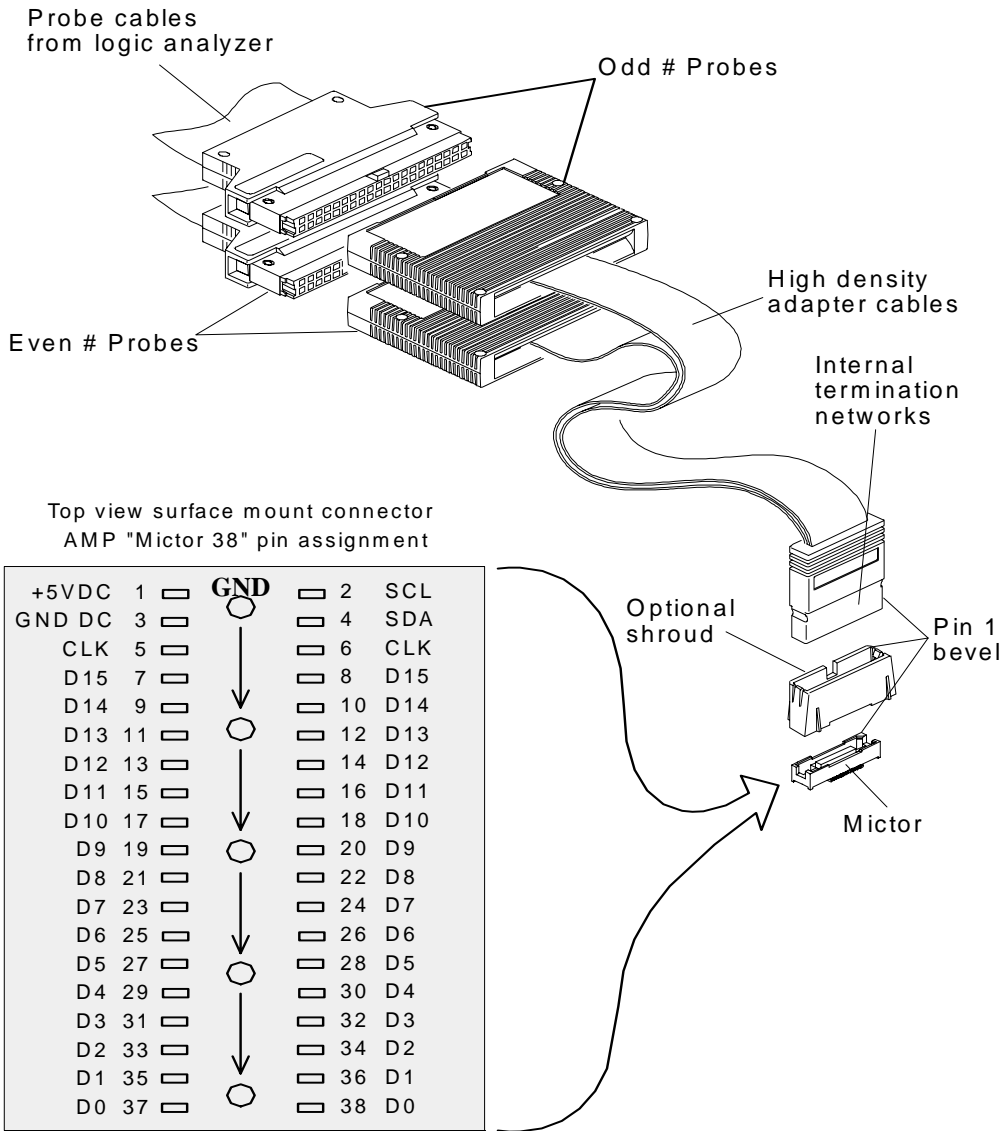
*This pin is unused and can be connected to any signal and assigned by the user in the Format menu.

LOGIC ANALYZER POD 6

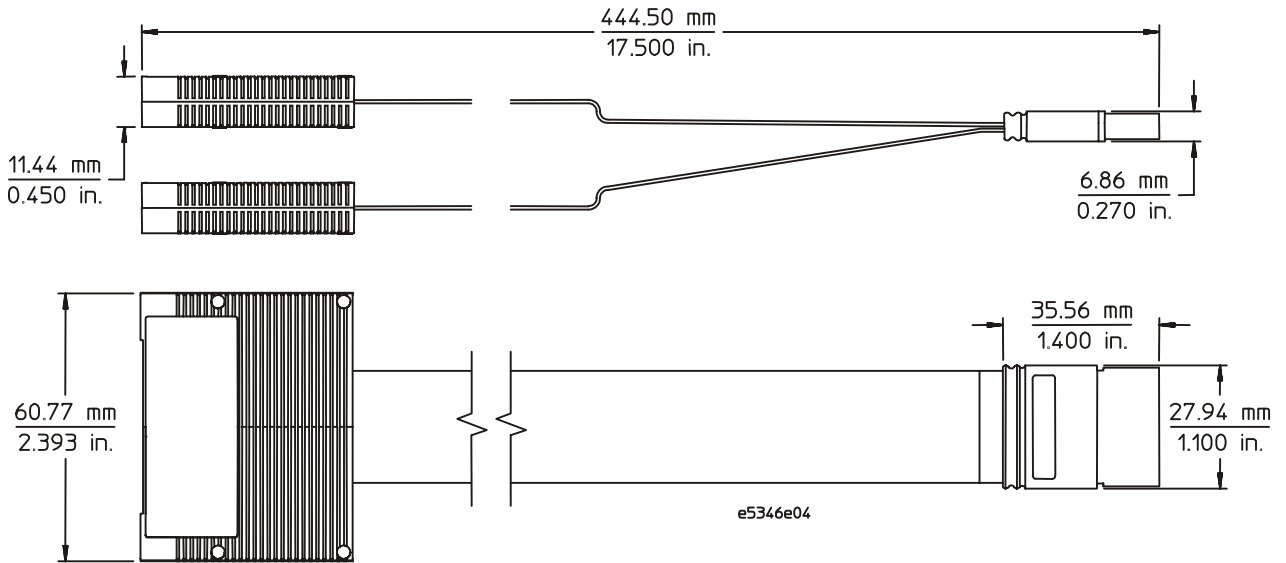
Mictor-38 #3 Pin Number EVEN POD	Logic Analyzer channel number	PCI Signal name
5	CLK/16	unused*
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48

*This pin is unused and can be connected to any signal and assigned by the user in the Format menu.

E5346A



E5346A/E5351A Mechanical Dimensions



AMP Mictor-38 Connector

