

The Bus Analyzer

AGP
ACCELERATED
GRAPHICS PORT

PCI
LOCAL BUS

SCSI

VXI
bus

USB

UNIVERSAL SERIAL BUS

DIMM, SIMM

ISA

Q4 '97

VME64

NEW MAIL ADDRESS

Please note the new address of our Colorado location, which appears in the center column. If you have need to correspond with us by postal mail, please change your records.

New Staff Members

If you have called our Colorado Springs office recently you have probably talked to our new sales and marketing assistant, Brenda Bergstrom. She comes from the state of Washington, where she completed a BA in Communications at Washington State University. Brenda is responsible for order management and literature request fulfillment and assists in other areas of sales and marketing. Brenda's outside interests include art appreciation, travel, skiing and competitive sports.

We have also recently hired an R&D Engineer, John Lenthall. John is a 10 year veteran of Digital Equipment Corporation. Prior to that John worked for British Aerospace in the UK. John has worked on development of both SW and HW architecture for Digital's PCI-VME interfaces. He was a contributor to the product definition of Alpha, StrongARM, CompactPCI, and VMEbus based products. He has worked on various projects related to network computing, embedded computing, bus bridges and system level debug. He is named co-inventor on 5 patents. John brings a wealth of HW design skills to FuturePlus, including ASIC and FPGA design experience. John lives in Nashua, NH and enjoys practicing and teaching Tai Chi Chaun in his spare time.

ABOUT THIS

NEWSLETTER

The Bus Analyzer is provided free by FuturePlus Systems Corporation to our customers and developers in the AGP, PCI, SCSI, VME, VXI and USB industries. FuturePlus Systems Corporation is a Value-Added Business Partner of the Hewlett-Packard Colorado Springs Division and provides easy-to-use state of the art test equipment to engineers and computer scientists around the globe. We can be reached at:

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FuturePlus Systems is a member of:
The PCI Special Interest Group
The USB Implementers Forum
The AGP Implementers Forum
HP Channel Partners (Premier Level)

INDUSTRY NEWS

DesignCon98

DesignCon98, sponsored by Hewlett-Packard, EDN, EETimes, and Integrated System Design, will be held January 26-29, 1998 at the Santa Clara Convention Center. FuturePlus Systems will be delivering technical papers on USB and CompactPCI, as well as demonstrating our new products at this conference. You may register at www.designcon.com or call 888 486-8736. Admission to the exhibits is free; the technical sessions cost \$250 to \$600 depending on how many you attend. Look us up at our booth and say hello!

FUTURE EVENTS

Begin planning now for the PC Developers' Expo at the San Jose Convention Center in San Jose, California, May 18-22, 1998. This is the big show of the year (it was called PCI Plus in 1997) for designers involved with computer buses. It is a little later this year than last year so make sure you get it scheduled.

TECHNICAL TRAINING

Want to get some good training on PCI or USB theory of operation? Visit www.annabooks.com for more information.

INSIDE

- ① AN IEEE-1394 PRIMER
- ② ANALYZING THE SCSI BUS
- ③ SOFTWARE UPDATES AVAILABLE
- ④ LITERATURE REQUEST FORM

A 1394 PRIMER

The IEEE 1394-1995 is a serial bus standard supporting 100 and 200 Mbits per second. Currently there are two supplements to the specification in progress, supplement A and supplement B. The provisions of supplement A include support for 100, 200 and 400 Mbits per second, Arbitration acceleration enhancements and resolution of some inter-operability issues from the 1394-1995 specification. Balloting on supplement A will occur shortly. Supplement B is still in definition but it is expected to support speeds up to 1 GBit per second. Both supplements will be backward compatible with 1394-1995 devices.

IEEE 1394 Summary:

The topology of the bus is a Tree (non-cyclic) where the basic unit is a node, which is an addressable entity that can be independently reset and identified. The network will include a root node (top of the tree) and all other nodes will be either a branch or leaf node. A branch node is a node which is connected to more than one other node and a leaf node is one that is connected to only one other node. Bus initialization consists of a Tree ID process and a Self ID process in which all nodes participate. All nodes must maintain a topology map. The standard supports both Asynchronous and Isochronous traffic. Peer to peer communication is supported and a node wishing to transmit a packet must Arbitrate for the bus at the appropriate time with the appropriate request. A device may be hot-plugged but this causes a Bus Initialization, which involves all nodes and all normal traffic is suspended until the Bus is reinitialized.

Electrically the 1394 Serial Bus uses two twisted pairs of signal wire, known as TPA and TPB. There is a single pair of wires that may be used to provide power to a node. The TPA and TPB pairs provide both differential and common mode signaling to allow for the recognition of a device attachment/detachment, automatic configuration, arbitration, speed signaling and packet transmission.

The TPA/TPA* pair transmits the Strb_Tx signal and receives the Data_Rx, Arb_A_Rx, and Speed_Rx signals. The TPB/TPB* pair transmits the Data_Tx and Speed_Tx signals and receives the Strb_Rx, Arb_B_Rx and Port_Status signals. There is a cross over of the pair between nodes, hence TPA of node 1 connects to TPB of node 2 and TPB of node 1 connects to TPA of node 2.

Protocol Architecture

The serial bus protocol is described as a set of three standard layers:

1. Transaction Layer
2. Link Layer
3. Physical Layer

1. Transaction Layer:

The Transaction Layer defines a complete Request/Response protocol to perform the bus transactions required to support the CSR Architecture.

2. Link Layer :

The Link layer provides an Acknowledge Datagram service to the Transaction layer.

- It provides Addressing, Data checking and framing for packet transmission and reception.
- It also provides an Isochronous data transfer service directly to the application. One link layer transfer is called a "subaction".
- It will generate the "Cycle" signal used for timing and synchronization of Isochronous traffic (only if this node is designated as Cycle master). Typically this layer is implemented in hardware.

3. Physical Layer:

The Physical Layer has three main functions.

- It translates the logical symbols used in the Link Layer into electrical signals on the differential Serial Bus media.
- It guarantees that only 1 node at a time is sending data by providing an arbitration service.
- It defines the mechanical interface for the Serial Bus. This layer is implemented in Hardware; the chip is usually called PHY.

The IEEE 1394 bus also known as Firewire provides an inexpensive interconnect strategy for a wide variety of applications. The applications that may be accommodated by the IEEE 1394 bus include video conferencing, video production, printers, entertainment and mass storage.

Monitoring the IEEE 1394:

The information required to construct an accurate picture of what is happening on this bus includes topology, arbitration, signaling speed, and packet type. Debug and compliance testing environment tools that monitor this bus will be very useful in shortening time to market for product development engineers. FuturePlus Systems Corporation is currently developing a product offering to fill these needs, and expects to introduce it in mid 1998.

NEW SOFTWARE AVAILABLE

New Inverse Assembler files are available for the **FS16P32E** and the **FS16P64** products. The changes are:

- * Bug fix for 64 bit transfers (FS16P64 only).
 - * Additional decode of the addresses 28h and 2Ch in PCI configuration space (FS16P32E and FS16P64).
- For your FREE update please e-mail your Preprocessor model number (FS16P32E or FS16P64) and serial number to tech_sup@futureplus.com. Please include your snail mail address and phone number. Due to licensing restrictions these files cannot be posted on the WEB. Also please indicate if you are a HP16505A user. An additional install diskette will be sent for use on the HP16505A.

For users of the **FSPCI64E**, two new configuration files are available for HP16555, HP16554 and HP16556. These files are posted on our WEB site and are for 64 bit demultiplex mode. They are the P64D_555 REV1.1 and the P64AD555 REV1.1. The changes are:

- *STOP bit assigned properly in the FORMAT menu.
- *REQ64 bit assigned properly in the FORMAT menu.

ANALYZING THE SCSI BUS

Hewlett-Packard has transferred their E2423A SCSI preprocessor to FuturePlus Systems. This product, now known as the FSSCSIA, is currently shipping. Connection to 50 pin low-density cables, 50 pin high-density cables, and 68 pin high-density cables are supported. Seven difference transaction inverse assemblers are also included. Any of the ten devices in SCSI ANSI X3.131-1994 are decoded by the Inverse Assemblers. The FSSCSIA requires two logic analyzer pods for state analysis and two for timing analysis. In fact, the FSSCSIA is unique in the industry in that it offers simultaneous state and timing analysis measurements.

The SCSI (Small Computer Systems Interface) standard has been evolving for years and is still changing as we speak. The FSSCSIA allows analysis of part of the current standard. We are also designing another product (FSSCSIB) that will support other parts of the standard. Whether we will support every part of the standard will be determined by our customers. The FSSCSIB will be introduced in the first quarter 1998.

Buzz words tend to make engineer's lives complicated, and SCSI is no different. There are many different terms being tossed around to describe the variations of the SCSI bus. Below is a table taken from the May 8, 1997 issue of EDN magazine, which describes the various versions of SCSI. We have added an additional

column to show which FuturePlus product will support which version.

Again quoting from the EDN article, "Ultra2 SCSI follows closely in the path of Ultra SCSI by taking its transfer capability and doubling it again, which allows for data-transfer rates of 80 Mbytes/sec max. on a Wide SCSI bus. But, because the existing single-ended and differential interfaces cannot support these transfer rates, a new interface standard is required."

"The SCSI committee adopted low-voltage differential (LVD) for just this purpose. The differential interface has long been known to have better electrical characteristics than do single-ended, but the requirement of external transceivers usually makes differential unpopular. LVD improves on what is now called "high-power differential: (HVD) by requiring lower voltage swings (60-mv differential receiver thresholds) and a 1.25 V common-mode biasing. These smaller voltage requirements allow the transceivers to be incorporated into the SCSI controller still using the low-cost CMOS technology, providing a differential solution that only slightly increases cost over single-ended."

"LVD signaling provides other electrical advantages that make configuring the SCSI bus more flexible. AN LVD bus can include the full 16 devices on a Wide SCSI bus and still achieve cable lengths of 12 meters - a significant advantage over the 1.5 meters allowed in fully

loaded, single-ended Ultra SCSI systems."

"Besides cost, another advantage of incorporating the LVD drivers into the controller's silicon is that LVD allows some backward compatibility to single-ended systems. This feature is commonly known as Universal LVD. The hardware detects legacy single-ended devices through the DiffSense signal and automatically switches the drivers to a single-ended configuration. Similarly, LVD is compatible with HVD, but external transceivers again become necessary. The only disadvantage to this backward compatibility is that systems that revert to single-ended or HVD are limited to the Ultra SCSI transfer rates."

"A few serial interfaces have partially evolved from SCSI. Fibre Channel and IEEE-1394 have SCSI as a common ancestor. In general, these standards try to apply some of the best features from the parallel interface to a serial one."

FuturePlus is currently designing a debug tool for users of the IEEE-1394, and is investigating a tool for Fibre Channel. The 1394 tool is expected to be introduced late in the first half of 1998. Stay tuned for announcements on Fibre Channel.

See also www.wcsita.com
(SCSI Trade Association) or
www.symbios.com/x3t10
(X3T10 Technical Committee).

Old Name	New Name	Defined In	SCSI Bus Width (Bits)	SCSI Maximum data-transfer rates (Mbytes/sec)	FuturePlus Product Support
Asynchronous	Asynchronous	SCSI - 1	8	5	FSSCSIA
Fast	Fast SCSI	SCSI - 2	8	10	FSSCSIA
Wide	Fast Wide SCSI	SCSI - 2	16	20	FSSCSIA
Fast - 20	Ultra SCSI	SCSI - 3	8	20	FSSCSIB
Wide Fast - 20	Wide Ultra SCSI	SCSI - 3	16	40	FSSCSIB
Fast - 40	Ultra 2 SCSI	SCSI - 3	8	40	FSSCSIB
Wide Fast - 40	Wide Ultra 2 SCSI	SCSI - 3	16	80	FSSCSIB

FuturePlus Systems Literature Request - Q4 '97

Please send me the following FREE information:

Technical Information

- _____ PCI Bus Compliance Testing - Paper presented at HP's *Design SuperCon '97*
- _____ USB Bus Compliance Testing - Paper presented at HP's *Design SuperCon '97*
- _____ Embedded PCI Test - Paper presented at HP's *Design SuperCon '96*
- _____ The PCI Compliance Checklist - Rev. 2.1 (3.5 in. diskette, WORD 6.0)
- _____ Back Issues Of *The Bus Analyzer*

Application Notes

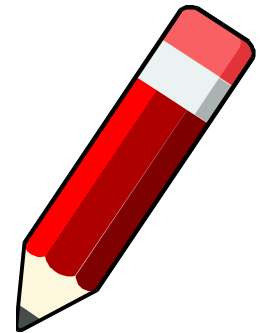
- _____ PCI Compliance Testing and Capturing PCI Bus Transactions With The FSPCI64E
- _____ Capturing PCI Bus Transactions With Passive PCI Preprocessors
- _____ Capturing USB Bus Transactions With The USB Preprocessor
- _____ Designing A Custom Connection To A 32-bit Embedded PCI Bus

NEW!

Product Literature

- _____ 32/64-bit PCI Bus Preprocessor - FS16P64
- _____ 32/64-bit PCI Bus Preprocessor and Extender - FSPCI64E-3,5
- _____ 32/64-bit PCI Bus LogicScope Preprocessor - FSPCI64LS
- _____ 32-bit PCI Bus Preprocessor and Extender - FS16P32E
- _____ 32-bit PCI Mezzanine Bus Preprocessor and Extender - FSPMC32E
- _____ 32-bit PCI CardBus Preprocessor and Extender - FSPCB32E
- _____ 32/64-bit CompactPCI Preprocessor and Extender - FSCPCI64E
- _____ 32-bit Accelerated Graphics Port Probe and Extender - FSAGP32TE
- _____ ISA Bus Preprocessor and Extender - FS16ISA
- _____ DIMM Probe and Extender - FSDIMPEA
- _____ SIMM Probe and Extender - FSSIMPE
- _____ Universal Serial Bus (USB) Preprocessor - FSUSB
- _____ 32/64-bit VME/VXI Bus Preprocessor and Extender - FSVME64E
- _____ SCSI Bus Preprocessor - FSSCSIA

NEW!



Mr. _____ Ms. _____ First Name: _____ Last Name _____

Company: _____ Mail Stop _____

Job Title: _____

Address: _____

City: _____ State: _____ Post Code _____ Country _____

Telephone: _____ FAX: _____

ADDRESS CORRECTION

_____ Please correct my address as shown above.

IEEE-1394

_____ Yes I am interested in a tool for this

Please FAX this completed form to : (719) 380-7362