

DisplayPort Preprocessor

For use with Tektronix Logic Analyzers

FuturePlus® Systems

Power Tools for Bus Analysis

- Low cost DisplayPort analysis
- Supports TLA7000-series logic analyzers
- Includes protocol-decode software, probe configuration software, and automatic logic analyzer setup software



FS4435 DisplayPort Preprocessor

Key Features

- Supports X1, X2, and X4 DisplayPort
- Data acquisition up to 2.7 GT/s
- Probe Manager software controls FS4435 via USB link and defines complex protocol aware filters for use with the logic analyzer
- Quad state LED's display instant port activity status
- Powerful Protocol Decode software decodes and displays Main Link and Auxiliary channel activity on the Tektronix logic analyzer
- Choose ½ size footprint, interposer, or flying leads adapter cables to connect FS4435 to your target system
- Probe Manager software allows instant lane reversal and polarity inversion

Straightforward, Reliable DisplayPort Analysis

The FuturePlus FS4435 DisplayPort Preprocessor provides a mechanical, electrical and software interface between a Tektronix logic analyzer and the DisplayPort, a digital display interface standard supported by the Video Electronics Standards Association (VESA). The FS4435 is used to design and debug computer motherboards, monitors, home theater systems, and silicon chips incorporating DisplayPort technology.



Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our preprocessors and software help you monitor and verify complex activities on your advanced-technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.

Tektronix

Embedded Systems
Tools Partner

Main Link Native Tektronix Disassembly

Sample	Timestamp	New Filter DisplayPort EventCode	New Filter DisplayPort Mnemonics
< 4896	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4897	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4898	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4899	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4900	3.625 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4901	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4902	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4903	3.625 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4904	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4905	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4906	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4907	3.625 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4908	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4909	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4910	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4911	3.750 ns	FO Pixel	Stuff Data Symbol
< 4912	3.625 ns	FO Pixel	P1020 R=166 G=202 B=240 P1021 R=166 G=202 B=240 P1022 R=166 G=202 B=240
< 4913	3.875 ns	BS	BS
< 4914	3.625 ns	Content Protection SR	CPSR
< 4915	3.750 ns	Content Protection SR	CPSR
< 4916	3.750 ns	BS	BS
< 4917	3.625 ns	Horizontal Blanking VBID	VB-ID = 0x10 VerticalBlanking_Flag = 0 FieldID_Flag = 0 Interlace_Flag = 0 NoVidStream_Flag = 0 AudioMute_Flag = 1 HDCP_Sync_Detect = 0 MvId = 60 Maud = 0 (No Audio)
< 4918	3.750 ns	Horizontal Blanking MVID	MVID = 0 (No Audio)
< 4919	3.750 ns	Horizontal Blanking MAUD	MAUD = 0 (No Audio)
< 4920	<929.250 us	Horizontal Blanking BE	Hor. Blanking End
< 4921	3.750 ns	FO Pixel	P0 R=10 G=36 B=106 P1 R=10 G=36 B=106 P2 R=10 G=36 B=106 P3 R=10 G=36 B=106
< 4922	3.625 ns	FO Pixel	
< 4923	3.875 ns	FO Pixel	
< 4924	3.625 ns	FO Pixel	
< 4925	3.750 ns	FO Pixel	
< 4926	3.625 ns	FO Pixel	P4 R=10 G=70 B=129 P5 R=169 G=168 B=188 P6 R=235 G=155 B=137 P7 R=235 G=155 B=137
< 4927	3.875 ns	FO Pixel	
< 4928	3.625 ns	FO Pixel	
< 4929	3.750 ns	FO Pixel	P8 R=236 G=87 B=139 P9 R=139 G=165 B=25 P10 R=119 G=174 B=40 P11 R=140 G=174 B=40
< 4930	3.625 ns	FO Pixel	
< 4931	3.750 ns	FO Pixel	
< 4932	3.750 ns	FO Pixel	P12 R=138 G=149 B=152 P13 R=57 G=149 B=152 P14 R=10 G=36 B=106 P15 R=10 G=36 B=106
< 4933	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4934	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4935	3.625 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4936	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4937	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4938	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4939	3.625 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4940	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol
< 4941	3.750 ns	FO Stuff Data Symbol (includ. FS/FE)	Stuff Data Symbol

Symbols such as Blanking Start and Content Protection Scrambler Reset appear often in DisplayPort traffic

Horizontal blanking indicator

The tool gives an index number to each pixel and identifies its color value

These event codes are handy for triggering and logic analyzer post processing

Pixel Data Display

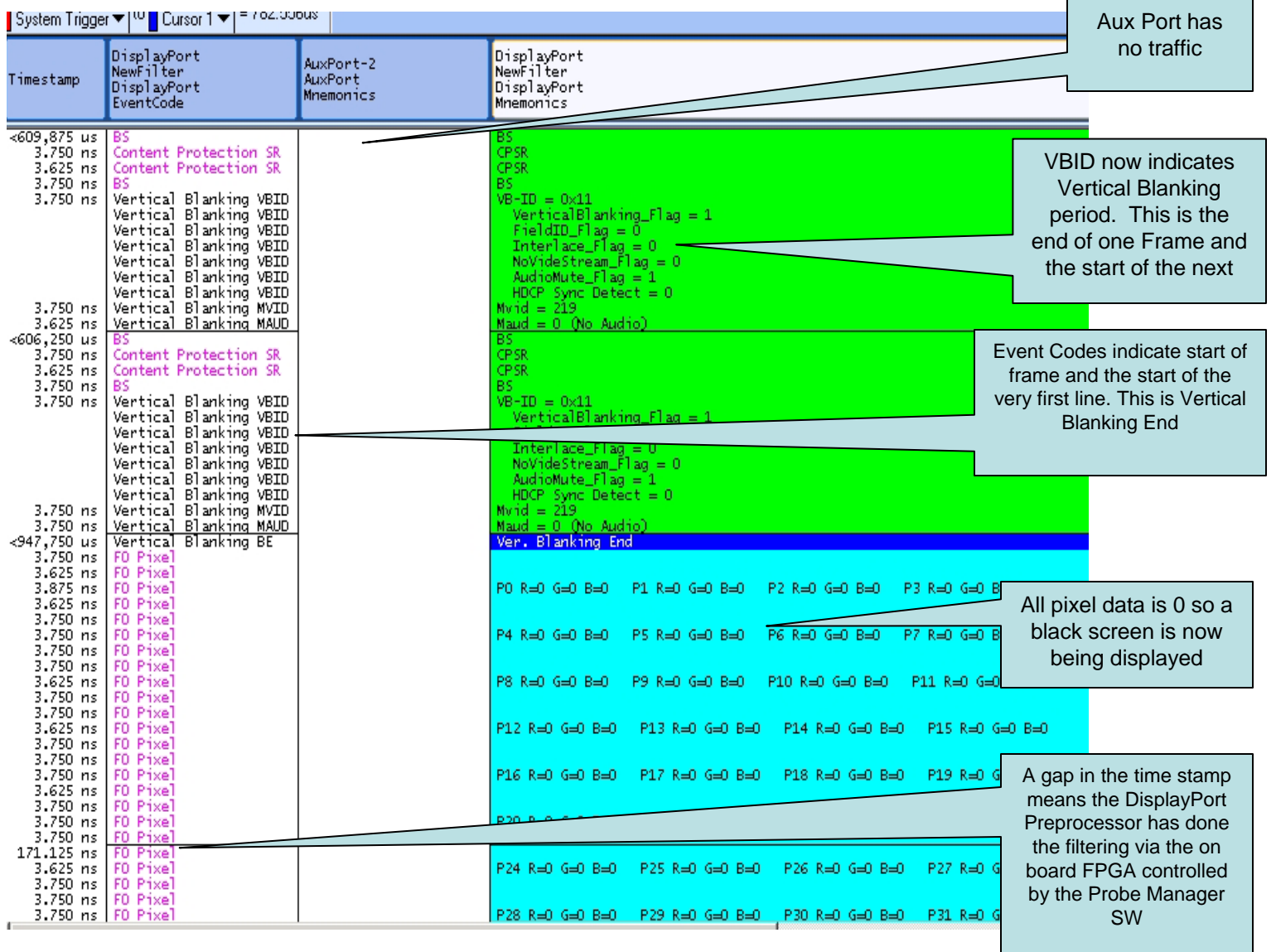
Sample	Di Ev	DisplayPort Mnemonics	Lane0_10bit	Lane1_10bit	Lane2_10bit	Lane3_10bit
<68812	>	Stuff Data Symbol	000	000	000	000
<68813	>	Stuff Data Symbol	000	000	000	000
<68814	>	Stuff Data Symbol	000	000	000	000
<68815	>	Stuff Data Symbol	000	000	000	000
<68816	>	Stuff Data Symbol	000	000	000	000
<68817	>	Stuff Data Symbol	000	000	000	000
<68818	>	Stuff Data Symbol	1F7	1F7	1F7	1F7
<68819	>	Stuff Data Symbol	09F	09F	09F	09F
<68820	>	P680 R=18 G=31 B=16 P681 R=18 G=31 B=16 P682 R=18 G=31 B=16 P683 R=18 G=31 B=16	040	040	040	040
<68821	>	Stuff Data Symbol	064	064	064	064
<68822	>	P684 R=6 G=18 B=31 P685 R=6 G=18 B=31 P686 R=6 G=18 B=31 P687 R=6 G=18 B=31	09F	09F	09F	09F
<68823	>	Stuff Data Symbol	040	040	040	040
<68824	>	Stuff Data Symbol	064	064	064	064
<68825	>	P688 R=16 G=6 B=18 P689 R=16 G=6 B=18 P690 R=16 G=6 B=18 P691 R=16 G=6 B=18	09F	09F	09F	09F
<68826	>	Stuff Data Symbol	040	040	040	040
<68827	>	P692 R=31 G=16 B=6 P693 R=31 G=16 B=6 P694 R=31 G=16 B=6 P695 R=31 G=16 B=6	064	064	064	064
<68828	>	Stuff Data Symbol	09F	09F	09F	09F
<68829	>	P696 R=18 G=31 B=16 P697 R=18 G=31 B=16 P698 R=18 G=31 B=16 P699 R=18 G=31 B=16	040	040	040	040
<68830	>	Stuff Data Symbol	064	064	064	064
<68831	>	Stuff Data Symbol	1FE	1FE	1FE	1FE
<68832	>	Stuff Data Symbol	000	000	000	000
<68833	>	Stuff Data Symbol	000	000	000	000
<68834	>	Stuff Data Symbol	000	000	000	000
<68835	>	Stuff Data Symbol	000	000	000	000
<68836	>	Stuff Data Symbol	000	000	000	000
<68837	>	Stuff Data Symbol	000	000	000	000
<68838	>	Stuff Data Symbol	000	000	000	000
<68839	>	Stuff Data Symbol	000	000	000	000
<68840	>	Stuff Data Symbol	000	000	000	000
<68841	>	Stuff Data Symbol	000	000	000	000
<68842	>	Stuff Data Symbol	000	000	000	000
<68843	>	Stuff Data Symbol	000	000	000	000
<68844	>	Stuff Data Symbol	000	000	000	000
<68845	>	Stuff Data Symbol	000	000	000	000
<68846	>	Stuff Data Symbol	000	000	000	000
<68847	>	Stuff Data Symbol	000	000	000	000
<68848	>	Stuff Data Symbol	000	000	000	000
<68849	>	Stuff Data Symbol	000	000	000	000
<68850	>	Stuff Data Symbol	000	000	000	000
<68851	>	Stuff Data Symbol	000	000	000	000
<68852	>	Stuff Data Symbol	000	000	000	000

The preprocessor verifies that all lanes carry the same data when the protocol requires it

Pixels are given an index number within a frame

Stuff Data Symbols only appear when filtering is disabled

Cross bus display, both AuxPort and Main Link



Aux Port has no traffic

VBIID now indicates Vertical Blanking period. This is the end of one Frame and the start of the next

Event Codes indicate start of frame and the start of the very first line. This is Vertical Blanking End

All pixel data is 0 so a black screen is now being displayed

A gap in the time stamp means the DisplayPort Preprocessor has done the filtering via the on board FPGA controlled by the Probe Manager SW

Auxiliary Port Protocol Analysis

Aux Port is a bidirectional half duplex 1Mb/sec communication channel

Sample	AuxPort Address	AuxPort Data	AuxPort Mnemonics	AuxPort Status	Byte_Count	Storage	HPD Even	Timestamp
0	00001	00	AUX Read request, Address = 00001 Byte Count = 01	7	00100	1	11	0 ps
1	00000	0A	Aux ACK	7	00010	1	11	<00,250 us
2	00002	00	AUX Read request, Address = 00002 Byte Count = 01	7	00100	1	11	
3	00000	84	Aux ACK	7	00010	1	11	
3	00000	84	Max link rate= 2.7Gbps	7	00010	1	11	
3	00000	84	Enhanced Frame cap = 1	7	00010	1	11	
4	00600	00	AUX Read request, Address = 00600 Byte Count = 01	7	00100	1	11	
5	00000	01	Aux ACK	7	00010	1	11	
5	00000	01	SET POWER	7	00010	1	11	
5	00000	01	Set Power sink ctrl(DPCD ver.1.1) = D0 Normal operation	7	00010	1	11	
6	00600	00	AUX Write request, Address = 00600 Byte Count = 01	6	00100	1	11	
7	00600	01	SET POWER	3	00101	1	11	
7	00600	01	Set Power sink ctrl(DPCD ver.1.1) = D0 Normal operation	3	00101	1	11	
8	00000	00	Aux ACK All Data bytes written	7	00001	1	11	
9	00206	00	AUX Read request, Address = 00206 Byte Count = 01	7	00100	1	11	
10	00000	88	Aux ACK	7	00010	1	11	<00,375 us
10	00000	88	VOLTAGE SWING AND EQUALIZATION SETTINGS	7	00010	1	11	
10	00000	88	Voltage Swing lane0 = Level 0	7	00010	1	11	
10	00000	88	Pre-emphasis lane0 = Level 2	7	00010	1	11	
10	00000	88	Voltage swing lane1 = Level 0	7	00010	1	11	
10	00000	88	Pre-emphasis lane1 = Level 2	7	00010	1	11	
11	00207	00	AUX Read request, Address = 00207 Byte Count = 01	7	00100	1	11	<00,375 us
12	00000	88	Aux ACK	7	00010	1	11	
12	00000	88	VOLTAGE SWING AND EQUALIZATION SETTINGS	7	00010	1	11	
12	00000	88	Voltage Swing lane2 = Level 0	7	00010	1	11	
12	00000	88	Pre-emphasis lane2 = Level 2	7	00010	1	11	
12	00000	88	Voltage swing lane3 = Level 0	7	00010	1	11	
12	00000	88	Pre-emphasis lane3 = Level 2	7	00010	1	11	
13	00002	00	AUX Read request, Address = 00002 Byte Count = 01	7	00100	1	11	<03,000 ms
14	00000	84	Aux ACK	7	00010	1	11	<00,375 us
14	00000	84	Max lane count = 4 lanes	7	00010	1	11	
14	00000	84	Enhanced Frame cap = 1	7	00010	1	11	
15	00101	00	AUX Read request, Address = 00101 Byte Count = 01	7	00100	1	11	<00,500 us
16	00000	84	Aux ACK	7	00010	1	11	<00,375 us
16	00000	84	LANE COUNT SET	7	00010	1	11	
16	00000	84	Lane count set = 4	7	00010	1	11	
16	00000	84	Enhanced frame enable(version 1.1)= enabled	7	00010	1	11	
17	00101	00	AUX Write request, Address = 00101 Byte Count = 01	6	00100	1	11	<00,375 us
18	00101	84	LANE COUNT SET	3	00101	1	11	<00,000 us
18	00101	84	Lane count set = 4	3	00101	1	11	
18	00101	84	Enhanced frame enable(version 1.1)= enabled	3	00101	1	11	
19	00000	00	Aux ACK All Data bytes written	7	00001	1	11	
20	00100	00	AUX Write request, Address = 00100 Byte Count = 01	6	00100	1	11	
21	00100	0A	LINK BANDWIDTH SET	3	00101	1	11	<00,125 us
21	00100	0A	Link BW set = 2,7 Gbps per lane	3	00101	1	11	
22	00000	00	Aux ACK All Data bytes written	7	00001	1	11	<00,125 us
23	00101	00	AUX Read request, Address = 00101 Byte Count = 01	7	00100	1	11	<00,500 us
24	00000	84	Aux ACK	7	00010	1	11	<00,375 us
24	00000	84	LANE COUNT SET	7	00010	1	11	
24	00000	84	Lane count set = 4	7	00010	1	11	

The serial data is deserialized into a 48 bit wide bus and clocked to the logic analyzer. This wide bus makes triggering easy

Aux Port communicates configuration data between the monitor and the host PC

Diagnostic mode information is also communicated over the Aux Port

Ordering Information

FS4435 – DisplayPort Preprocessor for use with Tektronix Logic Analyzers

One of the following is required to connect the FS4435 to the target system:

FS1032 – ½ Midbus footprint Cable Adapter

FS1036 – Flying Leads Cable Adapter

FS1040 – Interposer Cable Adapter

Four of the following are required to connect the FS4435 to the logic analyzer:

FS1055 – TLA7Axx / TLA7Bxx Full Channel Probe Cable

Software included:

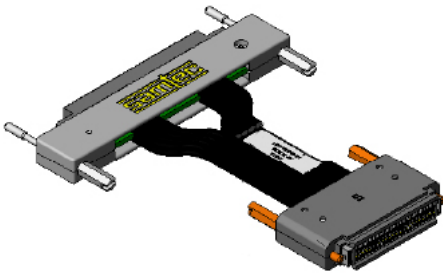
Probe Manager, runs on a PC or the logic analyzer

Setup files for the Tektronix logic analyzer

Protocol Decoder software, runs on the Tektronix logic analyzer

Logic Analyzer Requirements

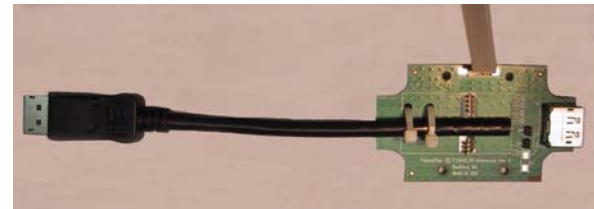
- 68 channels required for X1-X4 Main Link, 270 MHz state acquisition.
- 68 channels required for Aux Data, 100 KHz state acquisition.
- The Tektronix logic analyzer connects to the FS4435 with four FS1055 Probe Cables.



FS1032 ½ Size Midbus
Cable Adapter



FS1036 Flying Leads
Cable Adapter



FS1040 Interposer
Cable Adapter

FuturePlus Systems Corporation

6455 N. Union Blvd. Suite 202
Colorado Springs, CO 80918-5844
Tel: 719 278 3540
Fax: 719 278-9586
Website: www.futureplus.com

Represented By: