

## **USB** **Universal Serial Bus Analyzer**

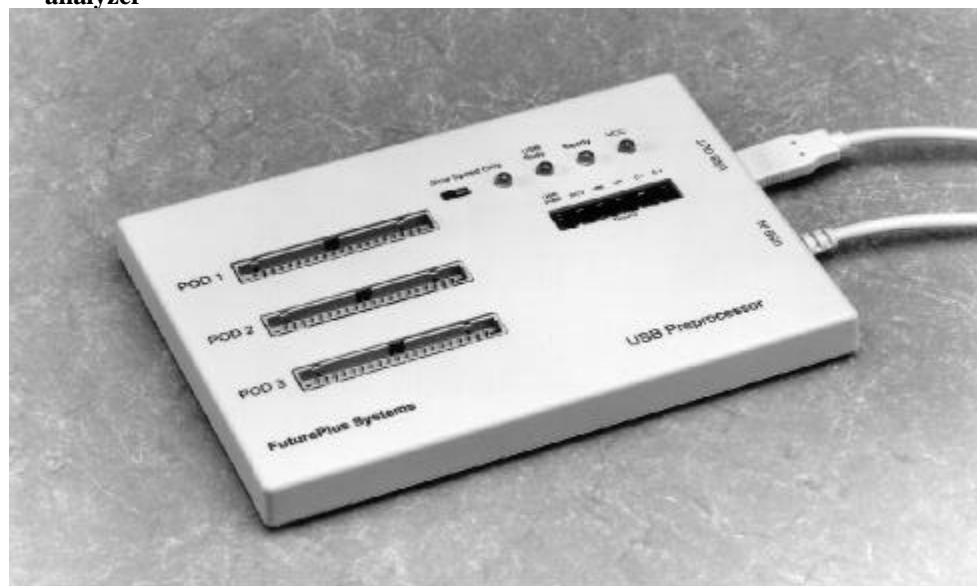
For use with Agilent Logic Analyzers

### **UNIVERSAL SERIAL BUS**

With this versatile product, designers can use their Agilent logic analyzer as a passive USB analyzer. The FuturePlus® protocol-sensitive logic and USB Transaction Inverse Assembler, coupled with the advanced triggering and system performance software of Agilent's logic analyzers, give the user a powerful tool in debugging, testing, and verifying compliance of USB peripherals and USB-based systems.

### Features

- Complete USB serial to parallel decode
- Automatic detection and operation at high-speed (12Mbits/s) or low-speed (1.5Mbits/s), including dynamic speed changing
- Automatic USB reset detection and dynamic hot swapping
- Address and end point specified in token packet held until transfer completes
- Allows for easy triggering, store qualification and performance monitoring of specific address and end points
- Complete configuration files and USB Transaction Inverse Assembler supplied for your Agilent logic analyzer
- Supports the full USB specification and decodes all Chapter 9 commands
- Supports all types of data transfers, including isochronous transfers
- Detects the following errors on all packet types: bad PID, invalid PID, serial bit stuffed error, CRC error, Start of Frame tokens sent at slow speed
- Error summary code triggers on the occurrence of any one of the above errors
- Possible End Of Packet protocol violations detected
- The FS4100, combined with Agilent's SPA software, enhanced triggering and cross-domain analysis gives the user complete system and USB performance monitoring



**FS4100**  
**Universal Serial Bus**  
**Analyzer**

## USB Analysis Probe Description:

The USB analysis probe provides two functions:

- 1) Provides an **electrical and mechanical interface** from the Universal Serial Bus to Agilent logic analyzers for passive bus analysis.
- 2) Provides **test points to measure the power and signal fidelity** of the USB bus.

### **State Analysis Mode**

The software included with the FS4100 contains complete configuration files and a FuturePlus USB Transaction Inverse Assembler for your Agilent logic analyzer. In **State Analysis** mode, the analyzer master clock is derived from the USB Protocol. The USB serial data is converted to parallel data in the analysis probe regardless of high or low speed operation. Any USB resets are automatically detected. Since the address and end point specified in the token packet are held until the transfer is complete, triggering, store qualification and performance monitoring of specific end point addresses is easy!

The enhanced triggering capabilities of your Agilent logic analyzer allow you to trigger on: (1) any address and end point, (2) any data pattern, (3) any data CRC, (4) any USB error (CRC fail, serial bit stuff error, and missing frames), (5) bad or invalid PID's, or any combination of these.

Store qualifiers allow the user to store any combination of: (1) any address and end point, (2) any data pattern, (3) any data CRC, (4) any PID type, or any combination of these.

All USB cycles and transaction identifiers (SOF, OUT, IN, SETUP, DATA0, DATA1, ACK, NAK, STALL, and PRE) are decoded by protocol-sensitive clocking logic and presented as separate bits to the logic analyzer. These packet identifiers will allow the user to: (1) store all USB traffic, (2) store only certain packet types, (3) store only packets to and from a certain function. The FuturePlus Transaction Inverse Assembler makes analyzing the resulting stored USB traffic easy and accurate. Another good feature: the electrical power for the FS4100 circuitry is drawn from the logic analyzer, not your USB bus!

### **Timing Analysis Mode**

The USB Analysis Probe has a third pod dedicated to **timing analysis** of the USB serial bit stream. The FS4100 in timing mode provides a unique state by state view of the USB serial interface engine (SIE). This mode allows for:

- Shadowing the state of the target USB SIE when that SIE state is unavailable
- Comparing the state of the target USB SIE with that of the FS4100 SIE
- Making accurate timing measurements of USB events
- Accurate USB protocol violation detection
- Accurate USB signaling violation detection.

### **Signals on Pod 3:**

<u>Signal Name</u>	<u>Description</u>
CLK 12	Recovered Clock
MDATA	Recovered Serial Data
SOFTIC	Start of Frame. 1 ms timer generated from recovered start of frame
EOP2_0	End of Packet state machine
LBC3_0	Load Byte Count State Machine
FEOPR	End of Packet
FEOSYN	End of Sync
LSDET	Low Speed Detect

### **Cross-Domain Analysis**

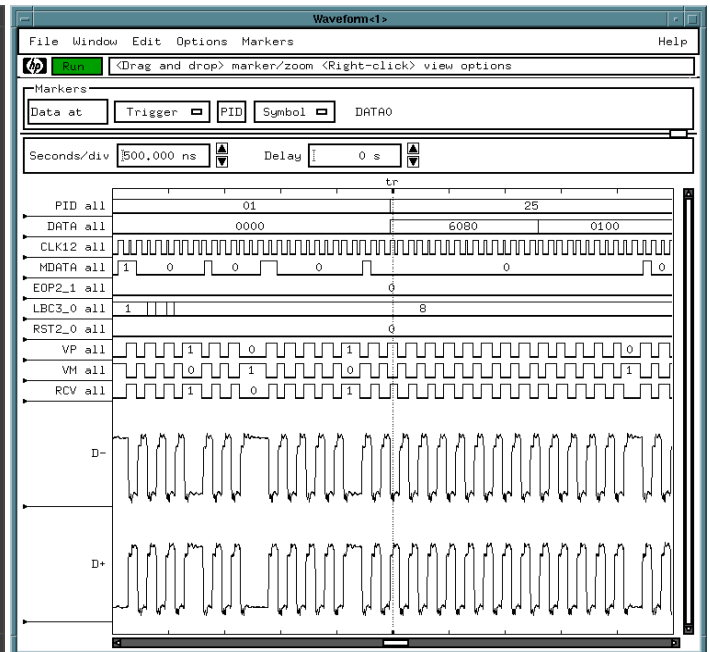
Are you analyzing data in multiple domains? Simply use this analysis probe to monitor the USB, and then use another FuturePlus Systems analysis probe to monitor your other bus. We have analysis probes for the AGP, PCI, ISA, VME, VXI, PMC, DIMM and SIMM buses. You can create your own custom measurement system, cross-domain trigger between buses, and view data from multiple buses simultaneously in the same display. In a similar fashion, you could connect an analysis probe for your host processor to another logic analyzer card. You could then use Agilent's Software Analyzer (B4620A) to view source code, code execution, and the corresponding USB packet transfers simultaneously.

## State Analysis

State Number	Time	FUTUREPLUS SYSTEMS c 1997	PID
Decimal	Relative	USB BUS TRANSACTIONS REV 1.1	Symbol
-1	999.752 us	SOF FRAME=022	SOF
0	3.248 us	SETUP ADDR=00 END_POINT=0	SETUP
1	3.920 us	GET_DESCRIPTOR Direction=Device to Host Type=Standard Recipient=Device	DATA0
2	1.336 us	Descriptor Type= Device	DATA0
3	1.352 us	wIndex=0000	DATA0
4	1.312 us	Length=0012	DATA0
5	768.000 ns	DATA CRC=072F	CRC DATA
6	1.752 us	ACKNOWLEDGE	ACK
7	986.064 us	SOF FRAME=023	SOF
8	3.248 us	IN ADDR=00 END_POINT=0	IN
9	2.016 us	NO ACKNOWLEDGE	NCK
10	994.480 us	SOF FRAME=024	SOF
11	3.248 us	IN ADDR=00 END_POINT=0	IN
12	4.024 us	DATA1= 0112	DATA1
13	1.336 us	DATA1= 0100	DATA1
14	1.312 us	DATA1= 0000	DATA1
15	1.328 us	DATA1= 0800	DATA1
16	752.000 ns	DATA CRC=C8E7	CRC DATA
17	2.000 us	ACKNOWLEDGE	ACK
18	985.752 us	SOF FRAME=025	SOF
19	999.752 us	SOF FRAME=026	SOF
20	3.248 us	OUT ADDR=00 END_POINT=0	OUT
21	3.328 us	DATA CRC=0000	CRC DATA

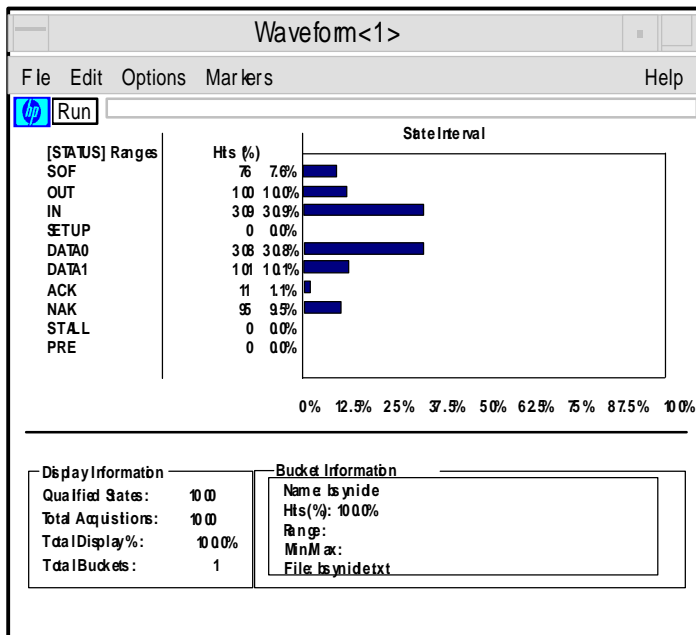
An easy-to-read, well organized state transaction listing shows you all the information you need to solve complex hardware and software problems on your Universal Serial Bus.

## Timing Analysis



Timing analysis capabilities allow you to easily see and analyze both the analog and digital data in the serial bit stream.

## System Performance Analysis



The USB Analysis Probe and Agilent's System Performance Analysis software turn your Agilent logic analyzer into a powerful USB system performance monitor.

## USB to PCI Cross Domain Analysis

USB:FUTUREPLUS SYSTEMS c 1997	PCI_BUS1:FUTUREPLUS SYSTEMS c 1996	Time	PCI_BUS1:CALPER
USB BUS TRANSACTIONS REV 1.1	PCI BUS - PC MAPPER REV 1.2	Absolute	Symbol
MEM READ ADR=00FCA48C		3,008 ms	No Parity Error
D32=00000000		3,008 ms	No Parity Error
IDLE		3,008 ms	No Parity Error
DATA0= 6159		3,011 ms	
DATA0= 6662		3,012 ms	
DATA0= 6F6A		3,014 ms	
DATA0= 7B78		3,015 ms	
DATA0= 8781		3,016 ms	
DATA0= 8F89		3,018 ms	
DATA0= 9491		3,019 ms	
DATA0= ACA2		3,020 ms	
DATA0= 2322		3,022 ms	
DATA0= 2226		3,023 ms	
DATA0= 231F		3,024 ms	
DATA0= 2221		3,026 ms	
DATA0= 2124		3,027 ms	
DATA0= 211F		3,028 ms	
DATA0= 2422		3,030 ms	
DATA0= 2324		3,031 ms	
SYSTEM MEMORY		3,031 ms	No Parity Error
MEM WRITE ADR=003C96C0		3,032 ms	No Parity Error
D32=66626159		3,032 ms	No Parity Error
D32=7B786F6A		3,032 ms	No Parity Error
D32=8F898781		3,032 ms	No Parity Error
D32=ACA29491		3,032 ms	No Parity Error
D32=22262322		3,032 ms	No Parity Error
D32=2221231F		3,032 ms	No Parity Error
D32=211F2124		3,032 ms	No Parity Error
D32=23242422	STOPW	3,032 ms	No Parity Error
IDLE		3,032 ms	No Parity Error
IDLE		3,032 ms	No Parity Error
DATA0= 261F		3,032 ms	
DATA0= 2826		3,034 ms	

This listing displays isochronous transfers from the USB to the PCI bus through the Intel UHCI bridge chip. Note that the PCI bridge asserts stop after 32 bytes and the USB has 64 bytes to transfer.

## Ordering Information

**FS4100.....Universal Serial Bus 1.1 Analysis Probe for use with Agilent Logic Analyzers**

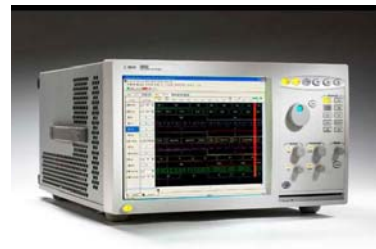
**Software included with the FS4100:**

Configuration files for the Agilent logic analyzer

Protocol Decoder software, runs on the Agilent logic analyzer

1. The FS4100 supports 16700, 1680, 16800, and 16900 40 pin logic analyzer modules
2. For protocol decode, the FS4100 requires 2 logic analyzer pods.
3. For timing analysis of the serial bit stream, an additional pod is required.
4. The FS4100 does not require Termination Adapters.
5. A logic analyzer pod has 17 channels

Please note: for the most up-to-date information about Agilent logic analyzer compatibility, please check the FuturePlus Systems website at:  
[http://www.futureplus.com/products/fs4100/fs4100\\_sysreq9.shtml](http://www.futureplus.com/products/fs4100/fs4100_sysreq9.shtml)



**We offer excellent technical support and quick delivery.**

More information and application notes are on the FuturePlus Systems website at:  
<http://www.futureplus.com/products/fs4100>

**FuturePlus Systems  
Corporation**

6455 N. Union Blvd. Suite 202  
Colorado Springs, CO 80918-5844  
Tel: 719 278 3540  
Fax: 719 278-9586  
Website: [www.futureplus.com](http://www.futureplus.com)

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