

# Extended IO Analysis Probe and Interposer

For use with Agilent Logic Analyzers

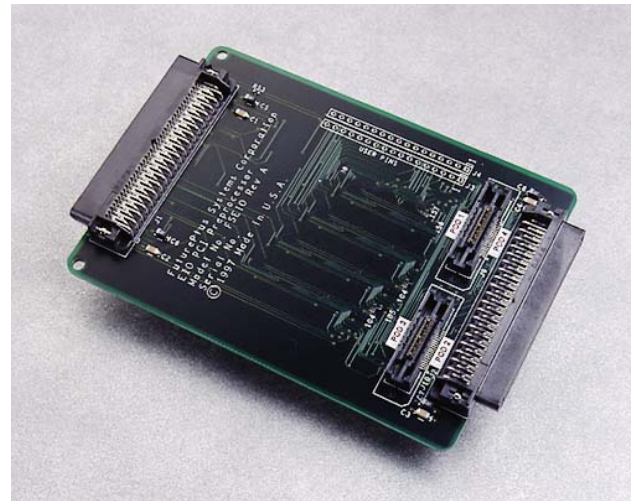
FuturePlus® Systems

Power Tools for Bus Analysis

## Straightforward, Reliable CardBus Analysis

The FS3030 Extended IO (EIO) Analysis Probe provides an electrical and mechanical interface to Agilent logic analyzers for passive EIO bus analysis. In State Analysis mode, the bus protocol decode software executes in the Agilent logic analyzer and decodes the key EIO signals.

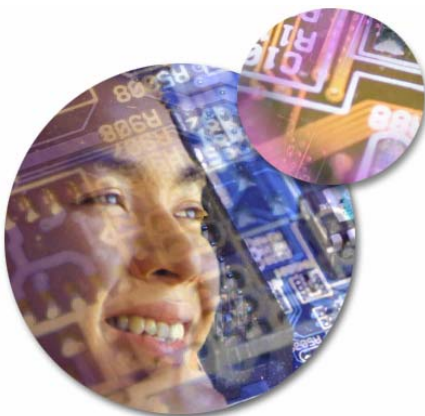
A readable display is presented that lists the transaction type, address, data and address modifiers. The software also supports user-defined symbols that can be easily added to the state listing display. To assist with triggering, pre-defined resource terms have been included.



FS3030 Extended IO Analysis Probe and Interposer

## Key Features

- Reliable and accurate 32-bit EIO bus monitoring
- Complete State Analysis to 66 MHz
- Timing Analysis to 500 MHz
- Logic Analyzer Configuration Software gets you up and running fast
- EIO bus protocol decode software executes in your Agilent logic analyzer
- No need for flying leads or termination adapters
- EIO module under test extends beyond the host board for easy debug
- Passive buffering of signals provides accurate Timing Analysis
- Post-Processing filters are supported with the Agilent logic analyzers



### Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our analysis probes and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit [www.futureplus.com](http://www.futureplus.com) for more information.



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## General Description

The EIO analysis probe and extender card provides three functions:

1) Acts as an extender for a EIO module beyond the host board front panel, and provides access to both sides for easy debug. Pads are available to add series resistors if necessary to compensate for the extension of your card.

2) Provides an electrical and mechanical interface to Agilent logic analyzers for passive EIO bus analysis. The passive logic analyzer termination presents a single electrical load on the EIO bus via low capacitance (10 pf), high impedance terminators, and also provides a matched impedance to the logic analyzer. The analysis probe includes four, 40 pin logic analyzer connectors.

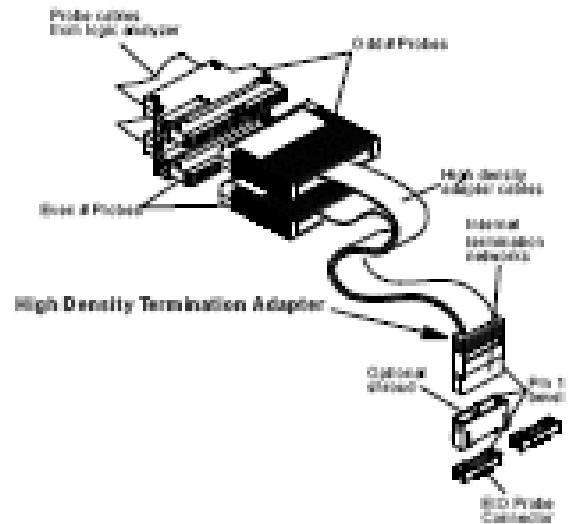
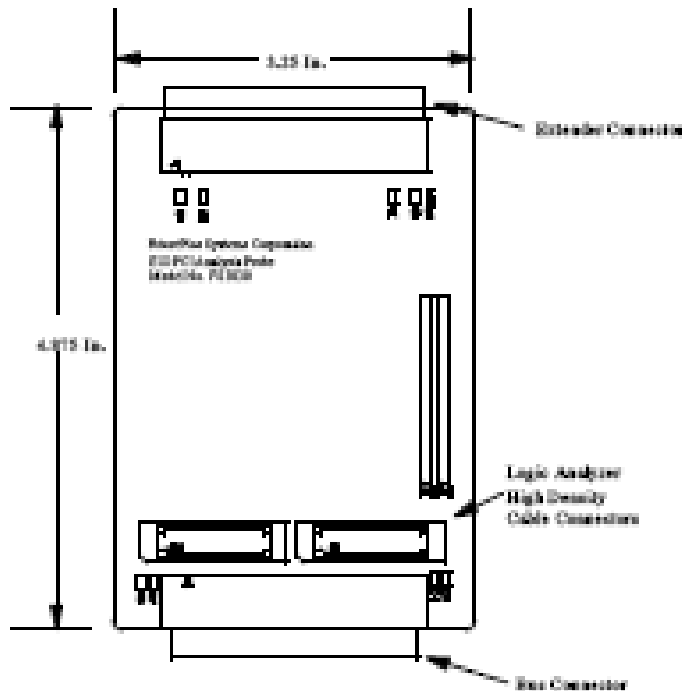
3) Provides test points to measure the power and signal fidelity of the EIO bus.

The EIO protocol decode software executes in your Agilent logic analyzer. In State Analysis mode, the analyzer master clock is derived from the EIO clock. The bus decoder software decodes the key EIO bus signals and presents a readable display that lists the transaction type, address, data, and key status conditions, such as wait states and retries. The software also supports user-defined symbols that can be easily added to the state listing display. The user can also select post-processing filters which allow the acquired data to display only chosen transactions.

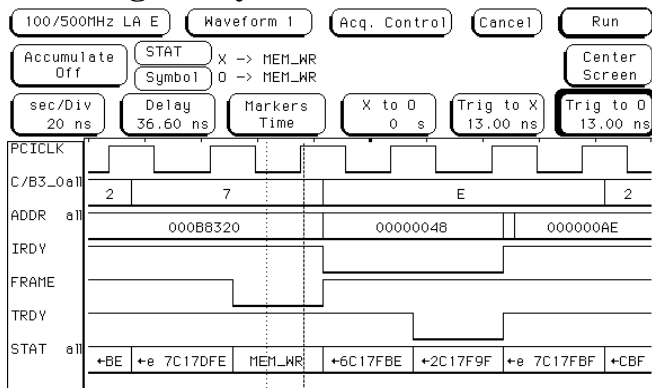
To assist with triggering, pre-defined resource terms have been included that can be used to prevent WAIT and IDLE states from being acquired, thus saving trace memory and providing an easier-to-read state display. FuturePlus Systems also provides a PCI bus triggering application note.

In Timing Analysis mode, the logic analyzer provides the master clock to make precision timing measurements. All signals are also available for probing with an oscilloscope or high speed timing analyzer.

## FS3030 Drawing

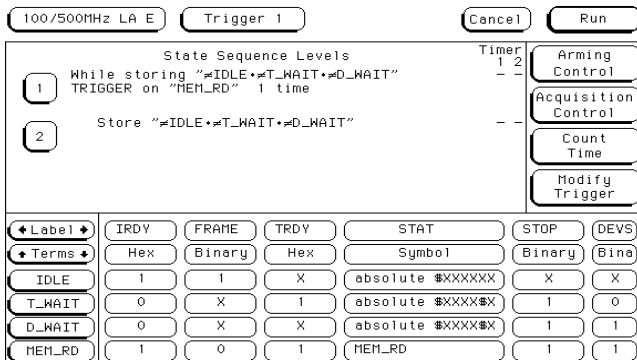
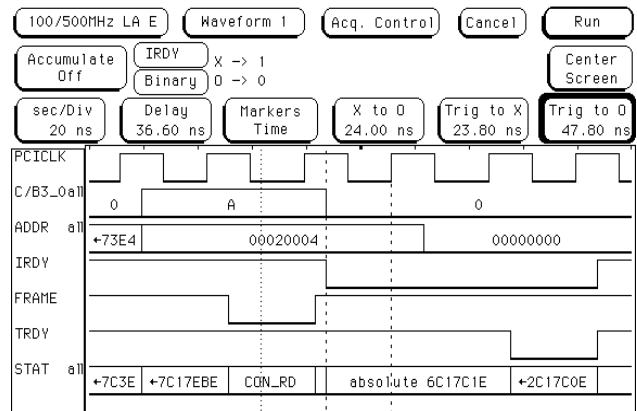


## Timing Analysis



Matched signal length, low capacitive loading, and no active buffering of the EIO signals makes the FS3030 ideal for accurate and easy timing analysis.

The EIO analysis probe software contains pre-defined trigger terms that help track down those hard to find bugs.



## State Analysis

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
242	D32=xxxxxxxx08	296 ns
243	I/O READ ADR=00000073	9.072 us
244	D32=23xxxxxx	1.096 us
245	I/O WRITE ADR=00000020	10.97 us
246	D32=xxxxxxxx20	168 ns
247	INTERRUPT ACK CYCLE	54.90 ms
248	D32=xxxxxxxx08	296 ns
249	I/O READ ADR=00000073	9.904 us
250	D32=23xxxxxx	1.128 us
251	I/O WRITE ADR=00000020	10.97 us
252	D32=xxxxxxxx20	168 ns

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
950	CONFIG READ ADR=80000000	8.960 ms
963	DEVICE ID=4158 VENDOR ID=1002	360.1 us
964	IDLE	32 ns
965	CONFIG READ ADR=0008000C	27.00 us
966	BIST=00 Hdr_Typ=00 Lat_Tmr=00 CLS=00	264 ns
967	IDLE	32 ns
968	CONFIG READ ADR=00080008	31.40 us
969	CLASS CODES:03 00 00 REV ID=00	264 ns
970	IDLE	40 ns

EIO Bus transaction inverse assembly options post-process the acquired data. This feature allows the user to customize the display to show only the transactions or cycles that are of interest.

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
12	MEM READ ADR=000FE060	264 ns
13	D32=A5837102	3.608 us
14	MEM READ ADR=000FE064	200 ns
15	D32=A6A6C5A5	3.536 us
16	MEM READ ADR=000FE068	296 ns
17	D32=B6C54471	3.568 us
18	MEM READ ADR=000FE06C	200 ns
19	D32=A6B566F5	3.536 us
20	MEM READ ADR=000FE070	304 ns
21	D32=A5560471	3.560 us
22	MEM READ ADR=000FE074	200 ns

## PCI Bus Inverse Assembly Options

- Wait Cycles:
- I/O Reads:
- I/O Writes:
- Configuration Reads:
- Configuration Writes:
- Memory Reads:
- Memory Writes:
- Idle Cycles:
- All Other Transactions:

## Ordering Information

### FS3030 EIO Analysis Probe and Extender Card

E5346A – 2 ea required, available from Agilent Technologies

#### Software included with the FS3030:

Configuration files for the Agilent logic analyzer

Protocol Decoder software, runs on the Agilent logic analyzer

### Logic Analyzer Requirements

The FS3030 supports all Agilent 1670, 16700, 1680, 1690, 16800 and 16900-series Logic Analyzers that have 40 pin connectors. Pod requirements are listed below:

For 32-bit protocol or timing analysis, the FS3030 requires 4 40-pin 33 MHz logic analyzer pods



Please note: for the most up-to-date information about Agilent logic analyzer compatibility, please check the FuturePlus Systems website at:  
[http://www.futureplus.com/products/fs3030/fs3030\\_sysreq9.shtml](http://www.futureplus.com/products/fs3030/fs3030_sysreq9.shtml)

**We offer excellent technical support and quick delivery.**

More information and application notes are on the FuturePlus Systems website at:  
<http://www.futureplus.com/products/fs3030>

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