

CompactPCI Analysis Probe and Interposer

For use with Agilent Logic Analyzers

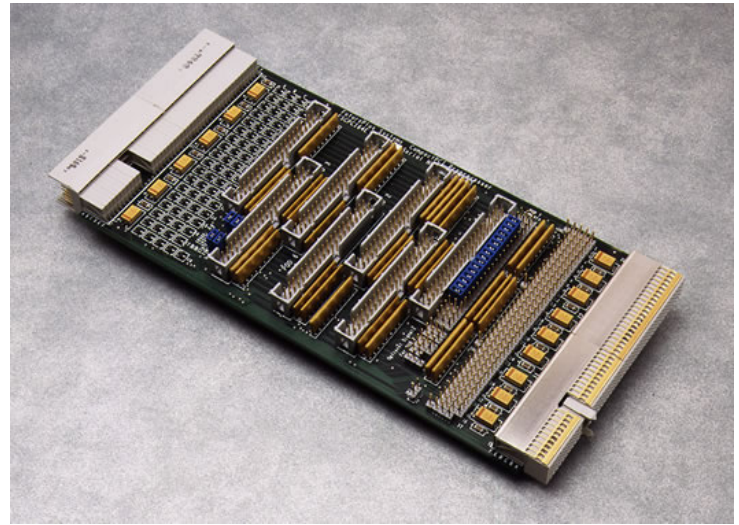
FuturePlus® Systems

Power Tools for Bus Analysis

Straightforward, Reliable CompactPCI Analysis

The FS3020 CompactPCI Analysis Probe provides an electrical and mechanical interface to Agilent logic analyzers for passive CompactPCI bus analysis in 3U or 6U systems. In State Analysis mode, the bus protocol decode software executes in the Agilent logic analyzer and decodes the key CompactPCI signals.

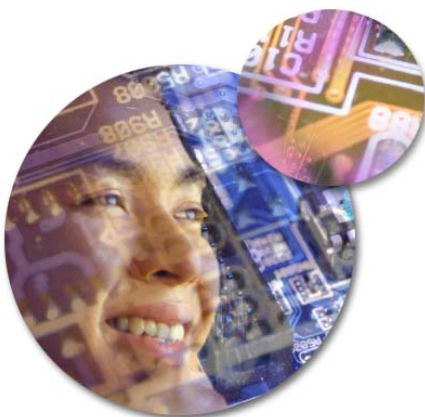
A readable display is presented that lists the transaction type, address, data and address modifiers. The software also supports user-defined symbols that can be easily added to the state listing display. To assist with triggering, pre-defined resource terms have been included.



FS3020 CompactPCI Analysis Probe and Interposer

Key Features

- Reliable and accurate 32 or 64-bit CompactPCI bus monitoring
- Complete State Analysis to 66 MHz
- Passive buffering of signals provides accurate Timing Analysis to 500 MHz
- Logic Analyzer Configuration Software gets you up and running fast
- CompactPCI bus transaction inverse assembly software executes in your logic analyzer
- No need for flying leads or termination adapters
- Simple logic analyzer connection allows easy in-system debug
- CompactPCI add-in card extends beyond the card cage
- Schottky diode clamping prevents unwanted reflections
- Both 3U and 6U size cards supported; connectors comply with IEC-1076, shielded
- Additional test points can be used for high speed timing analysis or oscilloscope connection
- Enhanced Inverse Assembler operation available
- Interposer design provides extender card functionality
- Additional signals can be attached to the logic analyzer via user pins
- Provides system arbitration slot support for viewing arbitration signals



Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our analysis probes and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.



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General Description

The CompactPCI analysis probe and extender card provides three functions:

- 1) Acts as an extender for a CompactPCI module beyond the backplane, and provides access to both sides for easy debug.
- 2) Provides an electrical and mechanical interface to Agilent logic analyzers for passive CompactPCI bus monitoring.
- 3) Provides test points to measure the power and signal fidelity of the CompactPCI bus.

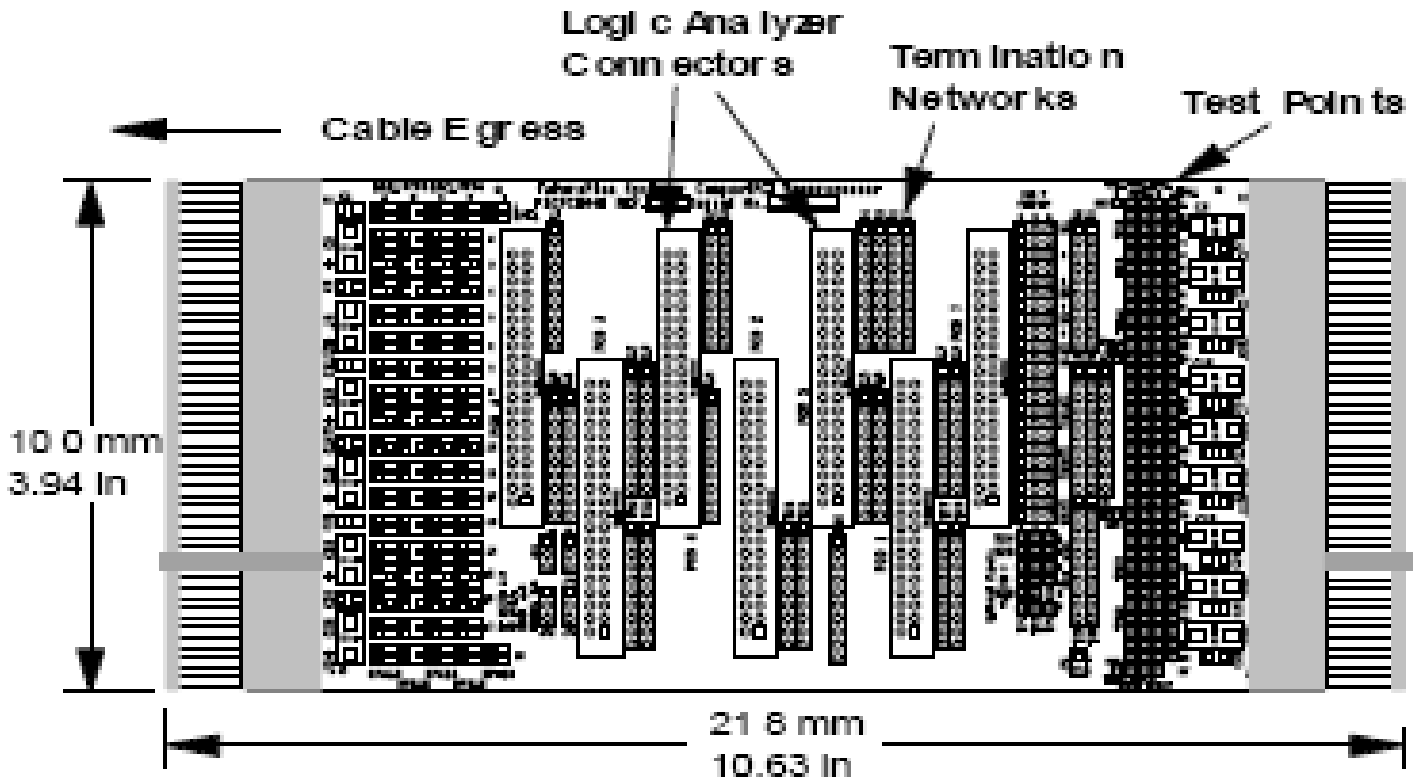
NOTE: Electrically, the CompactPCI bus is extended approximately 10.0 inches in etch length. Depending on the design of the system, users may experience difficulties with this extension of the CompactPCI bus. The passive logic analyzer termination presents a single electrical load on the CompactPCI bus via low capacitance (10 pf), high impedance terminators, and also provides a matched impedance to the logic analyzer.

The Analysis Probe includes seven 40-pin logic analyzer connectors. High speed Schottky clamping diodes connected to the CompactPCI bus signals and physically mounted near the extender connector prevent the added etch length from causing unwanted reflections back onto the bus.

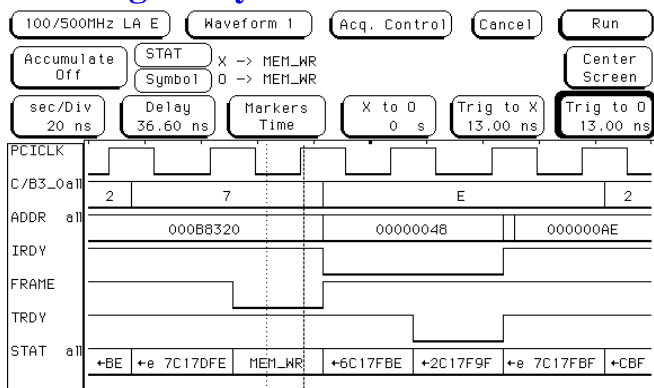
The CompactPCI protocol decode software executes in the logic analyzer. In State Analysis mode, the analyzer master clock is the CompactPCI clock. The bus protocol decode software decodes the key CompactPCI bus signals and presents a readable display that lists the transaction type, address, data and key status conditions such as wait states and retries. The software also supports user-defined symbols that can be easily added to the state listing display. The user can also select post-processing filters which allow the acquired data to display only chosen transactions.

To assist with triggering, pre-defined resource terms have been included that can be used to prevent WAIT and IDLE states from being acquired, thus saving trace memory and providing an easier-to-read state display. FuturePlus Systems also provides a CompactPCI bus triggering application note.

ES3020 Mechanical Drawing

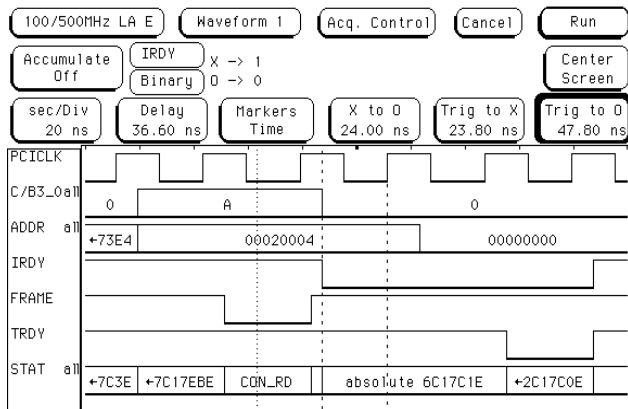


Timing Analysis



Matched signal length, low capacitive loading, and no active buffering of the CompactPCI signals makes the FS3020 ideal for accurate and easy timing analysis.

The FS3020 Analysis Probe software contains pre-defined trigger terms that help track down those hard-to-find bugs.



100/500MHz LA E Trigger 1

State Sequence Levels

1	While storing "≠IDLE≠T_WAIT≠D_WAIT" TRIGGER on "MEM_RD" 1 time	Arming Control
2	Store "≠IDLE≠T_WAIT≠D_WAIT"	Acquisition Control
		Count Time
		Modify Trigger

Label	IRDY	FRAME	TRDY	STAT	STOP	DEVS
Terms	Hex	Binary	Hex	Symbol	Binary	Bina
IDLE	1	1	X	absolute #XXXXXX	X	X
T_WAIT	0	X	1	absolute #XXXX#X	1	0
D_WAIT	0	X	X	absolute #XXXX#X	1	1
MEM_RD	1	0	1	MEM_RD	1	1

State Analysis

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
242	D32=xxxxxxxx08	296 ns
243	I/O READ ADR=00000073	9.072 us
244	D32=23xxxxxx	1.096 us
245	I/O WRITE ADR=00000020	10.97 us
246	D32=xxxxxxxx20	168 ns
247	INTERRUPT ACK CYCLE	54.90 ms
248	D32=xxxxxxxx08	296 ns
249	I/O READ ADR=00000073	9.904 us
250	D32=23xxxxxx	1.128 us
251	I/O WRITE ADR=00000020	10.97 us
252	D32=xxxxxxxx20	168 ns

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
950	CONFIG READ ADR=80000000	8.960 ms
963	FUNC=0 REG=0 TYPE=00	
964	DEVICE ID=4158 VENDOR ID=1002	360.1 us
964	IDLE	32 ns
965	CONFIG READ ADR=0008000C	27.00 us
966	FUNC=0 REG=3 TYPE=00	
966	BIST=00 Hdr_Typ=00 Lat_Tmr=00 CLS=00	264 ns
967	IDLE	32 ns
968	CONFIG READ ADR=00080008	31.40 us
968	FUNC=0 REG=2 TYPE=00	
969	CLASS CODES:03 00 00 REV ID=00	264 ns
970	IDLE	40 ns

CompactPCI Bus transaction inverse assembly options post-process the acquired data. This feature allows the user to customize the display to show only the transactions or cycles that are of interest.

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
12	MEM READ ADR=000FE060	264 ns
13	D32=A5837102	3.608 us
14	MEM READ ADR=000FE064	200 ns
15	D32=A6A6C5A5	3.536 us
16	MEM READ ADR=000FE068	296 ns
17	D32=B6C54471	3.568 us
18	MEM READ ADR=000FE06C	200 ns
19	D32=A6B566F5	3.536 us
20	MEM READ ADR=000FE070	304 ns
21	D32=A5560471	3.560 us
22	MEM READ ADR=000FE074	200 ns

PCI Bus Inverse Assembly Options

Configuration Reads:

Configuration Writes:

All Other Transactions:



Ordering Information

FS3020 CompactPCI Analysis Probe and Extender Card

Optional Accessory

FS1202 12 inch logic analyzer extender cable (Requires one for each logic analyzer pod.)

Software included with the FS3020:

Configuration files for the Agilent logic analyzer

Protocol Decoder software, runs on the Agilent logic analyzer

Logic Analyzer Requirements

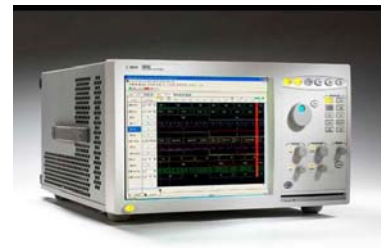
The FS3020 supports all Agilent 1670, 16700, 1680, 1690, 16800 and 16900-series Logic Analyzers that have 40 pin modules. Pod requirements are listed below:

For 32-bit protocol or timing analysis, the FS3020 requires 4 40-pin 33 MHz logic analyzer pods

For 64-bit protocol or timing analysis, the FS3020 requires 6 40-pin 33 MHz logic analyzer pods

For viewing bus arbitration signals, the FS3020 requires 1 additional 40 pin 33 MHz logic analyzer pod

The FS3020 does not require Termination Adapters



Please note: for the most up-to-date information about Agilent logic analyzer compatibility, please check the FuturePlus Systems website at:
http://www.futureplus.com/products/fs3020/fs3020_sysreq9.shtml

We offer excellent technical support and quick delivery.

More information and application notes are on the FuturePlus Systems website at:
<http://www.futureplus.com/products/fs3020>

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