

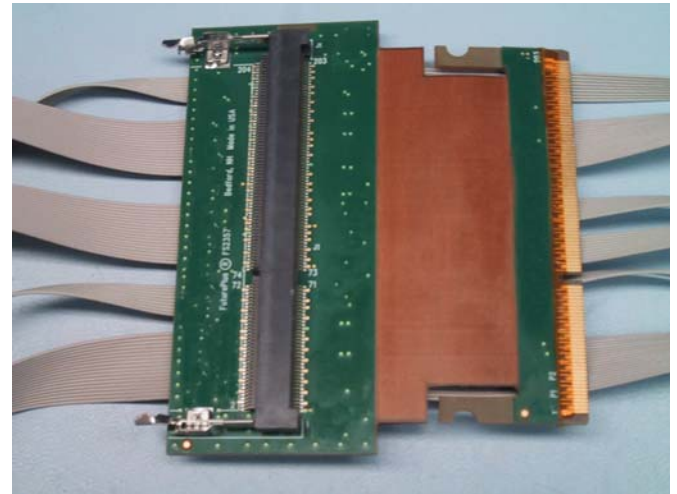
DDR3 SO-DIMM Interposer

For use with Tektronix Logic Analyzers

FuturePlus® Systems

Power Tools for Bus Analysis

- DDR3 1333 MT/s Analysis Probe
- Quick, easy connection between the SO-DIMM connector and Tektronix Logic Analyzers
- Compatible with all 204-pin DDR3 SDRAM SO-DIMMs
- Up to 1333 MT/s protocol decode
- 50 GHz MagniVu™ Timing Acquisition
- Non-intrusive interposer design



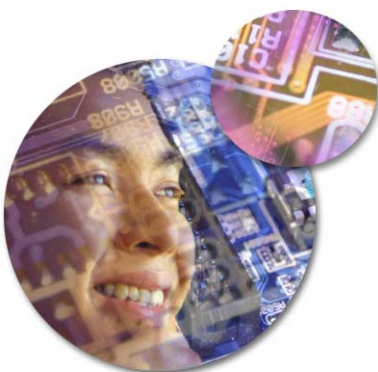
FS2359 DDR3 SO-DIMM Interposer

Key Features

- Quick and easy connection between the DDR3 SO-DIMM connector and Tektronix logic analyzers
- Up to 1333 MT/s protocol decode
- Supports both registered and non-registered SO-DIMMs
- Interposer design allows probing a fully-loaded memory bus
- Simultaneous capture of read and write transactions

Powerful, Reliable 1333 MT/s Protocol Decode

The FS2359 is a 1333 MT/s Double Data Rate (DDR3) SDRAM bus interposer. It provides complete protocol decode of memory transactions using a Tektronix logic analyzer as the analysis execution engine. This combination provides powerful triggering, debug and compliance verification measurements. Data is decoded and displayed at any level of detail from the protocol to binary levels.



Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our analysis probes and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.

Tektronix

Embedded Systems
Tools Partner

Accurate State and Timing Analysis

The FS2359 DDR3 1333 SO-DIMM memory bus interposer brings bus signals to your Tektronix logic analyzer via controlled impedance cables for an easy protocol-and-timing analysis connection while maintaining signal fidelity.

Protocol Analysis

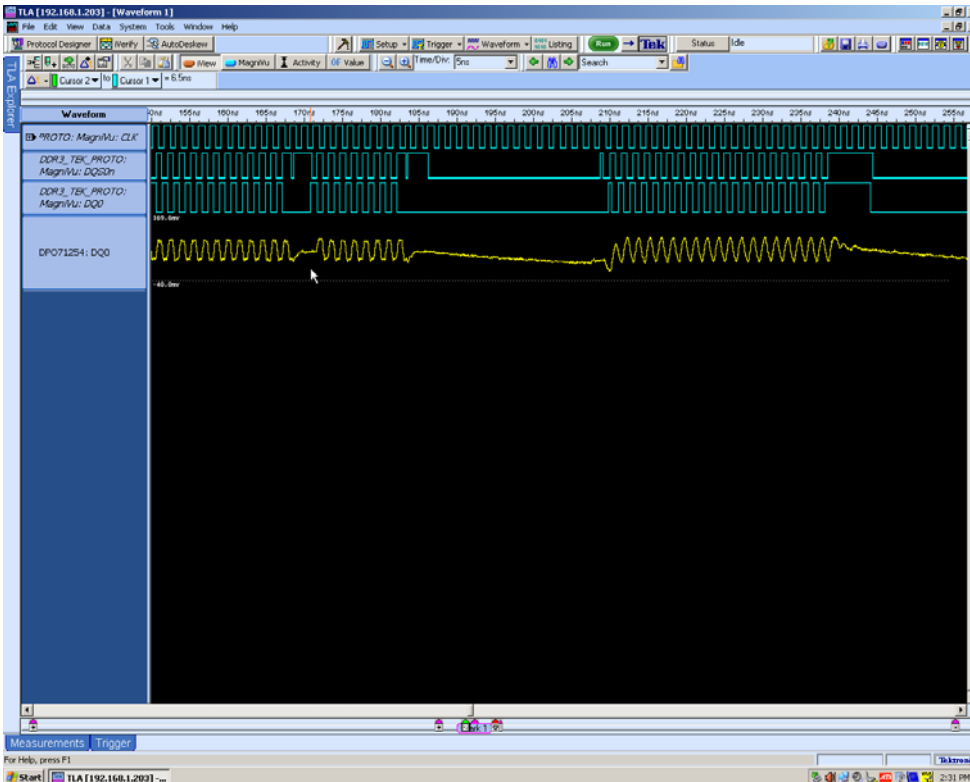
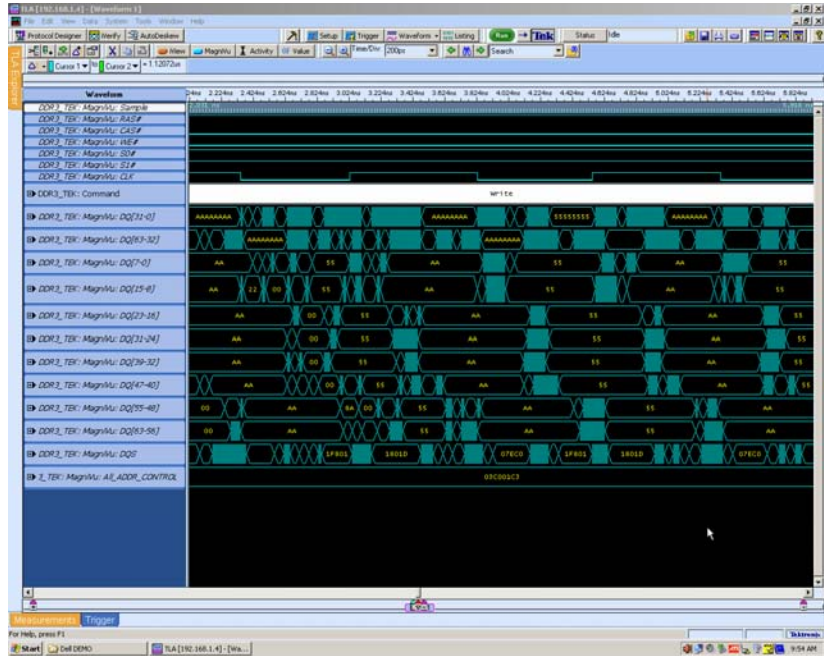
The screenshot displays the Tektronix Logic Analyzer (TLA) software interface. The main window shows a list of DDR3 transactions with the following columns: Address, Command, Mnemonics, Bank_Address, Chip_Selects, and Data. The transactions are color-coded: blue for Data, green for Activate, and yellow for Read. The 'Measurements' panel at the bottom allows users to add and configure various measurement types, including Period, Frequency, Positive/Negative Duty Cycle, and Positive/Negative Pulse Width. The interface also includes a menu bar, a toolbar, and a status bar at the bottom.

Address	Command	Mnemonics	Bank_Address	Chip_Selects	Data
3270	100	Data= 4c89fA0c 02008488 00	111	0010	00000000
3270	100	Data= 00100888 02008488 00	111	0010	00000000
3270	100	Data= 00000808 02008488 00	111	0011	00000000
3270	100	Deselect	111	0011	00000000
3270	100	Deselect	111	0011	00000000
3270	100	Write Data	111	0011	00000000
3270	100	Write Data	111	0011	0008240c
3270	100	Write Data	111	0011	0008240c
3270	100	Write Data	111	0011	0008240c
3270	100	Write Data	111	0011	00100888
3270	100	Write Data	111	0011	00100808
3270	100	Deselect	111	0011	00000808
05E4	011	Activate	001	0010	00000808
05E4	011	Address= 05E4	001	0010	00000808
05E4	011	Deselect	001	0011	00000808
05E4	011	Deselect	001	0011	00000808
05E4	011	Deselect	001	0011	00000808
05E4	011	Deselect	001	0011	00000808
05E4	011	Deselect	001	0011	00000808
05E4	011	Deselect	001	0011	00000808
001C	101	Read	001	0010	00000000
001C	101	Bank= 1	001	0010	00000000
001C	101	Address= 5E401C	001	0010	00000000
001C	101	Data= 00000000 00000000 00	001	0010	00000000
001C	101	Data= 00100000 00000000 00	001	0010	00000000
001C	101	Data= 00100080 00000000 00	001	0010	00000000
001C	101	Data= 80096080 15061000 00	001	0010	00000000
001C	101	Data= 02100004 00008148 01	001	0010	00000000
001C	101	Data= 00090080 00000000 00	001	0010	00000000

The FS2359 protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Tektronix logic analyzer provides extensive triggering and store qualification features. Depending on the logic analyzer's resources, the FS2359 interposer can be configured to perform State analysis of Reads or Writes, or both Reads and Writes, at 1333 MT/s. The DDR protocol decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions in different colors.

Timing Analysis

The FS2359 lets you perform timing analysis measurements on a DDR3 SO-DIMM bus at speeds up to 1333 MT/s. The MagniVu™ Timing signals provided by the Tektronix logic analyzer allow accurate waveform analysis of all signals on the DDR3 DIMM bus.



Signal Integrity Measurements

Simultaneously acquire both digital and analog data from your logic analyzer and oscilloscope, and display them together on the logic analyzer display. iCapture gives you access to Tektronix' industry-leading real-time oscilloscopes.

iCapture technology permits simultaneous viewing of analog and digital data

Ordering Information

FS2359 DDR3 1333 SO-DIMM Interposer

FS1061 TLA7BB4 DDR3 Full Channel Probe Cable (1 ea required)

FS1062 TLA7BB4 DDR3 Half Channel Probe Cable (3 ea required)

Software included with the FS2359:

➤DDR3 Support Package Windows License for FS2359, includes setup files and protocol decoder software

Logic Analyzer Requirements

See the table below for FS2359 protocol or timing analysis requirements.

The FS2359 makes connection and termination to the logic analyzer with probe cables, which must be ordered separately.

The FS2359 requires up to two logic analyzer modules and one TLA7000-series mainframe.

DDR Memory Bus Speed	Analyzer Type	Timing Analysis	Protocol Analysis (with 50 GHz MagniVu)
800 MT/s	TLA7AA4 (450 MHz mode), TLA7BB4	2 cards configured for timing analysis	2 cards configured for state analysis
1066 MT/s	TLA7BB4	2 cards configured for timing analysis	2 cards configured for state analysis
1333 MT/s	TLA7BB4	2 cards configured for timing analysis	2 cards configured for state analysis.

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