FuturePlus Systems

Power Tools For Bus Analysis

Agilent Technologies
Premier Solution Partner

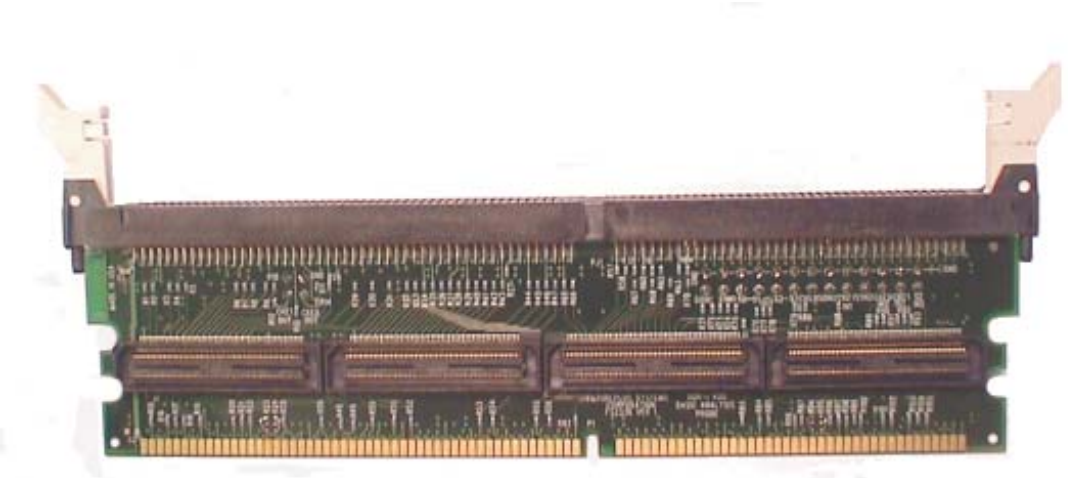
DDR 400 SDRAM MEMORY

DDR Memory Protocol Analysis For Use with Agilent Logic Analyzers

The FuturePlus® FS2336 DDR400 Double Data Rate (DDR) SDRAM bus analysis probe provides complete protocol decode of memory transactions using an Agilent logic analyzer as the analysis execution engine. This combination provides powerful triggering, debug and compliance verification measurements. Data is decoded and displayed at any level of detail from the protocol level to binary.

FS2336 Key Features

- Quick and easy connection between the DDR400 bus connector and Agilent logic analyzers
- Complete and accurate 400 MT/s protocol decode
- Complete and accurate 2 or 4 GHz timing analysis (depending on analyzer modules).
- Uses High-speed Timing Zoom traces to locate tight DDR data valid windows for optimal state data capture.
- Supports both X4 and X8 SDRAMS
- Off Line analysis software allows PC-based analysis of data captured on a 16700 series logic analyzer.
- Requires only 750 ps data valid window for state data capture.
- Interposer design does not consume a DDR400 slot.
- Supports burst sizes of 2, 4, or 8
- Write only, reads only, or writes and reads visible in most circumstances.



The FS2336 DDR400 Memory Bus Analysis Probe

An Agilent Technologies Premier Solutions Partner

FS2336 Description

Accurate State and Timing Analysis

The FS2336 DDR 400 DIMM memory bus analysis probe brings bus signals to your Agilent logic analyzer via controlled impedance cables for an easy protocol and timing analysis connection while maintaining signal fidelity.

The included transactor software translates the signals into easily understood bus transactions at the full bus speed. Extensive triggering and store qualification features are available through the Agilent logic analyzer. All signals are probed passively before being sent to the logic analyzer. These are also available unbuffered.

Protocol Decode Mode

The included protocol-decode software translates acquired signals into easily understood bus transactions at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features.

Burst size can be set to 2, 4, or 8. Burst truncation due to read or write chaining is supported. Users can select a display of writes only, reads only, writes and reads with the clock gated off during idle cycles (when the strobes float), or all strobe activity.

The DDR protocol-decode software executes in the Agilent logic analyzer. The software decodes the key DDR bus signals and presents a display that lists the transaction type, address, data and key status conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to be displayed in different colors based on transaction type.

Timing Analysis

The FS2336 has a unique dual-path design that enables 4 GHz true asynchronous timing measurements using Agilent's timing zoom technology (16753/4/5/6). The analysis probe has two separate paths for the command and data buses. The timing path goes directly through the analysis probe with no active components between the signals and the logic analyzer.

Cross-Domain Analysis

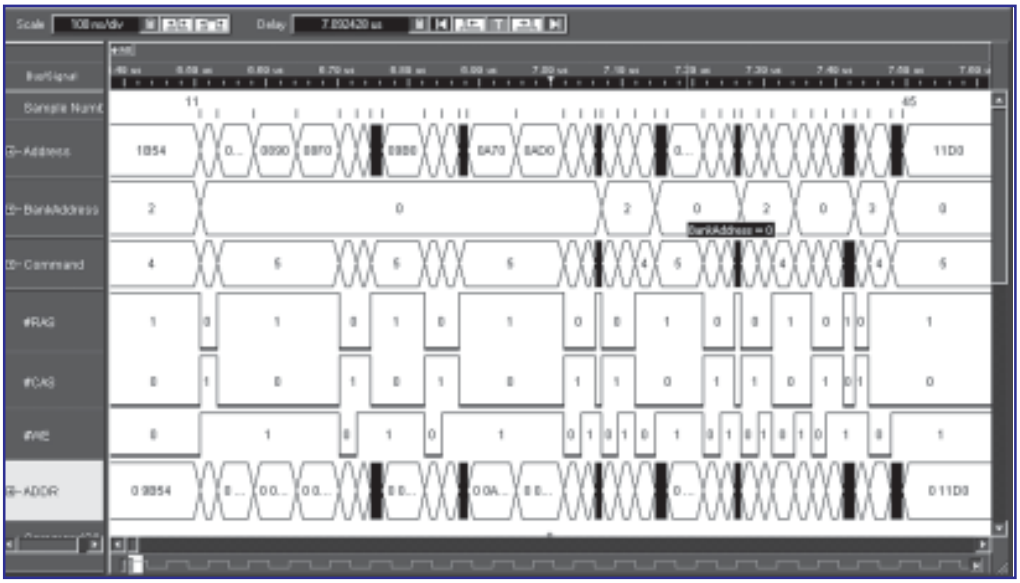
Use a single Agilent 16700-series logic analyzer to simultaneously capture data from multiple buses in your system. You can create a custom measurement system with cross-domain triggering between different types of buses, and display the time-correlated data on a single screen, with common markers.

For example, use the FS2336 to analyze the DDR memory bus — and use another analysis probe to analyze a different bus at the same time. FuturePlus Systems has analysis probes for the PCI-X, PCI, SCSI, Rambus, USB, and a wide variety of other buses.

Agilent Eye Scan Technology

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement of the design verification process. Eye scan lets you acquire comprehensive signal integrity information on all the buses in your design, under a wide variety of operating conditions, in minimum time.

The FS2336 allows you to use Eye Scan technology on signals being probed, but does not contain clock-recovery circuitry.



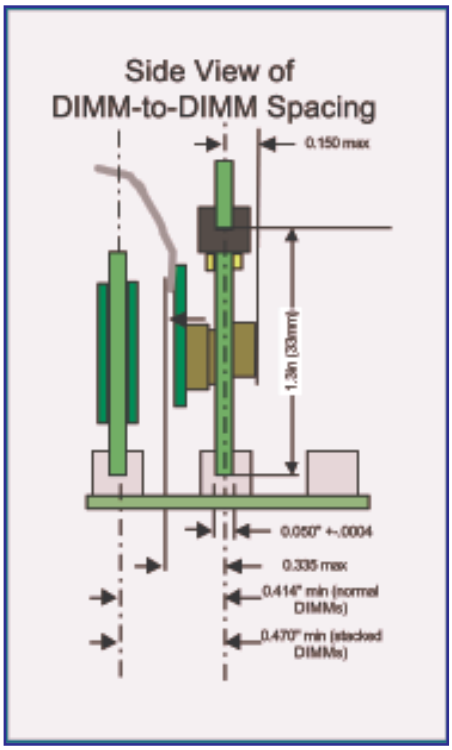
A screen capture of a typical timing display

Supported Memory Modules

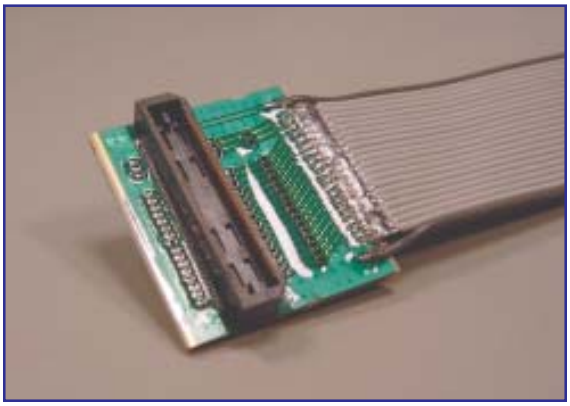
The FS2336 supports the PC3200 module, a 184-pin, 200 MHz clock (400 MT/s data rate), 64-bit, Unbuffered Synchronous Double Date Rate (DDR) DRAM Dual In-Line Memory Module (DDR SDRAM DIMM). It also supports slowers versions that uses a 100 MHz (200 MT/s data rate) or a 133 MHz clock (266 MT/s data rate) DDR SDRAM DIMM. Registered and non-registered DIMM's are supported.

Connecting to the Logic Analyzer

The FS2336 attaches to the logic analyzer with termination adapters. Two are available. The FS1014 (Agilent E5378A) attaches to a 16753A through 16756A or 16760A. For situations where the probe must be used in a slot adjacent to other DIMM modules, the FS1026 (Agilent FSI-60090) attaches via a right angle egress to a 16753A through 16756A or 16760A. The necessary impedance matching networks are included in the Termination Adapters.



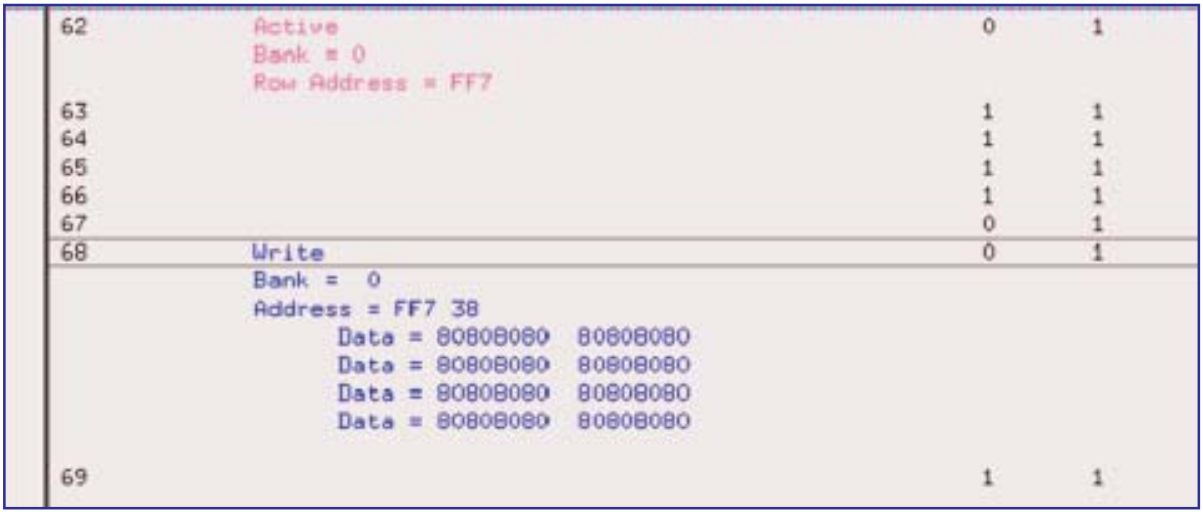
The FS1026 termination adapter enables easy connection of the probe in the tight space between two ajacent memory slots.



The FS1026 Right-angle Termination Adapter

Power Requirements

Power for the FS2336 is supplied by the logic analyzer. The analysis probe does not require any power from the DDR bus.



This display capture shows the typical output of the protocol decoder. The potocol decoder contains a filter that allows post filtering of any states including the *Not Selected* state, which is defined as a state that has no command or data associated with it.

Ordering Information

FS2336 DDR400 DIMM Bus Analysis Probe and Interposer
Termination Adapters (4 required)
FS1026 - Right angle egress, connects the 16753A-756A, 16760A, 16950A modules to FS2336
Agilent E5378A - 90 degree egress, connects the 16753A-756A, 16760A, 16950A modules to FS2336
Agilent E5385A - 90 degree egress, connects the 16717A-719A, 16750A-752A modules to FS2336

Software included with the FS2336:
Configuration files for the Agilent logic analyzer
Protocol Decoder software, runs on the Agilent logic analyzer

Logic Analyzer Requirements

See the table below for FS2336 protocol or timing analysis requirements.
The FS2336 requires up to four logic analyzer cards depending on whether protocol (double probed) or timing measurement are being used, and the type of logic analyzer card being used.
A logic analyzer pod has 17 channels

DDR Memory Bus Speed	Logic Analyzer Type	Timing Analysis	Protocol Analysis with Double Probing
200 MT/s (PC1600)	16750/751/752 16753/754/755/756 16910/911 16950	Two Cards Configured as One Timing Machine	Four Cards Configured as One State-Analysis Machine
400 MT/s (PC3200)	16753/754/755/756 16950	Two Cards Configured as One Timing Machine	Four Cards Configured as One State-Analysis Machine

Please note: for the most up-to-date information about Agilent logic analyzer compatibility, please check the FuturePlus Systems website at:
http://www.futureplus.com/products/fs2336/fs2336_sysreq9.shtml

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