

# DDR2 800 Bus Analysis Probe

## For Use With Agilent Logic Analyzers

FuturePlus® Systems

Power Tools for Bus Analysis



### DDR2 800 MT/s Analysis Probe

- Quick, easy connection between the DIMM connector and Agilent Logic Analyzers
- Compatible with all 240-pin DDR2 SDRAM DIMMs
- Protocol decode from 533 MT/s up to 800 MT/s
- 4 GHz Timing Analysis
- Non-intrusive interposer design
- Software only support available for embedded memory systems



FS2334 DDR 800 Memory Analysis Probe

### Key Features

- Quick and easy connection between the DDR2 DIMM connector and Agilent Logic Analyzers
- Up to 800 Megatransfers/s protocol decode
- Supports both registered and non-registered DIMMs
- Interposer design allows probing a fully-loaded memory bus
- Simultaneous capture of read and write transactions

### Powerful, Reliable Protocol Decode, up to 800 MT/s

The FuturePlus® FS2334 is a 800 MT/s DDR2 SDRAM bus analysis probe. It provides complete protocol decode of memory transactions using an Agilent logic analyzer as the analysis execution engine. This combination provides powerful triggering, debug and compliance verification measurements. Data is decoded and displayed at any level of detail from the protocol to binary.



### Helping You Design with Tomorrow's Computer Buses, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our analysis probes and software help you monitor and verify complex activities on your advanced-technology computer bus design. FuturePlus Systems offerings include bus-analysis solutions for HyperTransport®, PCI-X , DDR Memory, USB2.0, and most other popular computer buses.



## Accurate State and Timing Analysis

The FS2334 DDR2 800 DIMM memory bus analysis probe brings bus signals to your Agilent logic analyzer via controlled impedance cables for an easy protocol-and-timing analysis connection while maintaining signal fidelity.

## Configuration Software for Quick, Easy Setup

The FS2334 DDR2 protocol analysis probe includes automatic setup software for all supported Agilent logic analyzer configurations.

## Protocol Analysis

Sample Number	COMMAND	Filter Tags	ADDRESS	READdata31-0	READdata6
-850.4	Data = 80808080 80808080 CB = 0	0000			
-850.5	Data = 80808080 80808080 CB = 0	0000			
-850.6	Data = 80808080 80808080 CB = 0	0000			
-850.7		0000			
-849		DATA	0 0AF4	8080 8080	8080 8080
-848		DATA	0 0AF4	8080 8080	8080 8080
-847		DATA	0 0AF4	8080 8080	8080 8080
-846	Precharge: Bank 0	PRECHARGE	0 0AF4	8080 8080	8080 8080
-845		DATA	0 0EF4	8080 8080	8080 8080
-844		DATA	0 0EF4	8080 8080	8080 8080
-843		DATA	0 0EF4	8080 8080	8080 8080
-840	Active	ACTIVE	0 0EF4	8080 8080	8080 8080
-840.1	Bank = 0	0000			
-840.2	Row Address = EF4	0000			
-834	Write	WRITE	0 0BF0	8080 8880	8090 8080
-834.1	Bank = 0	0000			
-834.2	Address = AF4 BF0	0000			
-834.3	Data = 80808080 80808080 CB = 0	0000			
-834.4	Data = 80808080 80808080 CB = 0	0000			
-834.5	Data = 80808080 80808080 CB = 0	0000			
-834.6	Data = 80808080 80808080 CB = 0	0000			
-834.7		0000			
-830	Write	WRITE	0 0BF4	8080 8080	8080 8080
-830.1	Bank = 0	0000			
-830.2	Address = AF4 BF4	0000			

## Protocol Decode Mode

The FS2334 protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features.

Depending on the logic analyzer cards and frames available, the FS2334 probe can be configured to perform State analysis of Reads or Writes, or both Reads and Writes, from 533 MT/s, up to 800 MT/s.

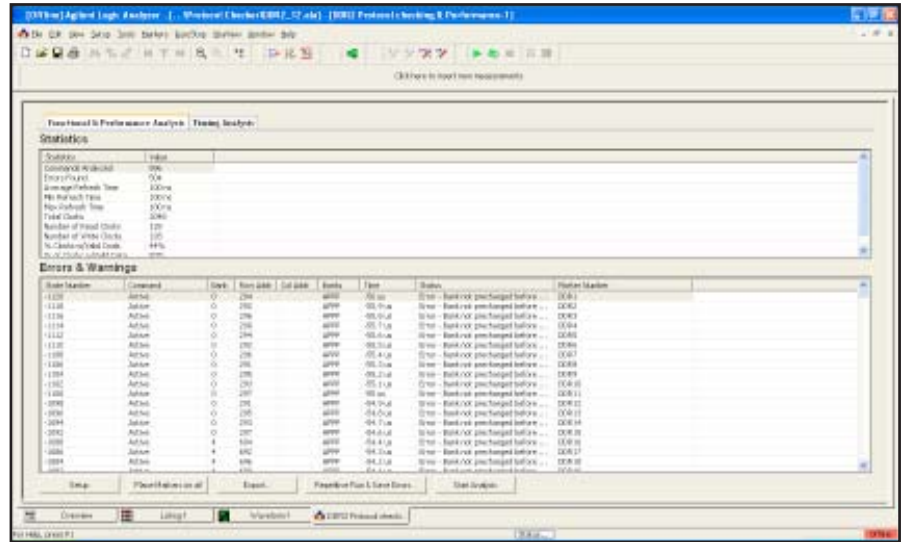
The DDR protocol-decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions in different colors.

## Power Requirements

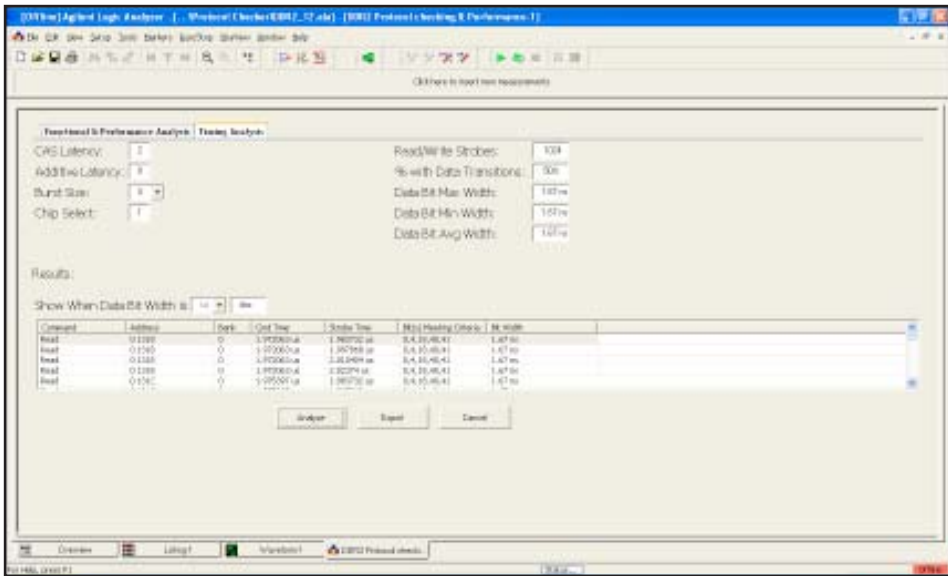
The FS2334 is powered by an external power supply, which is included with the product. The analysis probe does not tap any power from the DDR bus.

## DDR2 protocol Checking and Performance Tool.

The FS1140 protocol checking and performance tool works with the FS2334 analysis probe to analyze acquired data for protocol violations. It also executes several performance measurements. The FS1140 operates within the Agilent B4606A or B4607A Advanced Customization Environment for 16900-Series logic analysis systems. The B4606A and B4607A are available from Agilent Technologies.

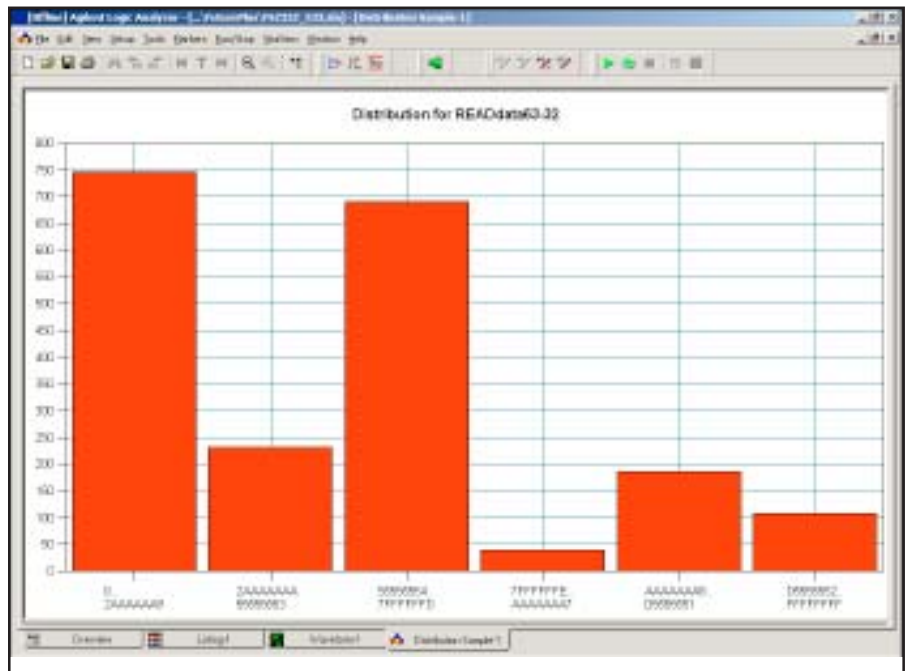


Protocol Checker takes a previously acquired trace and calculates a number of statistics, including errors found.



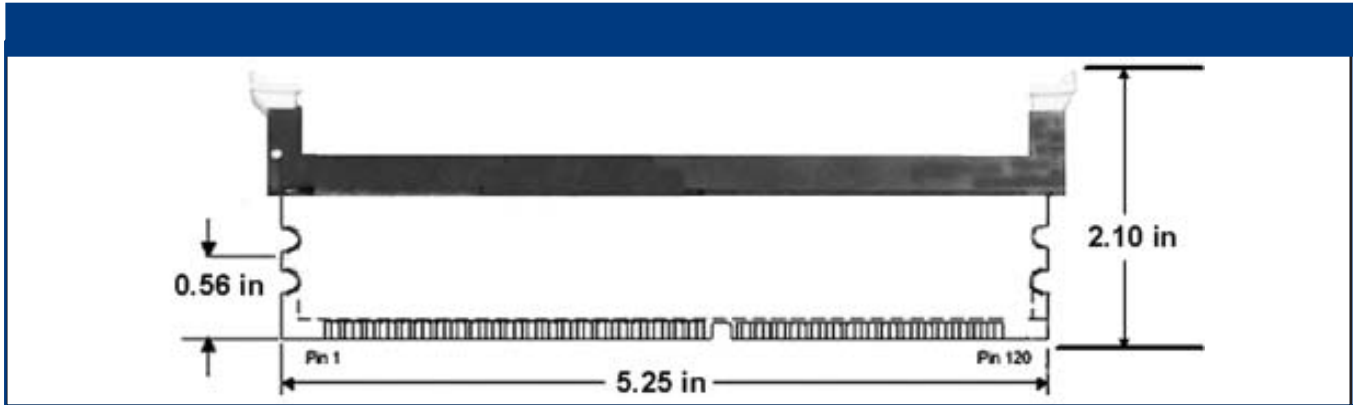
Timing Analysis takes a previously acquired trace and calculates timing statistics and performance benchmarks on that data.

Data from either the protocol- or timing-analysis screens can easily be exported to a CSV file for further analysis or graphing.



## Supported Agilent Logic Analyzers

Agilent 16900 series logic analysis system with seven each of the 16753-756 modules or 16950; or 14 each of the 16760 module.



## Ordering Information

**FS2334** ..... 800MT/s DDR2 Analysis Probe and Interposer

*We offer excellent technical support and quick delivery.*

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Visit our web site at [www.futureplus.com](http://www.futureplus.com).

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