



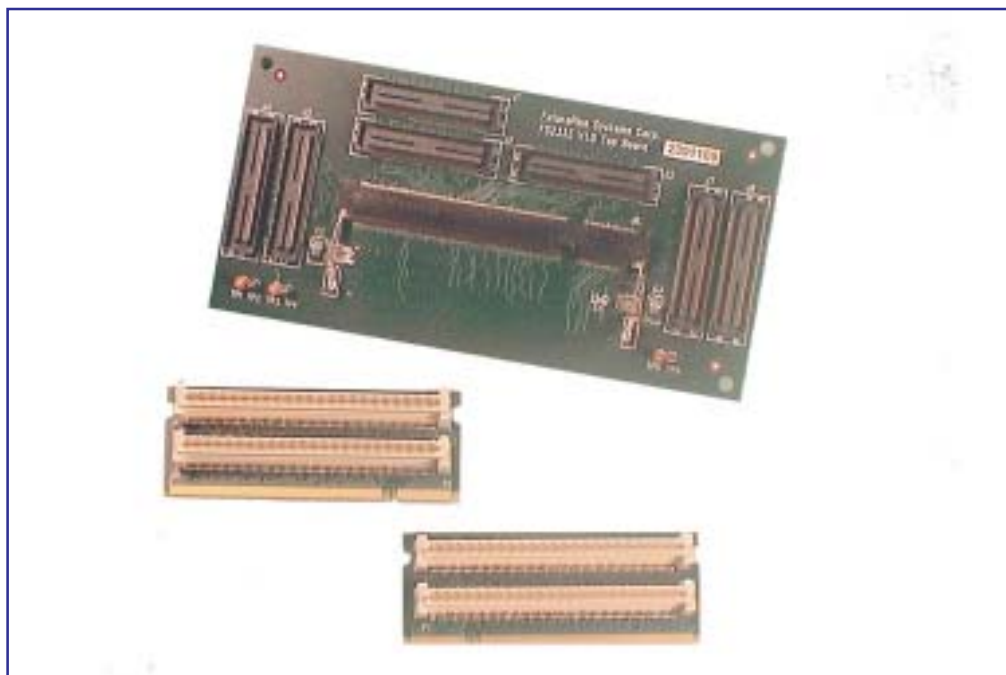
SODIMM Memory Analysis Probe

For use with Agilent Logic Analyzers

The FuturePlus Systems FS2333 is a 333 MT/s Double Data Rate (DDR) SDRAM bus analysis probe for SODIMMs. It provides complete analysis of memory transactions using an Agilent logic analyzer as the analysis execution engine. This combination provides powerful triggering, debug and compliance verification measurements. Data is decoded and displayed at any level of detail from the protocol level to binary.

Features

- Includes adapters for both left and right hand egress
- Quick and easy connection between the 333 MT/s DDR SO-DIMM SDRAM memory bus connector and Agilent logic analyzers.
- Interposer design does not consume a SO-DIMM slot, so you can probe in single socket systems.
- Complete and accurate 333 MT/s (PC2700) protocol analysis and timing analysis up to 4 GHz
- Compatible with all 200-pin DDR SDRAM SODIMM's up to 333 MT/s
- All signals are probed passively.
- Writes only, reads only, or writes and reads visible in all circumstances.
- Support for X8, X16 and X32 SDRAMs
- Requires only 750 ps data valid window for state data capture.



FS2333 DDR memory analysis probe with egress adapters

FS2333 Description

The DDR SO-DIMM analysis probe brings bus signals to your Agilent logic analyzer via controlled-impedance cables for an easy 333 MT/s state and timing analysis connection while maintaining signal fidelity. It provides a quick, reliable electrical and mechanical interface between a DDR memory bus and an Agilent logic analyzer. Memory transaction data is displayed on the logic analyzer in several levels of abstraction.

Protocol Analysis Mode

The included protocol-decode software translates acquired signals into easily understood bus transactions at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features.

Burst size can be set to 2, 4, 8, or can be automatically sensed. Burst truncation due to read or write chaining is supported. Users can select a display of writes only, reads only, writes and reads with the clock gated off during idle cycles (when the strobles float), or all strobe activity.

The DDR protocol-decode software executes in the Agilent logic analyzer. The bus protocol-decode software decodes the key DDR bus signals and presents a display that lists the transaction type, address, data and key status conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions in different colors.

Timing Analysis Mode

The FS2333 has a unique design that enables 4 GHz true asynchronous timing measurements using Agilent's timing zoom technology (16753/4/5/6). The timing path goes directly through the analysis probe with no active components between the signals and the logic analyzer.

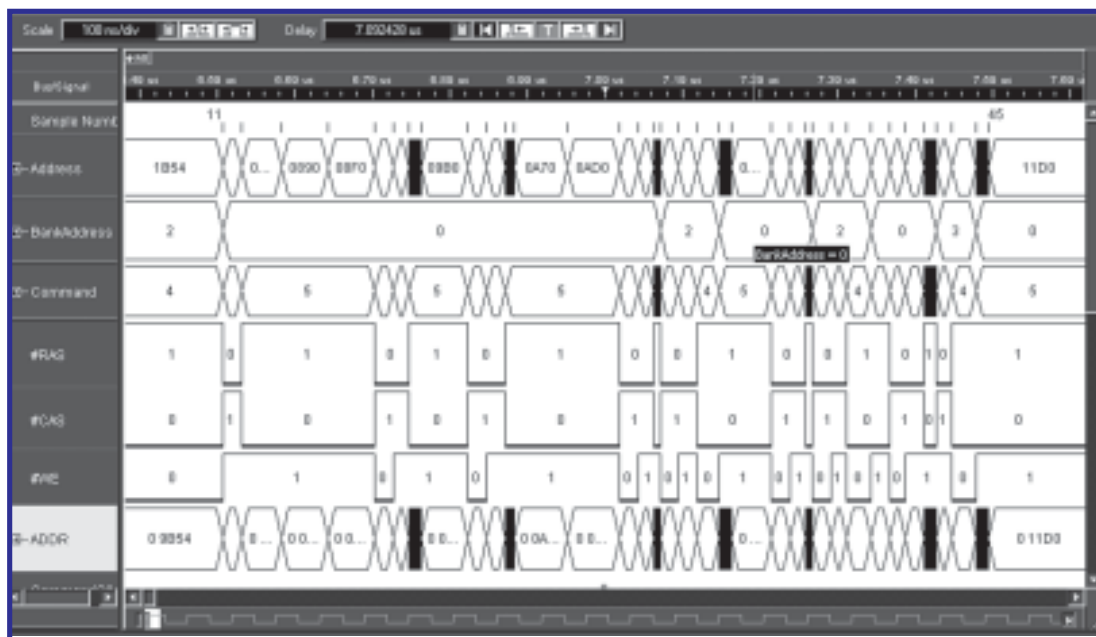
Cross-Bus Analysis

Use a single Agilent 16700-series logic analyzer to simultaneously capture data from multiple buses in your system. You can create a custom measurement system with cross-domain triggering between different types of buses, and display the time-correlated data on a single screen, with common markers.

For example, use the FS2333 to monitor the DDR memory bus — and use another analysis probe to monitor a different bus at the same time. FuturePlus Systems has analysis probes for the PCI-X, PCI, SCSI, Rambus, USB, and a wide variety of other buses.

Using An Extender

The FS2333 does not require you to dedicate one memory position to probing. Included are two different egress adapters. Because of different design implementations, one or the other of the adapters will allow your system to be probed successfully.



A screen capture of a typical timing display

The photo to the right is a typical output of the protocol decoder. Because the analyzer samples data on both edges of the clock, there are going to be some states that have no commands or data associated with them. The protocol decoder contains a filter that will allow post filtering of any states, including the *Not selected* state, which is defined as a state that has no command or data associated with it.

| State Number | DDR | #S0 | #S1 |
|--------------|---|--------|--------|
| Decimal | Inverse Assembler | Binary | Binary |
| 62 | Active Bank = 0 Row Address = FF7 | 0 | 1 |
| 63 | | 1 | 1 |
| 64 | | 1 | 1 |
| 65 | | 1 | 1 |
| 66 | | 1 | 1 |
| 67 | | 0 | 1 |
| 68 | Write Bank = 0 Address = FF7 3E Data = 80808080 80808080 Data = 80808080 80808080 Data = 80808080 80808080 Data = 80808080 80808080 | 0 | 1 |
| 69 | | 1 | 1 |

User Connector Requirements

The FS2333 is designed to plug into a SO-DIMM socket on the user's motherboard. FuturePlus Systems also offers a variety of adapters for situations in which the design or physical requirements require a different connection method.

Power Requirements

Power for the FS2333 is supplied by the Agilent logic analyzer. The analysis probe does not require any power from the DDR bus or an external power supply.

Do you have non-standard, or no connectors?

If you are using DDR memory chips in your design and do not intend to use the small-outline memory module (SODIMM), we still have a solution for you! You can include special Mictor or Samtec connectors in your design and then purchase a FS1107 DDR software license. You can connect your logic analyzer to the special connectors using the high density termination adapters. Information on designing in the Mictor or Samtec connector is available in a FuturePlus application note.

If designing special connectors into your system will not work for you, we have another alternative. FuturePlus Systems offers two special adapters that probe the Memory Access Controller chip in your system. The FS1008 probes a 100 pin TQFP package and the FS1009 probes a 66 pin TSOP package. You can connect your logic analyzer to these packages using the logic analyzer pod "flying leads."

Ordering Information

FS2333 DDR333 SO-DIMM Bus Analysis Probe

Termination Adapters *(Available from Agilent Technologies)*

Agilent E5378A - Connects the Agilent 16753A-756A, 16760, 16950A modules to the FS2333 Samtec connectors. Four are required.

Agilent E5385A - Connects the Agilent 16717A, 16750A-752A, and 16910-911 modules to the FS2333 Samtec connector. Four are required.

Software included with the FS2333:

- Configuration files for the Agilent logic analyzer
- Protocol Decoder software, runs on the Agilent logic analyzer

Logic Analyzer Requirements

- See the table below for FS2333 protocol or timing analysis requirements.
- The FS2333 makes connection and termination to the logic analyzer with either the Agilent E5378A or E5385A Termination Adapters. Four are required.
- The FS2333 requires up to four logic analyzer cards depending on whether protocol (double probed) or timing measurement are being used, and the type of logic analyzer card being used.

| DDR Memory Bus Speed | Logic Analyzer Type | Timing Analysis | Protocol Analysis with Double Probing |
|----------------------|--|--|--|
| 200 MT/s (PC1600) | 16750/751/752 16753/754/755/756 16910/911 16950 | Two Cards Configured as One Timing Machine | Four Cards Configured as One State-Analysis Machine |
| 333 MT/s (PC2700) | 16753/754/755/756 16950 | Two Cards Configured as One Timing Machine | Four Cards Configured as One State-Analysis Machine |



Please note: for the most up-to-date information about Agilent logic analyzer compatibility, please check the FuturePlus Systems website at:

http://www.futureplus.com/products/fs2333/fs2333_sysreq9.shtml

We offer excellent technical support and quick delivery.

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