

# FuturePlus® Systems

*Power Tools for Bus Analysis*



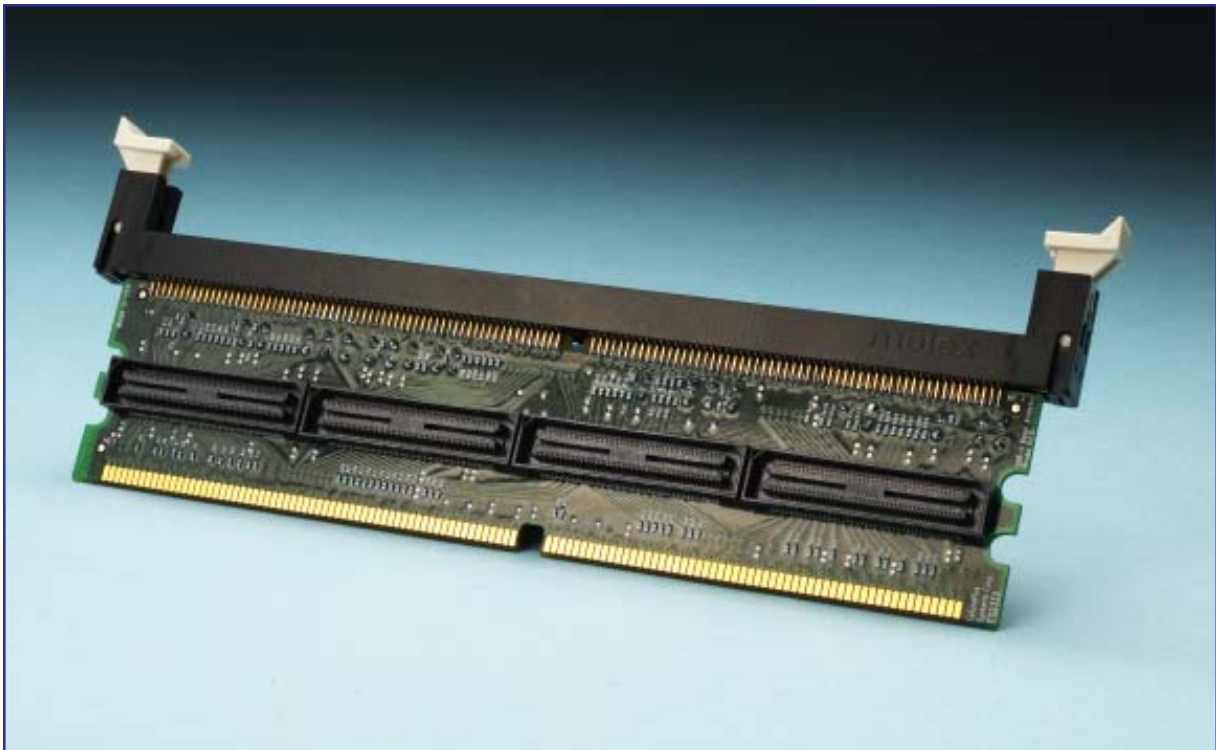
## DDR Memory Analysis Probe

*For use with Agilent Logic Analyzers*

*The FuturePlus® FS2332 is a 667 MT/s Double Data Rate (DDR2) SDRAM bus analysis probe. It provides complete protocol decode of memory transactions using an Agilent logic analyzer as the analysis execution engine. This combination provides powerful triggering, debug and compliance verification measurements. Data is decoded and displayed at any level of detail from the protocol level to binary.*

### FS2332 Key Features

- Quick and easy connection between the DDR2 DIMM connector and Agilent Logic Analyzers
- Up to 667 MT/s protocol decode
- 4 GHz Timing Analysis
- Supports both registered and non-registered DIMMs
- Requires only 750 ps data valid window for state data capture.
- Interposer support
- Compatible with all 240-pin DDR2 SDRAM DIMMs, up to 667 MT/s
- Software only support available for embedded memory systems
- Simultaneous capture of read and write transactions
- Non-intrusive mechanical design



FS2332 DDR2 memory analysis probe with termination adapter

## FS2332 Description

### Accurate State and Timing Analysis

The FS2332 DDR2 667 DIMM memory bus analysis probe brings bus signals to your Agilent logic analyzer via controlled impedance cables for an easy protocol and timing analysis connection while maintaining signal fidelity.

The included transactor software translates the signals into easily understood bus transactions at the full bus speed. Extensive triggering and store qualification features are available through the Agilent logic analyzer. All signals are probed passively before being sent to the logic analyzer. These are also available unbuffered.

The user can elect to view either write cycles, read cycles, or combination write-and-read cycles.

### Protocol Decode Mode

The included protocol-decode software translates acquired signals into easily understood bus transactions at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features.

Burst size can be set to 2, 4, or 8. Burst truncation due to read or write chaining is supported. Users can select a display of writes only, reads only, writes and reads with the clock gated off during idle cycles (when the strobes float), or all strobe activity.

The DDR protocol-decode software executes in the Agilent logic analyzer. The software decodes the key DDR bus signals and presents a display that lists the transaction type, address, data and key status conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions in different colors.

### Timing Analysis

The FS2332 has a unique dual-path design that enables 4 GHz true asynchronous timing measurements using Agilent's timing zoom technology. The analysis probe has two separate paths for the command and data buses. The timing path goes directly through the analysis probe with no active components between the signals and the logic analyzer.

### Cross-Domain Analysis

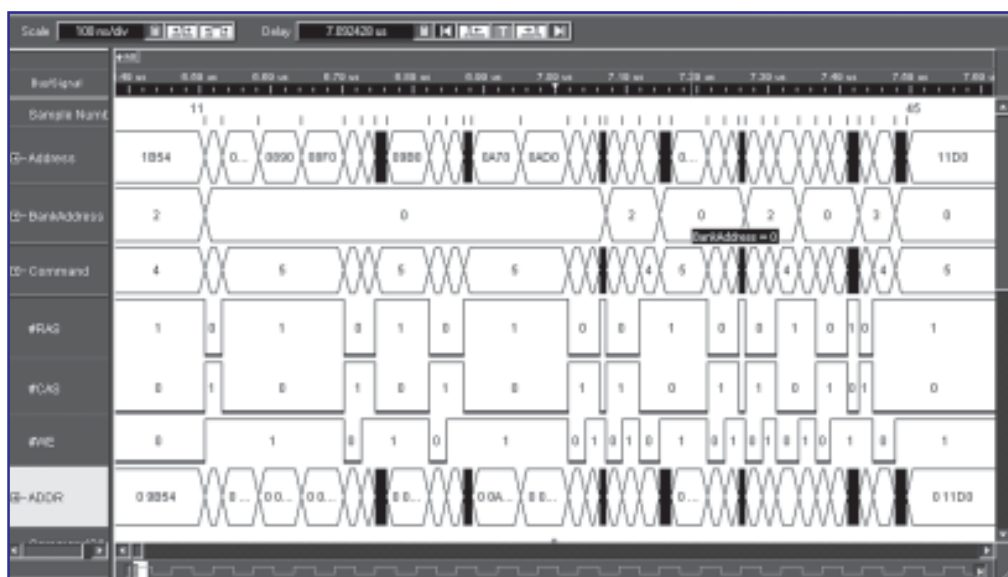
Use a single Agilent logic analyzer to simultaneously capture data from multiple buses in your system. You can create a custom measurement system with cross-domain triggering between different types of buses, and display the time-correlated data on a single screen, with common markers.

For example, use the FS2332 to analyze the DDR memory bus — and use another analysis probe to analyze a different bus at the same time. FuturePlus Systems has analysis probes for the PCI-X, PCI, SCSI, Rambus, USB, and a wide variety of other buses.

### Agilent Eye Scan Technology

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement of the design verification process. Eye scan lets you acquire comprehensive signal integrity information on all the buses in your design, under a wide variety of operating conditions, in minimum time.

The FS2332 allows you to use Eye Scan technology on signals being probed, but does not contain clock-recovery circuitry.



A screen capture of a typical timing display

### Supported Memory Modules

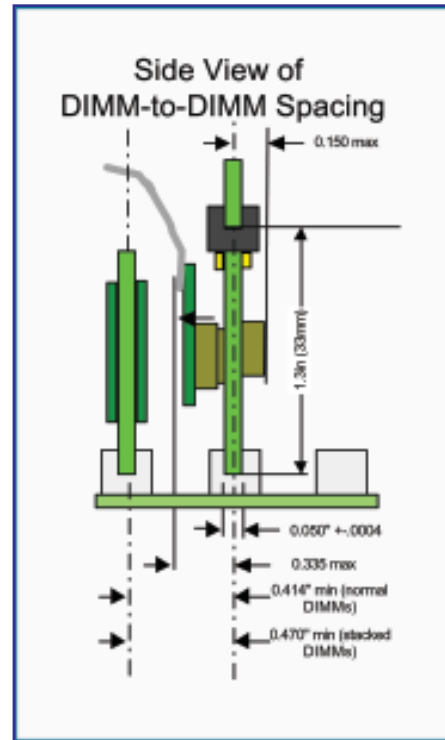
The FS2332 supports the 240-pin, 333 MHz clock (667 MT/s data rate), 64-bit, unbuffered synchronous double data rate (DDR) DRAM, dual in-line memory module (DDR SDRAM DIMM). It also supports slower versions that use a 100 MHz (200 MT/s data rate) or a 133 MHz clock (266 MT/s data rate) DDR SDRAM DIMM. Both registered and non-registered DIMM's are supported.

### Connecting to the Logic Analyzer

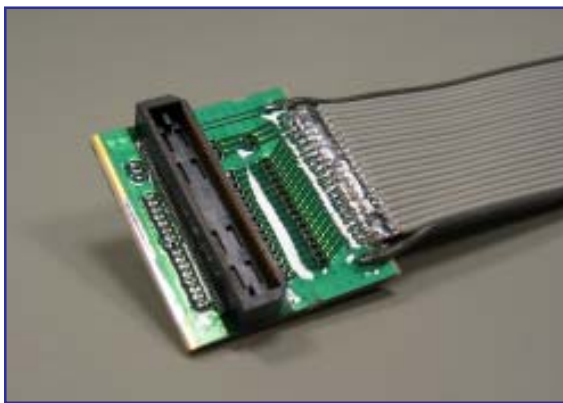
The FS2332 attaches to the logic analyzer with termination adapters. Two are available.

### Connecting the Probe in Confined Spaces

For situations where the probe must be used in a slot adjacent to other DIMM modules, the FS1026 provides right angle egress to the logic analyzer module. The necessary impedance matching networks are included in the Termination Adapters.



The FS1026 termination adapter enables easy connection of the probe in the tight space between two adjacent memory slots.



The FS1026 Right-angle Termination Adapter

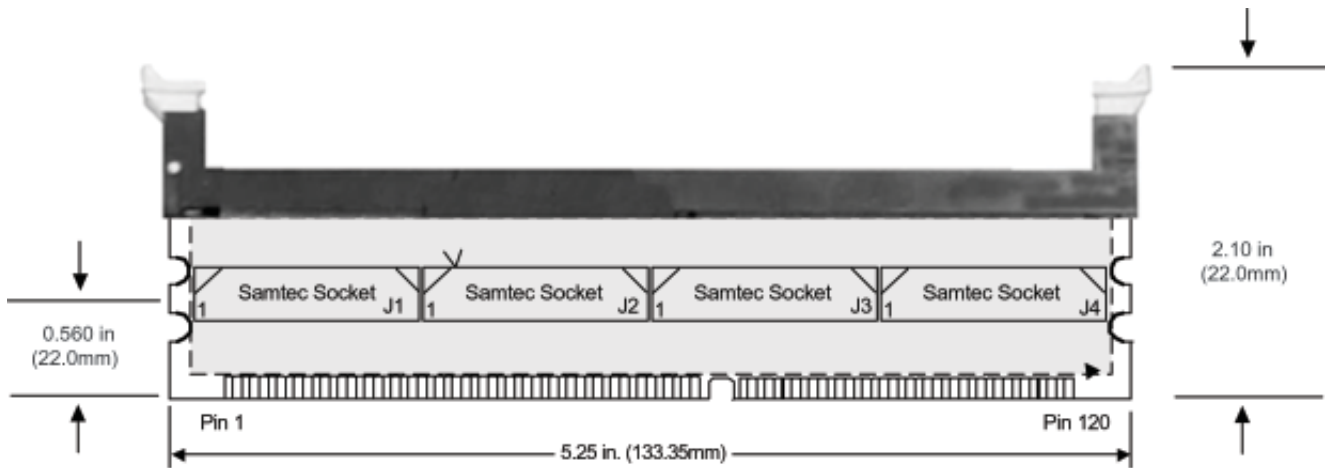
### Power Requirements

Power for the FS2332 is supplied by the logic analyzer. The analysis probe does not require any power from the DDR bus.

62	Active	0	1
	Bank = 0		
	Row Address = FF7		
63		1	1
64		1	1
65		1	1
66		1	1
67		0	1
68	Write	0	1
	Bank = 0		
	Address = FF7 38		
	Data = 80808080	80808080	
	Data = 80808080	80808080	
	Data = 80808080	80808080	
	Data = 80808080	80808080	
69		1	1

This display capture shows the typical output of the protocol decoder. The protocol decoder contains a filter that allows post filtering of any states including the *Not Selected* state, which is defined as a state that has no command or data associated with it.

## FS2332 Mechanical Dimensions



### Agilent Logic Analyzers Supported

#### Supported Logic Analysis Systems:

**Agilent** 16700A/B, 16702A/B, 16900A and 16902A  
(All systems require a logic analysis module)

**Please Note:** For the most up-to-date information about logic analyzer compatibility, please check the FuturePlus Systems web site.

### Logic Analyzer Module Requirements

The FS2332 requires up to four logic analyzer cards depending on whether protocol decode (double probed) or timing analysis is being used. A fifth card may be required if all \*DQS and SPD-EEPROM signals must be observed simultaneously.

### Supported Logic Analysis Modules

- 16717A, 16718A, 16719A (4 pods)
- 16750A, 16751A, 16752A (4 pods)
- 16753A, 16754A, 16755A, 16756A (4 pods)
- 16760A (2 pods)
- 16950A (4 pods)

### Ordering Information

<b>FS2332</b> .....	667 MT/s DDR Analysis Probe
<b>FS1026</b> .....	Termination adapter, right angle egress (4 required)
<b>E5378A</b> .....	Termination adapter - Order from Agilent Technologies (4 required)

**We offer excellent technical support and quick delivery.**

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Also, visit our web site at [www.futureplus.com](http://www.futureplus.com).

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