



PCI LOCAL BUS

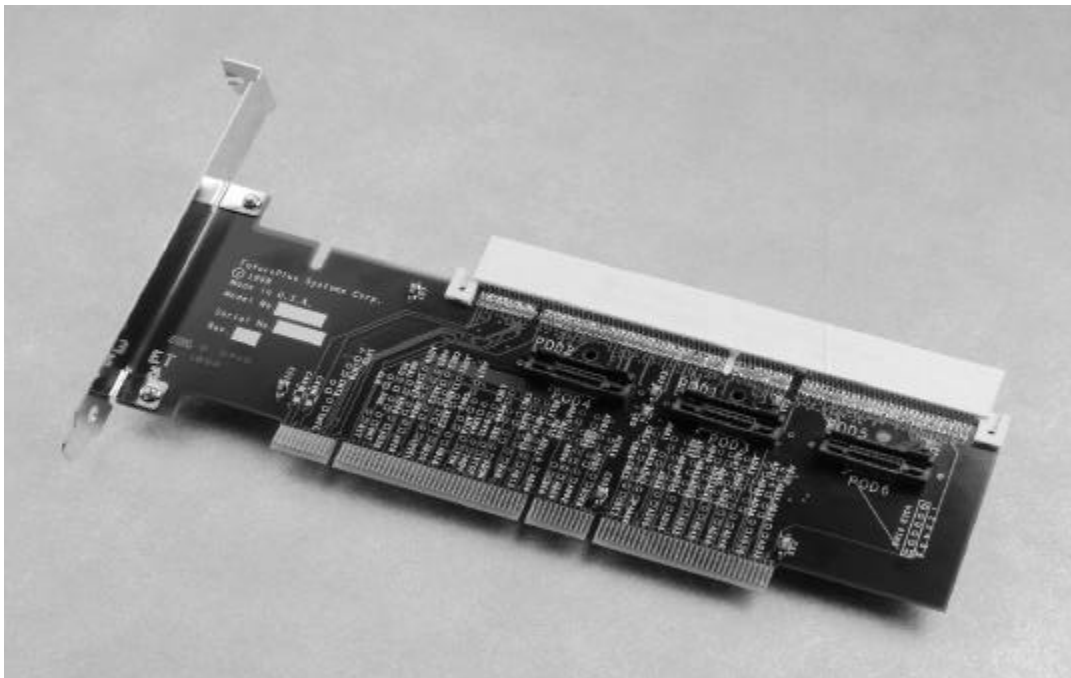
PCI Bus 66 MHz Passive Analysis Probe And Extender Card

For use with Agilent Logic Analyzers

The FS2005 and FS2006 are designed for the high end desktop market place. They contain an extender card connector for the add-in card under test, and a "right next to the bus" timing analyzer connection. Below are the features of the FS2005 and FS2006.

Features

- 3.3v (FS2005) or 5.0v (FS2006) operation
- 32 or 64 bit PCI bus monitoring
- 33 or 66 MHz operation
- Accurate timing analysis to 500 MHz (Logic Analyzer) or 4 GHz
- Logic Analyzer Configuration Software gets you up and running *fast*
- Use the ease of state triggering to capture and view timing problems
- PCI bus transaction inverse assembly software designed for easy software and hardware debug
- Short card form factor and simple logic analyzer connection allows easy *in-system* debug
- Support for Agilent's System Performance Analyzer allows key PCI performance metrics to be viewed in chart or histogram mode
- Test points give access to high speed timing analysis or an oscilloscope.



FS2005 / FS2006 PCI Bus Passive Analysis Probe

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FS2005 and FS2006 Description

The FuturePlus® PCI Passive Analysis Probe and extender card provides three functions:

- 1) Acts as an PCI extender card, extending the PCI card under test to provide access for additional probing. NOTE: The Extender card functionality is obtained through the use of the straddle mount connector located at the top edge of the FS2005 or FS2006. There are no buffers between the PCI local bus and the extender card connector. The etch from the PCI local bus is less than 3.5 inches and is of near equal length. Due to the extension of the etch length, operation is not guaranteed in all systems. The connector on the top of the card is either a 3.3 version (FS2005) or 5.0v version (FS2006). The card edge of the FS2005/2006 is a universal card edge so the FS2005/2006 can operate in either a 3.3v or 5.0v system.
- 2) Provides an electrical and mechanical interface to Agilent logic analyzers for passive PCI bus monitoring.
- 3) Provides test points to measure the power and signal fidelity of the PCI bus.

The PCI inverse assembly software executes in the Agilent logic analyzer. In State Analysis mode, the analyzer master clock is the PCI clock. The bus disassembler software decodes the key PCI bus signals and presents a readable display that lists the transaction type, address, data and key status conditions such as wait states and retries. The software also supports user-defined symbols that can be easily added to the state listing display. With the Agilent logic analyzers, the user can also select post-processing filters which allow the acquired data to display only chosen transactions. To assist with triggering, pre-defined resource terms have been included that can be used to prevent WAIT and IDLE states from being acquired, thus saving trace memory and providing an easier-to-read state display.

FuturePlus Systems also provides a PCI bus triggering application note to all PCI Bus Analysis Probe customers. An optional inverse assembler is also supplied called "PC Mapper". This inverse assembler allows the user to display bus transactions in terms of common PC accesses such as "video memory" or "RTC/CMOS RAM Data Port".

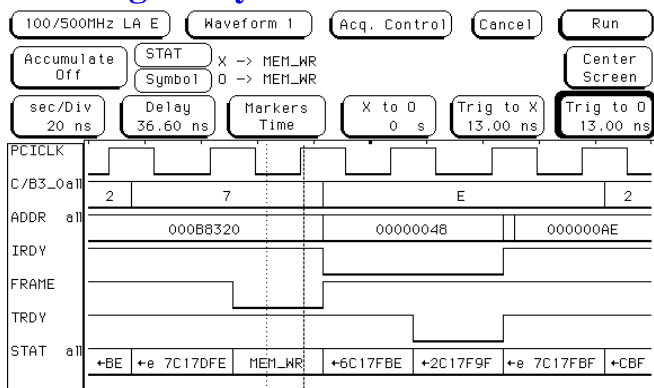
Cross-Domain Analysis

Are you analyzing data from multiple buses? Simply use this analysis probe to monitor the PCI bus, and then use another FuturePlus Systems analysis probe to monitor your other bus. We have analysis probes for many other buses. You can create your own custom measurement system, cross-domain trigger between buses, and view data from multiple buses simultaneously in the same display.

Additional Features

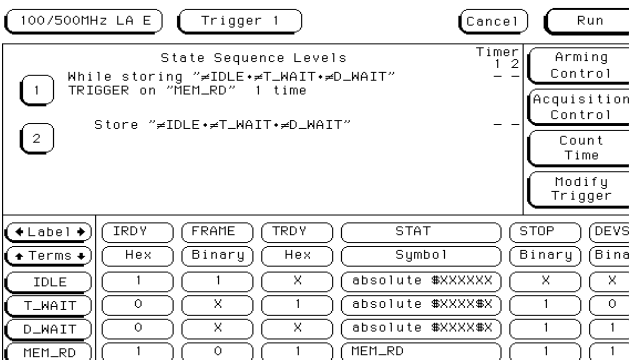
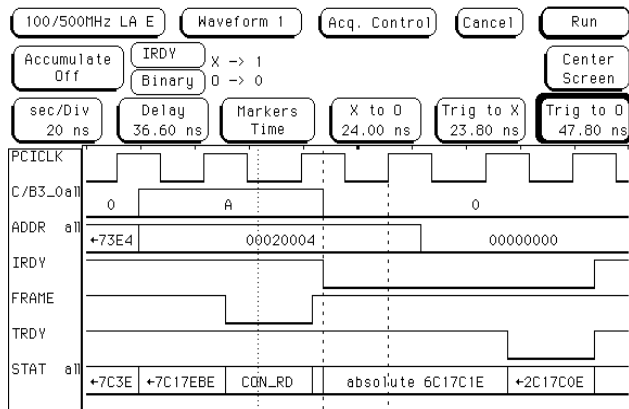
- Additional test points on all PCI signals can be used for high speed timing analysis or oscilloscope connection
- Enhanced Inverse Assembler operation available with the Agilent logic analyzers
- Extender Card edge connector supports bus analysis AND extender card functionality
- Two additional signals can be attached to the logic analyzer via user pins
- TDI/TDO jumper is provided so that the SCAN chain is not broken if an add-in card is not installed
- Mechanical notch allows for front plate clearance for board under test
- Mechanical offset of the card edge connector allows for easy installation and removal without system chassis modifications

Timing Analysis



Matched signal length, low capacitive loading, and no active buffering of the PCI signals makes the passive PCI Analysis Probe ideal for accurate and easy timing analysis.

The PCI Analysis Probe software contains pre-defined trigger terms that help track down those hard-to-find bugs.



State Analysis

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
242	D32=xxxxxxxx08	296 ns
243	I/O READ ADR=00000073	9.072 us
244	D32=23xxxxxx	1.096 us
245	I/O WRITE ADR=00000020	10.97 us
246	D32=xxxxxxxx20	168 ns
247	INTERRUPT ACK CYCLE	54.90 ms
248	D32=xxxxxxxx08	296 ns
249	I/O READ ADR=00000073	9.904 us
250	D32=23xxxxxx	1.128 us
251	I/O WRITE ADR=00000020	10.97 us
252	D32=xxxxxxxx20	168 ns

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
950	CONFIG READ ADR=80000000	8.960 ms
963	FUNC=0 REG=0 TYPE=00	
964	DEVICE ID=4158 VENDOR ID=1002	360.1 us
964	IDLE	32 ns
965	CONFIG READ ADR=0008000C	27.00 us
965	FUNC=0 REG=3 TYPE=00	
966	BIST=00 Hdr_Typ=00 Lat_Tmr=00 CLS=00	264 ns
967	IDLE	32 ns
968	CONFIG READ ADR=00080008	31.40 us
968	FUNC=0 REG=2 TYPE=00	
969	CLASS CODES:03 00 00 REV ID=00	264 ns
970	IDLE	40 ns

With certain Agilent products, PCI Bus transaction inverse assembly options post-process the acquired data. This feature allows the user to customize the display to show only the transactions or cycles that are of interest.

Label>	PCI BUS TRANSACTIONS	Time
Base>	REV 2.2	Relative
12	MEM READ ADR=000FE060	264 ns
13	D32=A5837102	3.608 us
14	MEM READ ADR=000FE064	200 ns
15	D32=A6A6C5A5	3.536 us
16	MEM READ ADR=000FE068	296 ns
17	D32=B6C54471	3.568 us
18	MEM READ ADR=000FE06C	200 ns
19	D32=A6B566F5	3.536 us
20	MEM READ ADR=000FE070	304 ns
21	D32=A5560471	3.560 us
22	MEM READ ADR=000FE074	200 ns

PCI Bus Inverse Assembly Options

- Wait Cycles:
 - I/O Reads:
 - I/O Writes:
 - Configuration Reads:
 - Configuration Writes:
 - Memory Reads:
 - Memory Writes:
 - Idle Cycles:
 - All Other Transactions:
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Ordering Information

FS2005 32/64 bit PCI Local Bus Passive Analysis Probe & Extender, 66 MHz - 3.3V

FS2006 32/64 bit PCI Local Bus Passive Analysis Probe & Extender, 66 MHz - 5V

Termination Adapters

Agilent E5346A Termination Adapter - 2 or 3 required (for 40-pin connection)

Agilent E5380A Termination Adapter - 2 or 3 required (for 90-pin connection)

Software included with the FS2005 or FS2006:

Configuration files for the Agilent logic analyzer

Protocol Decoder software, runs on the Agilent logic analyzer

Logic Analyzer Requirements

- For 32-bit protocol or timing analysis, the FS2005 and FS2006 require 4 logic analyzer pods with a 33 MHz minimum state analysis speed
- For 64-bit protocol or timing analysis, the FS2005 and FS2006 require 6 logic analyzer pods with a 33 MHz minimum state analysis speed
- For 40 pin Agilent logic analyzer modules you will need one Agilent E5346A Termination Adapter for each two pods to connect to the FS2005 and FS2006
- For 90 pin Agilent logic analyzer modules you will need one Agilent E5380A Termination Adapter for each two pods to connect to the FS2005 and FS2006

Please note: for the most up-to-date information about Agilent logic analyzer compatibility, please check the FuturePlus Systems website at:
http://www.futureplus.com/products/fs2005/fs2005_sysreq9.shtml



More information and application notes are on the FuturePlus Systems website at:
<http://www.futureplus.com/products/fs2005>

We offer excellent technical support and quick delivery.

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