



FS1105 Compliance Verification Consultant FS1106 Performance Verification Consultant

Software for use with Agilent Logic Analyzers

FuturePlus Systems offers software-only solutions for analysis of PCI data captured with Agilent logic analyzers. The **FS1105** provides PCI bus compliance verification functionality, while the **FS1106** provides PCI bus performance verification functionality. Whether you have a standard PCI Local Bus or an embedded PCI bus with a non-standard connection, owning and using these products is like adding a full time PCI consultant to your staff or design team!

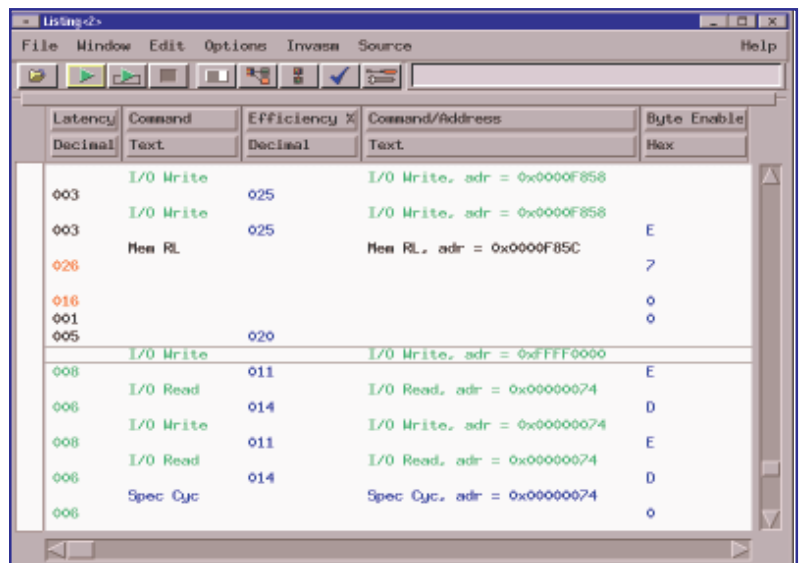
FuturePlus® FS1105 and FS1106 General Features

- Post-processing software provides passive-probe users with comprehensive, flexible performance and compliance verification.
- Decode all PCI command and cycle types.
- Color coded transaction display matches the command for easy correlation.
- Data labels are automatically transferred when the logic analyzer is switched into timing mode.
- Add value to your existing Agilent and FuturePlus investment without the need for expensive add-on hardware.
- Post-processing is done on your Agilent logic analyzer, so there's no need to download to a PC.
- It's like having your own full-time consultant.

Quick, Easily Customized Configuration

The FS1105 and FS1106 software tools take the input labels from the passive PCI configuration file FORMAT menu and generate columns in the listing screen. These columns will decode the PCI bus traffic in an easy to read format and provide additional performance or compliance information.

These applications include several sample configuration files that match the passive PCI products from FuturePlus Systems. For custom pinouts, use any of these files and modify them to match your own custom configuration. The configuration software sets up the format specification menu of the logic analyzer for compatibility with the specified FuturePlus PCI analysis probe. Once installed, the Compliance or Performance Consultant software will appear as an icon in the CUSTOM area of your workspace.

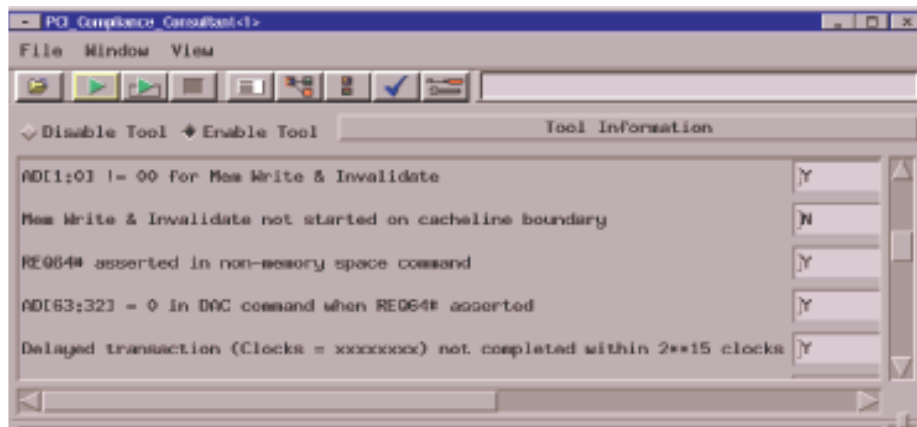


Latency Decimal	Command Text	Efficiency % Decimal	Command/Address Text	Byte Enable Hex
003	I/O Write	025	I/O Write, adr = 0x0000F858	
003	I/O Write	025	I/O Write, adr = 0x0000F858	E
026	Mem RL		Mem RL, adr = 0x0000F85C	7
016				0
001				0
005		020		
	I/O Write		I/O Write, adr = 0xFFFF0000	
008	I/O Read	011	I/O Read, adr = 0x00000074	E
008	I/O Read	014	I/O Read, adr = 0x00000074	D
008	I/O Write	011	I/O Write, adr = 0x00000074	E
006	I/O Read	014	I/O Read, adr = 0x00000074	D
006	Spec Cyc		Spec Cyc, adr = 0x00000074	0

The FS1105 and FS1106 applications generate columns that decode the PCI bus traffic in an easy-to-read format. Transactions are color coded to match the associated command.

Key Features of the FS1105 Compliance Consultant

- Verifies 26 different compliance rules.
- Allows quick, easy masking of each compliance rule.
- Filters out the input data set to present an uncluttered display.
- Post-processing software provides passive-probe users with comprehensive compliance verification.



The FS1105 software removes the raw PCI bus signals from the output display for easy reading. However, these signals are important and can quickly be added back into the display. Once this is done, the FS1105 output will appear beside the acquired PCI bus signals.

Columns generated by the FS1105 PCI Compliance Consultant Tool

Name	Description
Command	The command name
Address_H	The address as it appears during a 64 bit address transfer (as defined by a DAC)
Address_L	The address as it appears on the lower AD lines (AD[31:0]). This HEX value is incremented during burst transactions
Data_L	The lower 32 bit AD lines representing data
Data_H	The upper 32 bit AD lines representing data
Byte_Enable_H	High order data byte enables
Byte_Enable	Low order data byte enables
Termination	Termination type
TERM CODE	Termination type displayed in HEX (for use in SPA and filter tools)
CMD	The command type displayed in HEX (for use in SPA and filter tools)
Clocks	The number of clock tics that have elapsed. This takes into consideration those states filtered out by the Trigger menu store qualification.
Num Byte Enables	Number of byte enables asserted for that data transfer
Rule	The rule number corresponding to the violation seen
Description	A description of the violation found
Any Error	Can be used by the search function in the lister to quickly locate an error

PCI Compliance Rules Checked by the FS1105

Rule Number	Name	Description
1	Illegal control signal asserted during IDLE	Section 3.2.1 Basic Transfer Control
2	PERR# asserted without a parity error	Section 3.7.4.1 Data Parity Error signaling on PERR#
3	PERR# not asserted for parity error	Appendix C Rule 37c
4	Parity error	Appendix C Rule 37b and c
5	Illegal control signal asserted during Address Phase	Section 3.2.1 Basic Transfer Control
6	Reserved Command	Section 3.1.1 Command Definition
7	AD[1:0] !=00 for Mem Write and Memory Write Invalidate	The FS1105 checks for linear incrementing. Section 3.2.2.2 Memory Space Decoding
8	Mem Write and Invalidate not started on cacheline boundary	The FS1105 checks for cache aligned accesses per the input given by the user. Section 3.2.2.2 Memory Space Decoding
9	REQ64# asserted in non-memory space command	Section 3.10 64 bit bus extensions
10	AD[63:32]=0 in DAC command when REQ64# asserted	Section 3.10.1 64 bit Addressing on PCI
11	Delayed transaction (Clocks = xxxxxxxx) not completed within 2**15 clocks	Agilent Rule to detect potential deadlocks
12	Delayed transaction (Clocks = xxxxxxxx) not retried within 2**14 clocks	Agilent Rule to detect potential deadlocks
13	Illegal control signal asserted 2nd address phase of DAC	3.9 64 bit addressing on PCI
14	Reserved or DAC command in the 2nd address phase of a DAC	3.9 64 bit addressing on PCI
15	FRAME# deasserted illegally.	FRAME# cannot be deasserted unless IRDY# is asserted. Appendix C rule 8c
16	REQ64# asserted in non-memory space command	Section 3.9 64-bit Bus Extensions
17	Inconsistent address in 64-bit transfer	"Inconsistent address" means that AD[63:32] does not equal AD[31:0] in the first address phase.
18	High address must be non-zero	3.9 64 bit addressing on PCI
19	Illegal control signal while waiting for DEVSEL#	In a DAC the upper address must be non zero.
20	DEVSEL# asserted after 5 clocks from FRAME#	3.9 64-bit addressing on PCI
21	FRAME# and IRDY# deasserted before 5 clocks and no DEVSEL#	Appendix C Rule 14 and 29
22	Transfer latency > 8 clocks	Section 3.3.3.1 Master Initiated Termination
23	IRDY# latency > 8 clocks	Section 3.3.3.1 Master Initiated Termination
24	TRDY# initial latency > 16 clocks	Appendix C Rule 27
25	TRDY# subsequent latency > 8 clocks	Appendix C Rule 27
26	DEVSEL# asserted during a special cycle	Appendix C Rule 25

Key Features of the FS1106 Performance Consultant

- Indicates burst length, byte enables and number of byte enables, color coded to match the associated command.
- Provides a quick summary of the traffic through the Command/Address and Length/Termination labels.
- Determines the following performance metrics:
 - Latency: data-to-data and address-to-first data.
 - Byte-enable and Total efficiency
 - Total Efficiency
 - Overall Time Efficiency

Columns Generated by the FS1106 PCI Performance Consultant Tool	
Name	Description
Command	The command name
Address_H	The address as it appears during a 64 bit address transfer (as defined by a DAC)
Address_L	The address as it appears on the lower AD lines (AD[31:0]). This HEX value is incremented during burst transactions
Data_L	The lower 32 bit AD lines representing data
Data_H	The upper 32 bit AD lines representing data
BE_H	High order data byte enables
BE_L	Low order data byte enables
Latency	Number of states between data phases or if the first data phase the number of states between address and first data phase. This label is color coded to indicate spec compliance. Green indicates within spec, yellow indicates marginal, and red indicates out of spec.
Termination	Termination type
Command/Address	A summary giving the command and starting address
Length/Termination	A summary giving the length of the data transfer and the termination
TERM CODE	Termination type displayed in HEX (for use in SPA and filter tools)
CMD	The command type displayed in HEX (for use in SPA and filter tools)
Clocks	The number of clock tics that have elapsed. This takes into consideration those states filtered out by the Trigger menu store qualification
Burst Length	The length of the transaction in bytes and indicated at the end of the transaction
Num Byte Enables	Number of byte enables asserted for that data transfer
Byte Enable Efficiency %	Byte enable efficiency Data clocks (taking into consideration the Byte enables)/Total clocks in percent
Efficiency %	Time efficiency of the transaction. Data Clocks/Busy Clocks.
Total Efficiency %	Time efficiency * Byte enable efficiency
Mbytes/sec	Burst Length/Transaction time

Supported Agilent Logic Analyzers

The FS1105 and FS1106 are supported on the Agilent 16700A/B and 16702A/B logic analysis systems. The logic analyzer must also have one or more of the following logic analysis modules installed:

16715A through 16719A
16740A through 16742A
16750A through 16752A

Note: Agilent Technologies continually updates its product offerings. Please check the the FuturePlus web site at www.futureplus.com for an up-to-date list of supported logic analyzers.

Supported FuturePlus Analysis Probes

In addition to custom probing solutions, the FS1105 and FS1106 post-process data from the following FuturePlus PCI Analysis Probes:

FS2000 FS2001 FS2004 FS2005
FS2006 FS3010 FS3020 FS3030

Licensing

The FS1105 and FS1106 are licensed to be used on a single Agilent 16700-series frame. You can download both products from the FuturePlus website and take a look at the included demo workspace on your Agilent 16700A/B or 16702A/B. A demo time is provided by typing the word "demo" into the licensing area next to the product name. The licensing area for the 16700-series mainframe is found under *System Administration*. To continue using the software beyond the demo period, please contact FuturePlus Systems at sales@futureplus.com, or call (719) 278-3540.

Ordering Information

FS1105PCI Compliance Verification Consultant Software
FS1106PCI Performance Verification Consultant Software

FuturePlus Systems provides excellent technical support and quick delivery.

Ask about our free quarterly newsletter, *The Bus Analyzer*

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