REV 2.2

CAPTURING USB BUS TRANSACTIONS

USING THE FUTUREPLUS SYSTEMS USB ANALYSIS PROBE (FS4100) AND LOGIC ANALYZER ©

This application note is designed to help USB Analysis Probe users trigger their logic analyzers in order to capture USB bus transactions and events. Effectively using the trigger specification coupled with appropriate store qualifications ensures the optimum use of the analyzer memory and the best probability of capturing the desired event. The USB Analysis Probe software comes with preconfigured symbols to help get one started.

ANALYSIS PROBE OPERATION

The USB Analysis Probe is designed to optimize the use of the analyzer memory:

- It does not send data to the analyzer when the bus is in an idle state.
- When it detects that the bus has been SUSPENDED, it sends the SUSPEND status and sends the RESUME status once the bus transitions to the RESUME state.
- In the case of a RESET state the Analysis Probe reports USB RESET when it detects the reset and RESET END when the reset deasserts, thus the duration of USB RESET may be determined.
- The USB Configuration Files define the PID variable. This variable details the USB packet type and packet related errors such as crc, bitstuffed, invalid or bad PID. (See Appendix A for a complete list of errors).There is a status called ANY ERROR, this is a catch all error status, if any error condition is detected such as a data crc error, the crc error status will be clocked to the analyzer followed by the ANY ERROR status.

OPERATIONAL MODES:

The following is a description of three ways that the Analysis Probe and THE AGILENT Analyzer may be used to capture USB traffic.

STATE MODE:

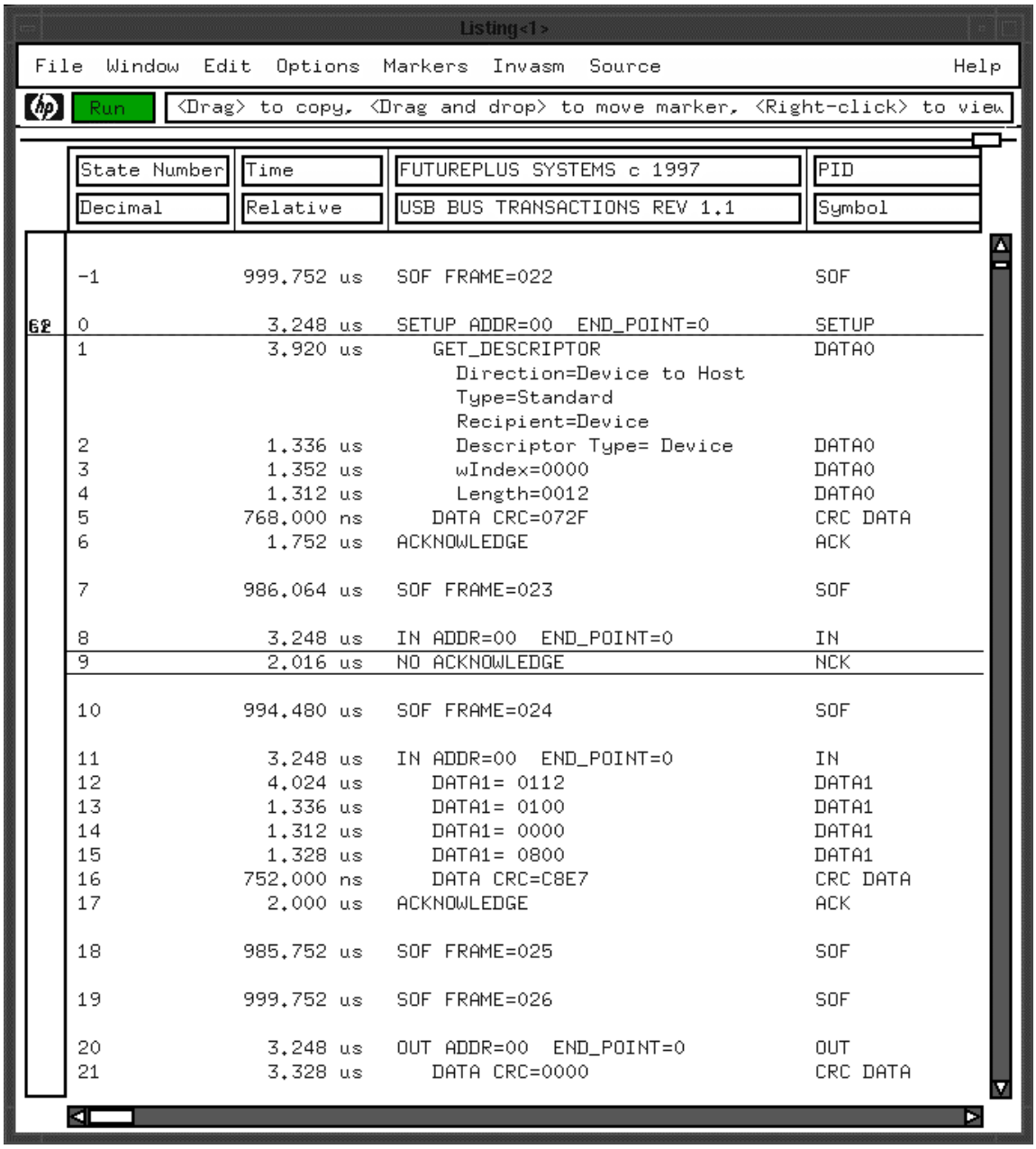
State Mode allows the user to view all USB traffic as transactions or command types, this mode uses the data brought in on PODS 1 and 2. In

state mode the user can trigger on any one of or combination of the following variables.

- The **PID** variable allows for triggering on or filtering out certain transaction types or errors. (Refer to Appendix A for a complete list).
- The FS4100 latches and holds the address and endpoint of a token packet so that all traffic directed at a particular address and or endpoint (Pipe) may be captured. The symbols **ADR** and **ENDPT** can be set so that the user can capture only the cycles that are directed to a particular destination .
- **CTLCMD** This variable allows for triggering on Command types, see appendix B for a full description of this variable.
- **DATA** allows the user to trigger on a data pattern i.e. actual data or CRC data.

Note the symbols STAT and ADDR which appear under the Format are software only symbols and should not be used in triggering or filtering

The following picture is an example of data captured in state mode with the FS4100 and the analyzer (16505A).



SERIAL BIT STREAM ANALYSIS:

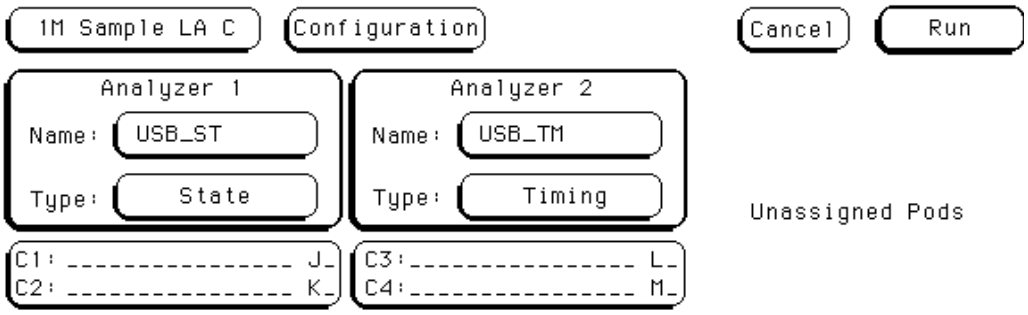
The second mode of operation is for ***Serial Bit Stream Analysis.*** This uses POD 3 (and POD 4 if desired) coupled with the **Timing Mode** of the analyzer.

PODS 1 and 2 may be viewed in timing mode but exercise care when looking at the values on the variables. The values on the variable PID is held until the next transaction is received unless the current transaction had an error on it. The ADR and ENDPT values are held from one Token packet until the next token packet is received. Data is clocked up two bytes at a

time. Hence during an Idle period on the bus these variables will hold the values of the last transaction.

COMBINATION MODE:

The third mode of operation is the ***Combination mode***, this is the default mode set up by the software shipped with the Analysis Probe. The configuration is as follows:



It is very useful to trigger the timing machine (analyzer 2) from the state capture machine (analyzer 1) when looking for glitches on VP or VM.

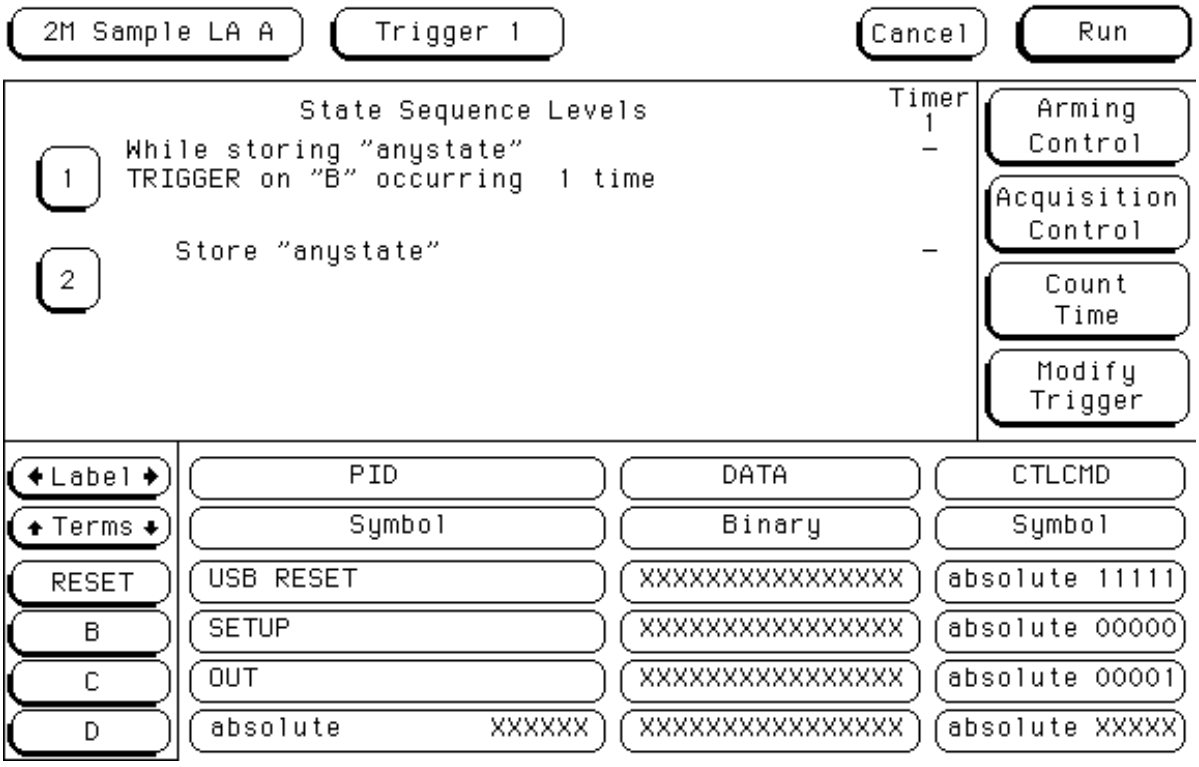
Appendix D reviews some of the key triggering and store terms for the 16500 mainframe.

The signals VP, VM and RCV are listed on POD 4. For access to these signals use a flying lead set attached to the FS4100 test points.

STATE MODE ACQUISITION:

Triggering on the first occurrence of a transaction.

If it was desired to capture the enumeration sequence for a newly attached device then triggering on the first Setup packet and putting the trigger at the start of Acquisition memory is what is required. The following is a trigger that would find the first SETUP packet.



Trigger condition “B” is set to look for a SETUP PID, once a SETUP PID is encountered the analyzer will trigger and fill its memory with all the subsequent transactions. The user may place the Trigger at the desired place in memory, placing the trigger at the beginning of memory will allow the user to capture the maximum packets after the event.

Triggering on traffic to a particular address and endpoint.

This trigger will trigger on the first occurrence of the ADR/ENDPOINT and then store only traffic to that ADDRESS and ENDPOINT.

Trigger 1 (Analyzer 1 USB_ST)

State Sequence Levels

1 While storing “anystate”

Trigger on “B” 1 time

2 Store “ B”

< Label >	PID	ADR	ENDPT	DATA	CTLCMD
TERMS					
A	XX	XXX	XX	XXXX	XXXX
B	XX	04	01	XXXX	XXXX

Triggering on a particular Command.

The following trigger shows how to capture all the “SET_ADDRESS” commands issued by a host.

Trigger 1 (Analyzer 1 USB_ST)

State Sequence Levels

1 *While storing* “anystate**”**

Trigger on “B” 1 time

2 *Store “B”*

< Label >	PID	ADR	ENDPT	DATA	CTLCMD
TERMS					
A	XX	XXX	XX	XXXX	XXXX
B	XX	XX X	XX	XXXX	SET_ADDRESS

Triggering on Error conditions:

The FS4100 detects the following anomalous conditions crc errors, serial stuffed bit errors, bad and invalid PIDS, Start of Frame tokens sent at slow speed. If the FS4100 detects any of the above conditions it will send the appropriate status per Appendix A and additionally send the ANY ERROR status.

The following trigger shows how to capture an error condition.

Trigger 1 (Analyzer 1 USB_ST)

State Sequence Levels

1 *While storing* "anystate**"**

Trigger on "B" 1 time

2 *Store "B"*

< Label >	PID	ENDPT	DATA	CTLCMD
TERMS				
B	ANY ERROR	XX X	XXXX	XXXX

USB Serial Bit Stream Analysis:

Debug scenario, the device under test is missing transactions and the Analysis Probe is capturing them.

Place the Analysis Probe as close to the peripheral under test as possible, that is insert it between the device under investigation and its upstream port/hub. The device under test may be missing packets because it is not detecting a Sync pattern or it may be concatenating two packets together because it did not detect the end of packet.

CHECKING SYNC PATTERN (compliance checklist item FLT1)

Per the USB specification the sync pattern is a pattern of 00000001(KJKJKJKK), however the compliance checklist indicates that a device must be able to detect a sync pattern even if the first 2 bits are corrupted (FLT1).This sync pattern is not unique and can occur many times in DATA packets so this pattern is a sync pattern only when the bus has

been in the IDLE state previously. Hence to trigger on the true Sync Pattern trigger on the signal FEOSYNC coupled with the LBC3_0 state machine being in the IDLE state. The user can then make a determination as to whether the sync pattern seen on this segment of the USB meets specification.

Trigger 2 (Analyzer 2 USB_TM)

Timing Sequence Levels

1 *While storing* "anystate"

Trigger on "B" 1 time

< Label >	LBC3_0	FEOSYNC
TERMS		
A	XX XX	X
B	IDLE	1

CHECKING FOR A BAD END OF PACKET.

If the FS4100 operating in full speed mode, detects a valid SE0 for at least 60ns but a valid J_STATE does not follow, it will do the following.

1. Pass the packet up to the logic analyzer.
2. Pass a " POSSIBLE BAD EOP" status to the analyzer.

If the FS4100 operating in slow speed mode, detects a valid SE0 for at least 300ns but a valid J_STATE does not follow, it will do the following.

1. Pass the packet up to the logic analyzer.
2. Pass a "POSSIBLE BAD EOP" status to the Analyzer.

A status of "POSSIBLE BAD EOP" should be treated as cautionary and the user would be advised to view the received signals in timing mode by doing the following.

1. Attach POD 3 of the analyzer to POD 3 of the USB Analysis Probe.
2. Attach a flying lead set to stake pins RCV, VP and VM.
3. In state mode trigger on PID " POSSIBLE BAD EOP". Using the arming control trigger the timing Analyzer from the State Analyzer.
4. Once the State Analyzer Triggers switch to Timing Analyzer Waveform 2.

BIT WIDTH VIOLATION:

The following trigger may be used to check the bit width of the USB received data RCV.

Trigger 2 (Analyzer 2 USB_TM)

Timing Sequence Levels

Trigger on “Edge 1” occurring within 40ns after “Edge 1”

Set Edge 1 to look for either a rising or falling edge on the RCV signal.

(RCV signal is on POD 4).

USB COMBINATION MODE ACQUISITION:

If one has captured something in state mode and wants to see what was happening on the POD3/POD4 signals either before or after this state mode event then set the USB_ST to trigger the USB_TM.

To set this mode up,

- Enter the Trigger 1 menu, set the state trigger event that is desired.
- Then under the label ARMING CONTROL select the USB_SM to be triggered by the RUN option.
- Set the USB_TM machine to trigger from the USB_ST machine.
- Note that there is an ARM_OUT option, this may be used for triggering the oscilloscope which can be used to monitor the USB signals D+ and D-.

Trigger 1 (Analyzer 1 USB_ST)

State Sequence Levels

1 *While storing* “anystate”

Trigger on “B” 1 time.

2 *Store “B”*

< Label >	PID	ADR	ENDPT	DATA	CTLCMD
TERMS	STALL	XXX	XXX	XXXX	XXXX

Trigger 2 (Analyzer 2 USB_TM)

Timing Sequence Levels

Trigger on “arm” 1 time

USB CORRELATED WITH OTHER BUSES

The USB Analysis Probe may be used in conjunction with other Analysis Probes that are supported on the Logic Analyzer such as the PCI Analysis Probe. Using these two Analysis Probes allows the user to understand the timing relationship between transactions on the two buses.

APPENDIX A: PID VARIABLE

Symbol	Binary Code	Comment
IDLE	000000	IDLE STATE
SETUP	000001	SETUP
IN	000010	IN
OUT	000011	OUT
SOF	000100	START OF FRAME
DATA0	XX0101	DATA0
CTL DATA0	1X0101	SETUP DATA0
DATA1	XX0110	DATA1
CTL DATA1	1X0110	SETUP DATA1
CRC DATA	000111	CRC DATA
PRE	011000	PREAMBLE
ACK	011001	ACKNOWLEDGE
NCK	011010	NO ACKNOWLEDGE
STALL	011011	STALL
USB RESET	111111	USB RESET
RESET END	111001	USB RESET DEASSERTED
INVALID	011101	INVALID PID RECEIVED
BAD PID	011110	BAD PID RECEIVED
SUSPEND	111110	SUSPEND CONDITION DETECTED
RESUME	111101	RESUME CONDITION DETECTED
KEEP ALIVE	111011	KEEP ALIVE
SETUP SBS ERROR	001001	SETUP PACKET WITH SERIAL BIT STUFFED ERROR DETECTED
IN SBS ERROR	001010	IN PACKET WITH SERIAL BIT STUFFED ERROR DETECTED
OUT SBS ERROR	001011	OUT PACKET WITH SERIAL BIT STUFFED ERROR DETECTED
SOF SBS ERROR	001100	START OF FRAME SERIAL BIT STUFFED ERROR DETECTED
DATA0 SBS ERROR	001101	DATA0 PACKET WITH SERIAL BIT STUFFED ERROR DETECTED

DATA1 SBS ERROR	001110	DATA1 PACKET WITH SERIAL BIT STUFFED ERROR DETECTED
CRC DATA SBS ERR	001111	CRC DATA WITH SERIAL BIT STUFFED ERROR DETECTED
SETUP CRC ERROR	010001	SETUP PACKET WITH CRC ERROR DETECTED
IN CRC ERROR	010010	IN PACKET WITH CRC ERROR DETECTED
SOF CRC ERROR	010100	START OF FRAME PACKET WITH CRC ERROR DETECTED
OUT CRC ERROR	010011	OUT PACKET WITH CRC ERROR DETECTED
CRC DATA CRC ERROR	010111	CRC DATA WITH CRC ERROR DETECTED
ANY ERROR	111000	ERROR SUMMARY STATUS
SLOW SPEED SOF	011111	SOF TOKEN DETECTED AT SLOW SPEED
RES SE0	111100	SE0 AT THE END OF RESUME SIGNALING
RES JSTATE	111010	J STATE sent after RESUME_SE0
POSSIBLE BAD EOP	110111	POSSIBLE BAD END OF PACKET, INCORRECT J STATE DETECTED.
SLOW SPEED SOF	011111	SOF DETECTED AT SLOW SPEED

APPENDIX B: CTLCMD VARIABLE

Standard Device Requests
GET_STATUS
CLEAR_FEATURE
SET_FEATURE
SET_ADDRESS
GET_DESCRIPTOR
SET_DESCRIPTOR
GET_CONFIGURATION
SET_CONFIGURATION
GET_INTERFACE
SET_INTERFACE
SYNCH_FRAME

APPENDIX C

The Format Menu

The USB Analysis Probe diskette sets up the format menu as shown in the following table. To gain access to the signals listed under POD4, a flying lead set should be attached to the appropriate stake pins.

LABEL	POD 4	POD 3	POD 2	POD 1
STAT			15:11	16
ADDR			10:0	
DATA				15:0
ADR			10:4	
ENDPNT			3:0	
PID			15:11	16
CTLCMD			15:11	16, 15:0
MCLK				
CLK12		16		
MDATA		15		
SOFTIC		14		
EOP2_0		13:11		
LBC3_0		10:7		
RST2_0		6:4		
FEOPR		3		
FEOSYNC		2		
LSDET		1		
UNUSED		0		
VP	2			
VM	1			
RCV	0			

APPENDIX D

The Acquisition Control Field

In the 16500 mainframe, the Acquisition Control field can be found on the right hand side of the trigger menu and can be used to access the Acquisition Control menu. The Acquisition Control menu is used to set the acquisition mode and trigger position within available memory.

The Acquisition Mode Field

The Acquisition Mode field toggles between Manual and Automatic. When set to Automatic in STATE mode, the trigger position is computed based on the sequence specification. In TIMING mode, the trigger position and the sample period is computed based on the sec/Div and the delay settings in the Waveform menu.

When the Acquisition Mode field is set to Manual, additional configuration fields become available. Use these fields to further qualify what data is stored.

The Trigger Position Field

The trigger Position Field accesses a selection menu with the options of Start, Center, End or User Defined. When an option is selected, that point of the available memory is positioned relative to the trigger. In TIMING mode, the start of the acquisition can also be delayed.

Branches Taken Stored/Not Stored

The Branches Taken field is a toggle field which sets the analyzer to store, or not to store, the resource term that sent the analyzer off on a branch. The trigger specifications shown in this application note assume that this field is set to Branches Taken Stored.

For more detailed information please refer to the User's Reference of your Hewlett-Packard Logic Analyzer.

Using Symbols

In the 16500 mainframe, the SYMBOLS button can be found in the upper right hand corner of the FORMAT menu. Once selected, the user can set up symbols for any label listed in the FORMAT menu. These symbols can be added to or deleted. The user can create new labels in the format menu and these labels can be any combination of USB signals and symbols that are acquired by the USB Analysis Probe.

Additional information on triggering can be found in Hewlett-Packard Application note 1223 *Logic Analyzer Triggering Applications*. This application note can be obtained from your local Hewlett-Packard sales representative.

For more information on the USB Analysis Probe please contact:

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