

Hyper Transport CRC Alignment
Application Note for FS2240 Analysis Probe
© FuturePlus Systems, Corp February 24, 2003
Revision 1.0

Introduction

The HyperTransport link incorporates a CRC error detection scheme. This paper is intended to be a guide for determining the correct CRC value to be entered in the FuturePlus FS2240 software to insure proper protocol decode.

Section 10.1.1 Transmission Errors from the HyperTransport 1.05 specification is contained at the end of this document. Table 1 of the specification is included and provides an excellent overview of the data structure and the CRC function. If you are unfamiliar with the CRC function this section should be reviewed before reading the rest of this application note.

FuturePlus FS2240 HyperTransport Analysis Probe Implementation

By its very nature an analysis probe is designed to capture data around a specific time or event that is defined by the user. This almost always occurs a significant amount of time after the link comes out of reset.

When the HyperTransport link comes out of a reset state it generates a link synchronization message. This message is the synchronization sequence between all of the devices on the link. As long as the CRC values are correct, the link will not send out another link/error synchronization message.

When the control bit (CTL) is asserted (1) the data on the link will be a command, the lower 40 bits of address, the upper 40 bits of address(version 1.05 or later), or a CRC. When the link analysis probe captures the link traffic, assuming this occurs some time after reset, the analysis probe software has no way of identifying the difference between a command, address or a CRC.

Because the captured data on the link does not contain a reference point, the link synchronization message, the FS2240 analysis probe is unable to properly decode the HyperTransport protocol. In order to insure correct disassembly of the trace data the user must provide a known starting point for the analysis probe to begin synchronization.

Since the CRC occurs every 512 bit times the protocol can be properly aligned once the user identifies the CRC value to the FuturePlus software..

To summarize these conditions:

- 1) The trace file most likely will not contain the link synchronization message
 - a. this only occurs at reset
- 2) Data sent from the FS2240 probe to the Agilent logic analyzer is in a 32 bit format
 - a. the 32 bit word contains 4 bit times for 8 bits
 - b. the 32 bit word contains 2 bit times for 16 bits.
- 3) The CTL bit is asserted (1) for a
 - a. CRC
 - b. the lower 40 bits of address
 - c. the upper 40 bits of address (in version 1.05)
- 4) The FS2240 software must be aligned to a known CRC value
 - a. this value is determined and then input by the user

Overview Of The FS2240 HyperTransport Analysis Probe

The FS2240 analysis probe converts the 8 or 16 bit links into a complete 32 bit packet for transmission to the logic analyzer. Each 32 bit word contains four bit times.

Consequently, the format of the data contained in the trace file will differ slightly from the format specified in the HyperTransport specification.

- ? The 512 bit times of a CRC cycle are represented in 128 states ($512/4 = 128$). The CRC is reported 16 states (64 bit times) after its window is transmitted.
- ? A CRC is reported as the 17th state after the end of a CRC window.
- ? The FuturePlus FS2240 analysis probe converts the bit times to 32 bit state values.

This example below illustrates how the CRC location is converted from what is listed in Table 1 (from section 10.1.1 of the specification located at the end of this document) to the following format:

```

state 112 in the sequence      ✎ Window A-1
=====
: state                        ✎ CRC window A
:
: 16 states
:
: state 16                     ✎ CRC window A
CRC = 0xC6C7C940 (data state) ✎ CRC value for A-1, Window
: state 17                     ✎ CRC window A
:
: 112 states
:
: state 128                    ✎ CRC window A
=====
: state
:
: 16 states                    ✎ This is now CRC window B
:
: state 16
CRC = 0xC6C7C940 (data state) ✎ CRC value for Window A
: state 17
:
: 112 states                    ✎ CRC window B
:
: state 128
=====
: state
:
: 16 states                    ✎ This is now CRC window C
:
: state 16
CRC = 0xC6C7C940 (data state) ✎ CRC value for Window B
: state 17
:
: 112 states                    ✎ CRC window C
:
: state 128

```

The 512 bit times of a CRC cycle are represented in 128 states on the logic analyzer (512/4 = 128). The CRC is reported 16 states (64 bit times) after its window is transmitted.

A CRC is reported at the 17th state after the end of a CRC window.

The link synchronization at power-on reset is what enables each side of the link to count bit times. As long as the CRC values match the link assumes the bit times match. Only if the CRC value fails does the link generate a new link synchronization message to resynchronize the links.

The HyperTransport link assumes that both sides of the HyperTransport link will be counting bit times. This will allow both sides of a link to determine if a bit time that has the CTL bit asserted is command, address or a CRC value. However, the logic analyzer trace memory will not contain all of the communication on the link. It will only store what it has been configured to store in the analyzer trace menu. Thus, the link synchronization message will most probably not be captured by the logic analyzer. Because of this, the Protocol Decode software will need to be manually aligned to the link. Please refer to the [FS2240 Users Manual](#) for complete instructions on how to align the Protocol Decode to the captured data.

In order to decode the HyperTransport captured traffic the Protocol Decode software uses the requirement that a CRC occurs every 512 bit times. By finding one CRC, the Protocol Decode software can then align all other states in the trace and provide a proper decode.

Using the CRC value specified by the user the Inverse Assembler will attempt to locate the CRC state in the trace file. The Inverse Assembler examines the first 512 states that precede the current state. If a CRC state value is not located, the Protocol Decode software will examine the 512 states that follow the current state. If the CRC state is located, the search is terminated and the data is decoded properly.

The Inverse Assembler will also tag the current state with prevalent information (e.g. is the current state a CRC, if not, what position does it occupy in the bit times algorithm) so that the number of searches is limited on subsequent states being processed.

The Inverse Assembler will utilize the tagged information in the previously processed state to disassemble concurrent states, thus allowing the user to scroll forward and backwards in the trace file without the Inverse Assembler failing to locate the CRC state status for each state processed.

Locating a CRC value in the Trace file

The current version of the Protocol Decode Software will cause the first trace file to be displayed with no CRC synchronization. This allows the operator to peruse the file quickly, and then specify the “default” CRC value.

After capturing the desired information, the user must undertake the following steps to determine which state represents the CRC and then enter the CRC value into the **CRC Alignment Value** (Figure B) screen insure proper alignment of the disassembly with the data.

After a short time users will become proficient at ‘spotting’ a valid CRC value.

The following table lists the necessary steps required to identify a CRC state:

1. Examine the 128 states (or 512 bit times) that precede or follow the state found at the center of logic analyzer display to determine which state represents the CRC.
 - a. Typically after an acquisition the center of the display will contain the trigger event.
2. Find the label for CTL. Disregard any of the 128 states where the CTL bit is set to zero (0).
3. Disregard any of the 128 states that are NULL states (0X00000000)
4. Disregard any of the 128 state that are NoOps or Flow Control packet a value with only 1 or 2 bits set to a one (for example 0100000000 or 0000001000). If viewing the value as HEX a NoOp will almost never contain an alpha character.
5. Any state with a large number of zeros (0) is most likely not a CRC

Figure A shown below shows a trace without the protocol decode

State Number	CTL	CAD	Command	UnitID	SeqId	PassPW	STAT	DATA	CAD 7-0	CAD 15-8	CAD 23-16
Decimal	Binary	Hex	Hex	Hex	Hex	Binary	Binary	Hex	Hex	Hex	Hex
13	1	00000400	00	04	0	0	1	00000400	00	04	00
14	1	00000000	00	00	0	0	1	00000000	00	00	00
15	1	00000000	00	00	0	0	1	00000000	00	00	00
16	1	00000100	00	01	0	0	1	00000100	00	01	00
17	1	00000000	00	00	0	0	1	00000000	00	00	00
18	1	00000000	00	00	0	0	1	00000000	00	00	00
19	1	00000000	00	00	0	0	1	00000000	00	00	00
20	1	00000000	00	00	0	0	1	00000000	00	00	00
21	1	00000000	00	00	0	0	1	00000000	00	00	00
22	1	00000000	00	00	0	0	1	00000000	00	00	00
23	1	00000000	00	00	0	0	1	00000000	00	00	00
24	1	00000000	00	00	0	0	1	00000000	00	00	00
25	1	00000000	00	00	0	0	1	00000000	00	00	00
26	1	00000000	00	00	0	0	1	00000000	00	00	00
27	1	00000000	00	00	0	0	1	00000000	00	00	00
28	1	00000000	00	00	0	0	1	00000000	00	00	00
29	1	00000000	00	00	0	0	1	00000000	00	00	00
30	1	00000000	00	00	0	0	1	00000000	00	00	00
31	1	00000000	00	00	0	0	1	00000000	00	00	00
32	1	00000000	00	00	0	0	1	00000000	00	00	00
33	1	00000000	00	00	0	0	1	00000000	00	00	00
34	1	00000000	00	00	0	0	1	00000000	00	00	00
35	1	00000000	00	00	0	0	1	00000000	00	00	00

Figure A

6. Removing the states listed in steps 2 through 5 will minimize the number of possible states containing the CRC. Experience with the link will provide insight as to which is the CRC.
 - a. The CRC value typically will be a large HEX value. The defaulted CRC value is 0xC6C7C940, which is the value of 128 states (512 bits times) containing the NULL (0x00000000) value with the CTL bit asserted.
 - b. At this point some trial and error experimentation is required. The verification is accomplished by entering the CRC value into the CRC Alignment Value (Figure B) screen and then examining the disassembled states to determine if the disassembled states are displayed correctly.

Figure B shows the CRC Alignment Value screen for inputting the CRC value.

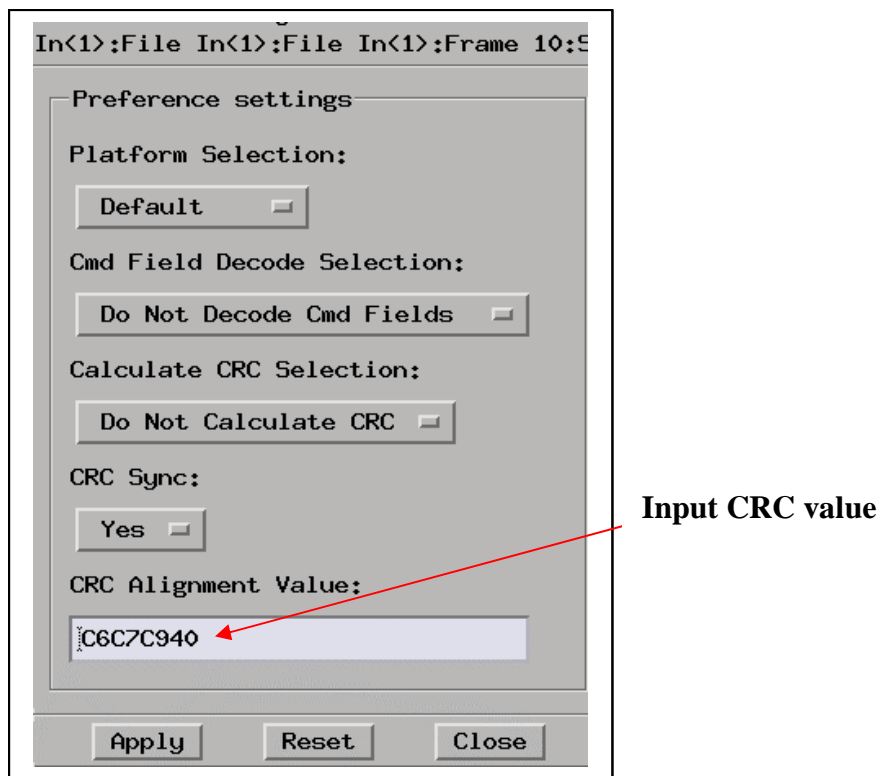


Figure B

After entering a valid CRC and scrolling through the data, the Decode Software will stay synchronized the proper protocol decode will be displayed. The user can scroll through the data file either in line or page mode.

Figure C shows a disassembled trace with the correct CRC value entered.

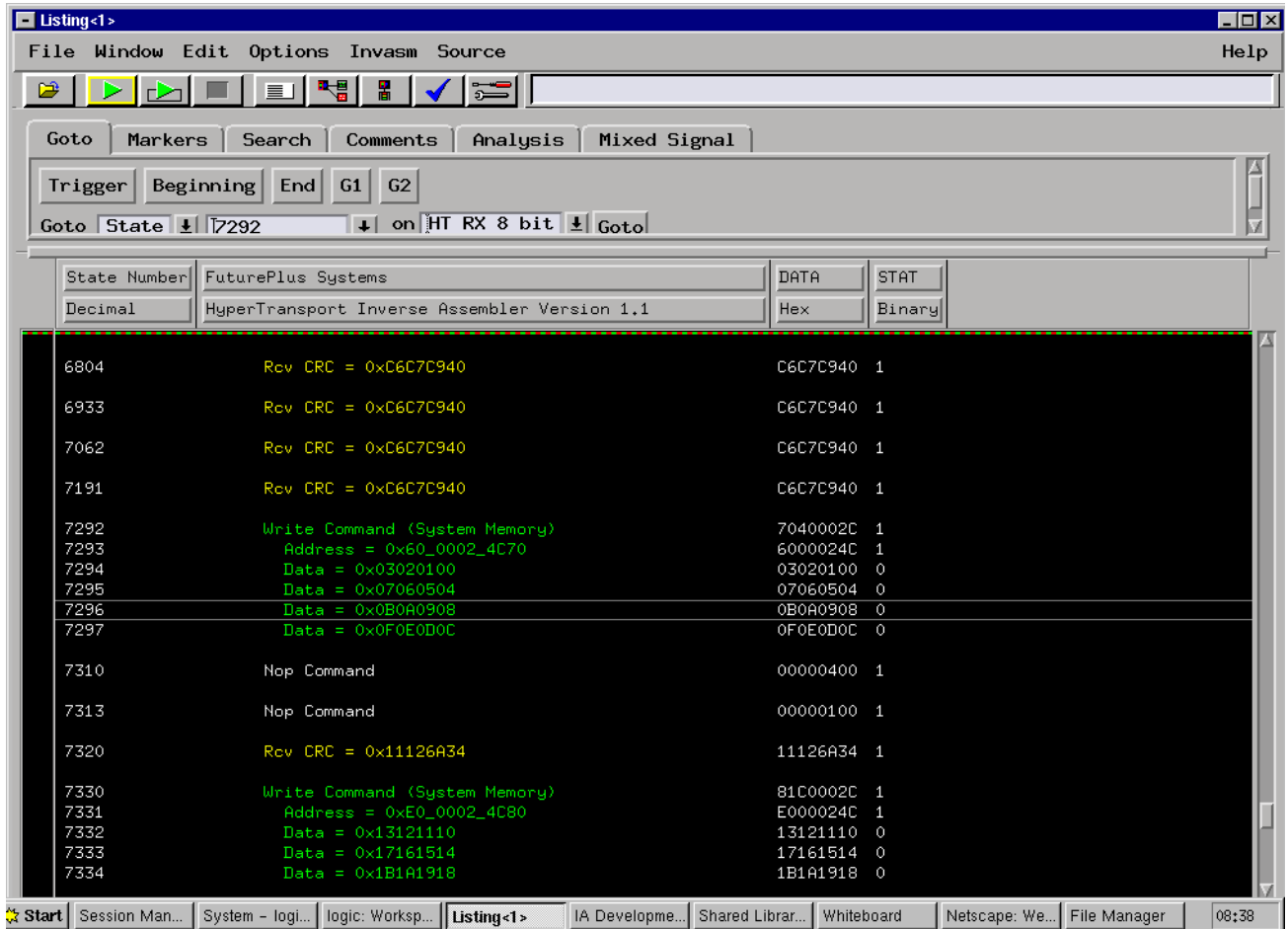


Figure C

If the Decode Software is extremely slow in disassembling the state trace file then the CRC value specified by the user cannot be located. The slow response is due to the Decode Software executing the maximum search of 1024 locations for each state being processed.

Jumping to a different location in the trace file, using markers or line numbers, where the jump is greater than 512 states will cause the CRC synchronization to be lost. The lost synchronization will cause the Decode Software to fail in locating the CRC and thus label the current state as an “**unknown**” state. When this happens steps 1 through 6 must be repeated until a valid CRC can be found and entered in the **CRC Alignment Value** screen (Figure B).

Additional Information Concerning Operation of Protocol Decode

The logic analyzer stores data based on the trigger and data qualification storage conditions set by the user. The FS2240 captures all data states from the link; the logic analyzer may or may not store all data states based on the criteria set by the user. This means that the states contained in a trace file may not be a complete set of states. In this case the trace file will be lacking many states. Some states have simply have been dropped because they were observed prior to the trigger state

The link synchronization message will most probably be contained in this first set of states dropped, thus causing the Decode Software to fail due to its inability to determine when to start counting states.

Furthermore, the Decode Software will not be able to determine when a state with the CTL bit asserted is a CRC, a command, or an address state (again, the link components can make this determination because they are in sync with each other).

To avoid this, the Decode Software assumes that it will be informed as to which data value will be the first occurrence of a CRC in the first CRC window (564 bit times or 128 states).

Using this information, the Decode Software will begin processing the states contained in the trace file. On the first state being processed, it will attempt to locate the CRC with the value specified by the user. Once that state is located, it will be able to determine if the current state falls on the 128 state boundaries and thus make the determination as to whether or not the current state is the CRC.

The Decode Software examines the first 512 states that precede the current state. If the CRC value is not located, the Decode Software will examine the 512 states that follow the current state in order to determine if the current state is a CRC. If the CRC state is located, the search is terminated and the state is processed accordingly.

The Decode Software will also tag the current state with prevalent information (e.g. is the current state a CRC, if not, what position does it occupy in the bit times algorithm) so that the number of searches is limited on subsequent states being processed.

For the very first state that is being disassembled, the Decode Software will have to locate a CRC state in order to disassemble the current state. All other adjacent states will encounter the “processed” state and glean the required information in order to ascertain whether or not the current state is a CRC. This significantly limits the search algorithm.

The Decode Software will utilize the tagged information in the previously processed state to disassemble concurrent states, thus allowing the user to scroll forward and backwards in the trace file without the Decode Software failing to locate the CRC state status for each state processed.

HyperTransport Specification 1.05

10.1.1 Transmission Errors: 8-Bit, 16-Bit, and 32-Bit Links

The following is part of section chapter 10, section 10.1.1 of the HyperTransport specification, version 1.05.

A 32-bit cyclic redundancy code (CRC) covers all HyperTransport™ links. The CRC is calculated on each 8-bit lane independently and covers the link as whole, not individual packets. CTL is included in the CRC calculation. In each bit-time, CAD is operated on first, beginning with bit 0, followed by CTL. For 16- and 32-bit links, where the upper byte lanes do not have a CTL bit associated with them, a CTL value of 0 (Data) is used. The CRC is computed over 512 bit-times. Each new CRC value is stuffed onto the CAD bits of the link 64 bit-times after the end of the 512-bit-time window and occupies the link for 4 bit-times. Therefore, bit-times 64–67 (the first bit-time being 0) of each CRC window after the first contain the CRC value for the previous window. There is no CRC transmission during the first 512-bit-time window after the link is initialized, and the value of the transmitted CRC bits is not included in the CRC calculation for the current window. Therefore, each CRC window after the first is 516 bit-times in length—512 of which are included in the calculation of the CRC that will be transmitted in the next window. There is no indication on the bus that CRC information is being transmitted. It is the responsibility of the parties on both ends of the link to count bit-times from the beginning of the first valid packet after link synchronization to determine the boundaries of the CRC windows. During transmission of the CRC, the CTL bit will be driven to a value of 1 (Control).

For example, the contents of 8-, 16- and 32-bit links during the first three CRC windows after link synchronization are shown in Table 1.

Table 1. CRC Window Contents After Link Synchronization

CRC Window After Sync	Number of Bit-Times	Link Contains
1 st	512	Payload for first window
2 nd	64	Payload for second window
	4	CRC of first window
	448	Payload for second window
3 rd	64	Payload for third window
	4	CRC for second window
	448	Payload for third window

For additional information on the operation and use of the FuturePlus Systems FS2240 HyperTransport analysis probe please contact tech_sup@futureplus.com.

For information on purchasing the FS2240 HyperTransport analysis probe or other bus analysis tools from FuturePlus systems please contact sales@futureplus.com or call 719 278-3540.