

**HyperTransport Design Application Note**

The FuturePlus® Systems FS2240, FS2241, and FS2243/44 HyperTransport Analysis Probes provide a mechanical and electrical connection between an Agilent logic analyzer and a HyperTransport link. Software is also provided that configures the logic analyzer and translates the incoming data into HyperTransport transaction mnemonics. The analysis probes when coupled with the powerful triggering and state analysis capabilities of Agilent's state analyzer modules, gives the user a powerful tool for debugging, testing, and verifying the compliance of HyperTransport Technology link-based systems.

This application note describes the operation of the analysis probes and the requirements for designing in the test connections to insure proper operation of the FS2240, FS2241, and FS2243. Following recommendations of this application note will insure maximum signal integrity and provide the highest bandwidth for the target link. It also provides simulation data describing the impact of the probe on the HyperTransport link,

The differences between the FS2240, FS2241, and FS2243/44 are related to the different methods of connecting to the systems under test.

Proper usage of this application note assumes a thorough knowledge of electrical engineering and PCB design.

Rev: 12/06



FS2240 - 2.4 GT/s  
80 Pin 3M Connector

FS2241 - 400 MT/s  
20 Pin Samtec Connector

FS2243/44 - 2.4 GT/s  
Soft Touch Connector



FS2240, FS2241, FS2243, FS2244  
HyperTransport Analysis Probe

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# HyperTransport Link Probing

## 1.0 Introduction

The HyperTransport link is 2 to 32 bits wide, with a 400 to 2800 Million Transfers per second (MT/s) transfer rate that is clocked synchronously on both rising and falling edges of the clock. Designed as a point-to-point packet-based link, HyperTransport utilizes two unidirectional signal sets between single chips on a board or between boards. *Figure 1* illustrates this link.

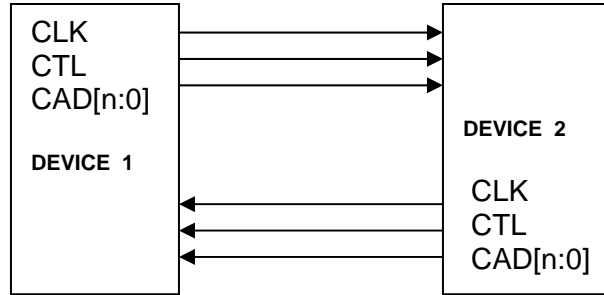


Figure 1. HyperTransport Link

*Figure 2* shows the nominal voltage levels and timing of the differential HyperTransport signals.  $T_{CADV}$  is the CAD/CTL valid time relative to the CLK signal. Section 19.5 of the HyperTransport Link Specification lists the maximum and minimum values of  $T_{CADV}$  for different link speeds.

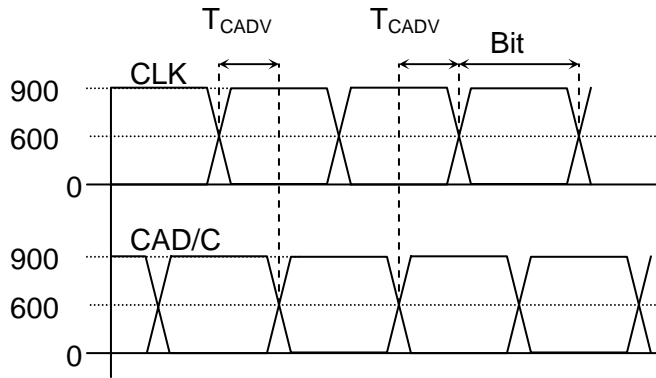


Figure 2. HyperTransport Link Signal Levels and Timing

This paper will describe 4 probing methods designed to capture these signals and decode them for the purpose of hardware and software development.

## 2.0 Probing concepts

### **Probing methodology**

Oscilloscopes and logic analyzers are the primary instruments used to probe any link. HyperTransport is no exception. Oscilloscopes are of value when looking at individual HyperTransport signals for signal integrity or pairs of signals for timing (setup and hold or skew). They are of little use when looking at groups of signals, especially on the packet level. This paper will deal with the use of a logic analyzer for HyperTransport link analysis. Digital probing with a logic analyzer involves adapting the analyzer to the HyperTransport environment in the areas of mechanical interface, electrical compatibility, timing and packet decoding.

### **Mechanical interface**

The mechanical interface consists of one or more connectors located on the target system board that mates with a connector on the end of a coax ribbon cable. The board connector is chosen to minimize board space. It is surface mounted to leave inner layers free for routing.

### **Electrical compatibility**

Electrical compatibility implies that the probe should be “invisible to the link”. Loading of the link should be minimized. No signals should be introduced onto the link by the probe. The probe also has to be compatible with the logic levels of HyperTransport so that it may provide the logic analyzer with signal levels that can be captured with the minimum number of channels. The HyperTransport probe discussed herein utilizes both buffers and passive isolation techniques. This insures minimal link loading while providing logic level translation to the logic analyzer.

### **Timing**

The HyperTransport probe needs to perform deserialization in order to capture packets and present them to the logic analyzer. To accomplish this, timing is critical and must not be distorted. Clock to data skew must be minimized.  $T_{CADV}$ , the timing of CAD/CTL<sub>OUT</sub> to CLK<sub>OUT</sub>, specified by the HyperTransport specification Section 19.5 for operation at 1600MT/s (800 MHz clock) is 166 ps min to 459 ps max. This specification must be adhered to for all the CAD/CTL lines that tap onto the HyperTransport link. Tight control of line to line skew for CAD/CTL signals is implied here. Probe design assumes that this timing will be adhered to including any additional skew introduced by circuit traces from the link taps to the connector. Probes are calibrated to minimize this skew across all the signals due to cable variations but the target board skew cannot be anticipated. That is why link tap circuit trace lengths are specified. Reference must be made to the HyperTransport specification section M.2 PCB Skew.

### **Packet decoding**

Packet decoding consists of deserialization of the CAD stream in the probe and the inverse assembly (decoding) of the captured CAD words to display the commands, data and CRC's on the logic analyzer. The protocol decode software has an intimate knowledge of the HyperTransport protocol built into it.

### 3.0 Benefits and challenges of digitally probing HyperTransport

This section describes the benefits and the challenges faced when probing the HyperTransport link with a logic analyzer.

#### Benefits

The first and most obvious benefit is a mechanical connection to the link. Designing in a connector to the system under test provides a reliable and easy method of connecting to all of the signals on the link. This enables the logic analyzer to simultaneously view activity on all signal lines.

A more important benefit is to minimize electrical intrusion of the HyperTransport link. The FuturePlus analysis probes and the connection layout described in this document provide a way of probing an electrically transparent connection.

Moving of all data and command lines into the analysis probe enables the information to be converted from serial information into 32 bit packets and sent to the logic analyzer. Once in the logic analyzer the FuturePlus protocol decode software translates and displays the information as HyperTransport transactions. This facilitates hardware and code debug.

#### Challenges

There are several challenges inherent in probing HyperTransport. The link transfers data at data rates up to 2.8 GT/s using differential signals with unique logic levels. This calls for special probe input buffers and conversion of differential signals to single-ended. The analysis probe also minimizes the number of logic analyzer channels used. In addition, the deserialization of data requires synchronization of the master clock to the logic analyzer with the start of the data. This is handled internally to the probe hardware with a synchronization circuit that keys off the start of data.

Another challenge involves maintaining the signal integrity of the link both with and without the probe attached to the target board connector. Furthermore the data to clock skew in both the probe and the link attachment must be minimized.

The CRC codes in HyperTransport present a unique challenge. Packet decoding is accomplished in the logic analyzer employing a protocol decode software that keys off of CRC's. The CRC codes appear every 512 bit times and can occur in the middle of packets. The protocol decode software must be able to identify these codes as well as calculate them for the preceding data. These codes occur with the CTL bit asserted and can therefore masquerade as commands. The protocol decode software must allow the selection of a bit time when the CRC occurs. The protocol decode software can then identify all the commands that occur on 512 bit time boundaries as CRC's, with the selected CRC bit time used as the index point. Simply stated, if you find a CRC then 512 bit times later another will occur.

## 4.0 Signal integrity issues and solutions

The signal integrity issues involve HyperTransport link loading and CAD/CTL to CLK signal skew from the link into the probe input registers. This paper addresses the signal chain in light of these issues and presents solutions.

The circuit from the link to the probe connector shall be discussed first. Link loading must be minimized to the point where the probe is electrically invisible to the link. There must also be minimal impact with the probe cable disconnected. This means that the impedances of the tap points should be high and no stub effects should be apparent at the frequencies involved. The implementation that provides the best solution to the above issues has the following criteria:

1. Delays of signals from the driving device to the connector are equalized
2. The maximum etch length from target signal to the connector is controlled
3. The stub length of the etch from target signal to the tip resistors (for FS2240) is minimized
4. Tip resistors when required are chosen by simulation to provide a best match between the probe and the HyperTransport link on the target board

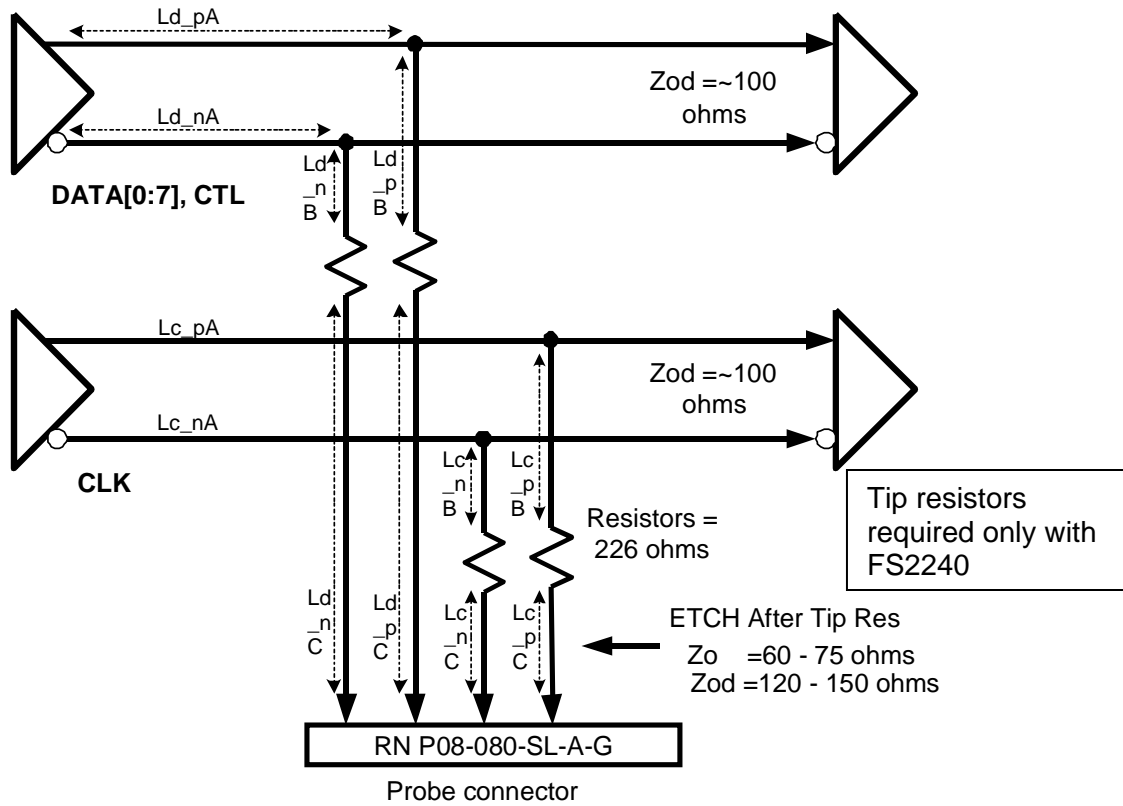
*Figure 3* shows the parameters (with the constraints listed) that provide an optimal solution at the maximum clock frequency. When designing in the 3M connector for the FS2240, in some situations, the lengths from the tip resistors to the connector can be longer, but a simulation run is advised to assess the impact.

More information on the simulations will be presented later on in this section.

The next piece of the signal integrity issue involves the path from the connector to probe input buffers via the coax ribbon cable. As previously mentioned, connectors must minimize impedance discontinuities and be capable of passing the maximum frequencies expected for HyperTransport. This controls reflections and stub effects. The cable frequency response must support HyperTransport. The skew in the coax ribbon cables is due to mechanical path differences and is difficult to precisely control.

Input signal levels to the probe are attenuated and buffering is required. The buffers exhibit different propagation delay times and hence cause skew. Skew on the probe circuit board is caused by mechanical path differences, uneven capacitive loading of individual signals (slowing the rise time and creating skew) and semiconductor device delay variations. Calibration of the HyperTransport probe adjusts the CLK to CAD/CTL skew so that the setup and hold times for the input registers are met for all HyperTransport bit times.

## HT Probe Etch Length Rules



### Data to Clock Length Matching

$$[Ld_{pA} + Ld_{pB} + Ld_{pC}] - [Lc_{pA} + Lc_{pB} + Lc_{pC}] = 0 \pm 0.020''$$

### Diff Pair Length Matching

$$[Ld_{pA} + Ld_{pB} + Ld_{pC}] - [Ld_{nA} + Ld_{nB} + Ld_{nC}] = 0 \pm 0.020''$$

$$[Lc_{pA} + Lc_{pB} + Lc_{pC}] - [Lc_{nA} + Lc_{nB} + Lc_{nC}] = 0 \pm 0.020''$$

### Maximum Etch Length Rules

$$\text{Driver to Probe Connector} : [Ld_{pA} + Ld_{pB} + Ld_{pC}] < 4.0''$$

$$\text{and } [Lc_{pA} + Lc_{pB} + Lc_{pC}] < 4.0''$$

$$\text{Etch to Tip R Stub } [Ld_{pB} \text{ or } Ld_{nB} \text{ or } Lc_{pB} \text{ or } Lc_{nB}] < 0.050''$$

Figure 3 Etch Length Rules for HyperTransport Probe Connector Attachment

Note: For HT Link speeds at  $\leq 800$ MT/s, these tolerances double and the maximum etch to tip R stub can be  $\leq 0.100''$

## 5.0 HyperTransport Probing Simulation

The information presented below constitutes the SPICE models and simulation used to predict HyperTransport link probing. *Figure 4* shows the simulation results at a HyperTransport receiver with tip resistors depopulated. *Figure 5* shows the results with tip resistors installed but probe cable detached. *Figure 6* displays the result with the probe attached and operating.

### Simulation models

By utilizing the SPICE models and simulation, the board designer can observe the behavior of the layout before fabrication. This allows the designer to try variations in trace impedances, lengths, etc. that are sometimes necessary when routing a board. As the results for a typical board show, digital probing has little impact on the HyperTransport link.

This section lists the SPICE models for the various sub-circuits that were used to model the HyperTransport probing and derive the results shown at the end of this section.

HyperTransport driver:

HyperTransport receiver:

HyperTransport link etch:

Link tap etch:

Tip resistors:

Tip resistor-to-connector etch:

Connector:

Coax ribbon cable:

Probe board:

Probe buffers:

The SPICE simulation will ultimately contain vendor models that are likely to be proprietary as well as circuit board models that are layout specific. For these reasons the simulation listing for the results in *Figures. 4, 5, and 6* is not presented here. FuturePlus will supply their models and assistance on request.

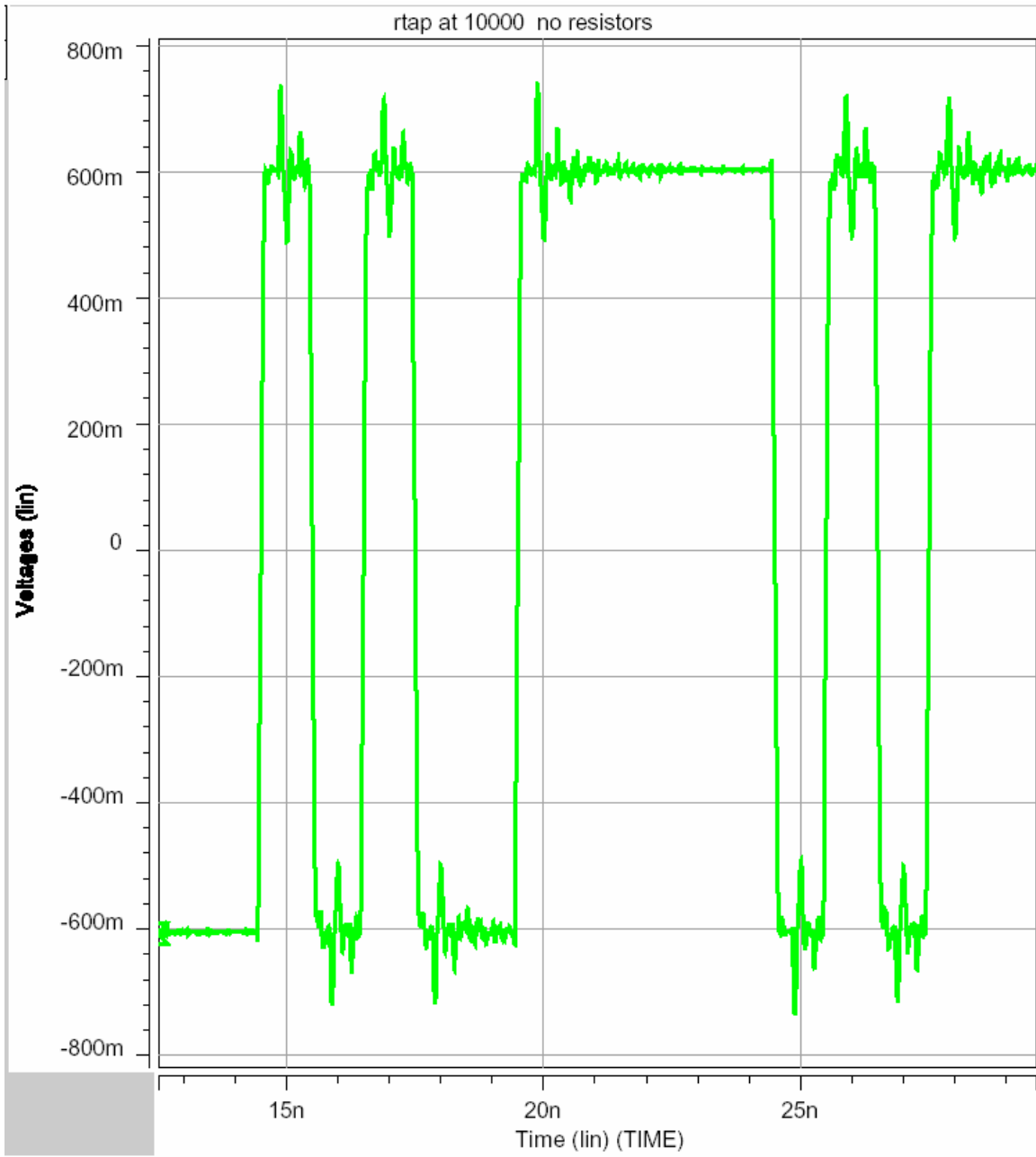


Figure 4 HT link Without Tip Resistors (Differential Signal at HT Receiver)

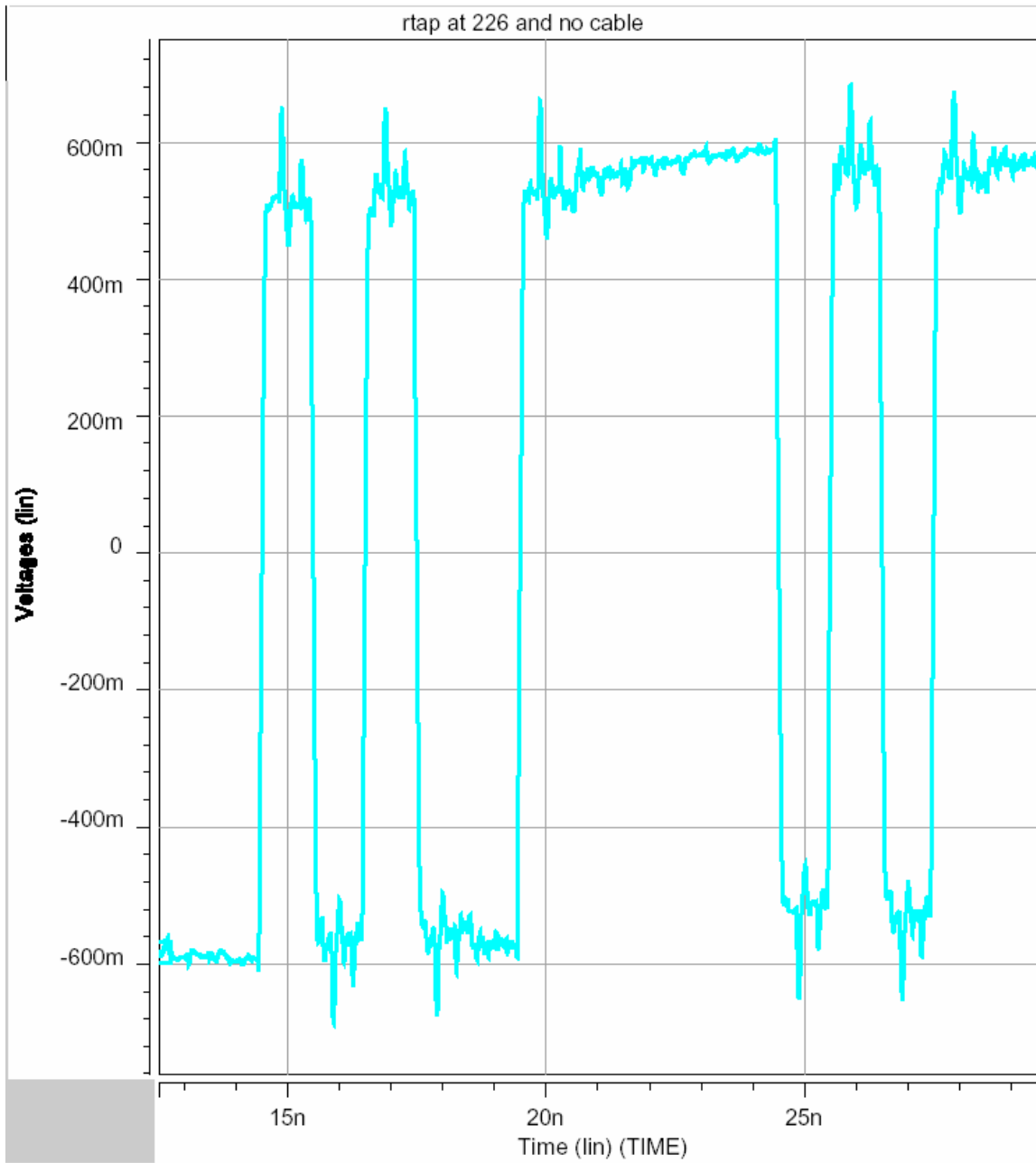


Figure 5 Resistors In and Cable Detached (Differential Signal at HT Receiver)

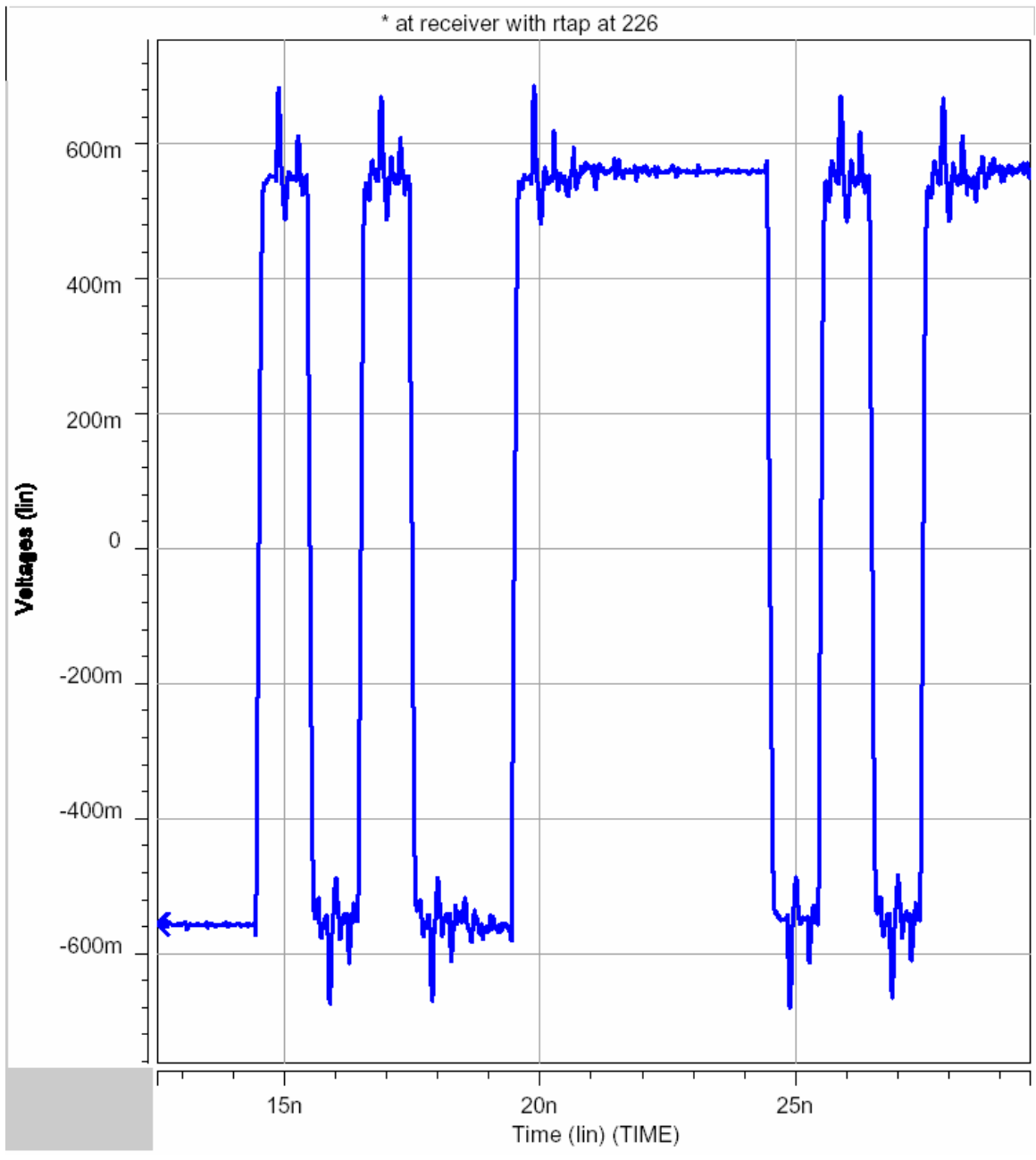


Figure 6 HT Probe attached (Differential Signal at HT Receiver)



Figure 8 shown below shows the dimensions of the cable connector end. This defines a keep out area on the target board for components.

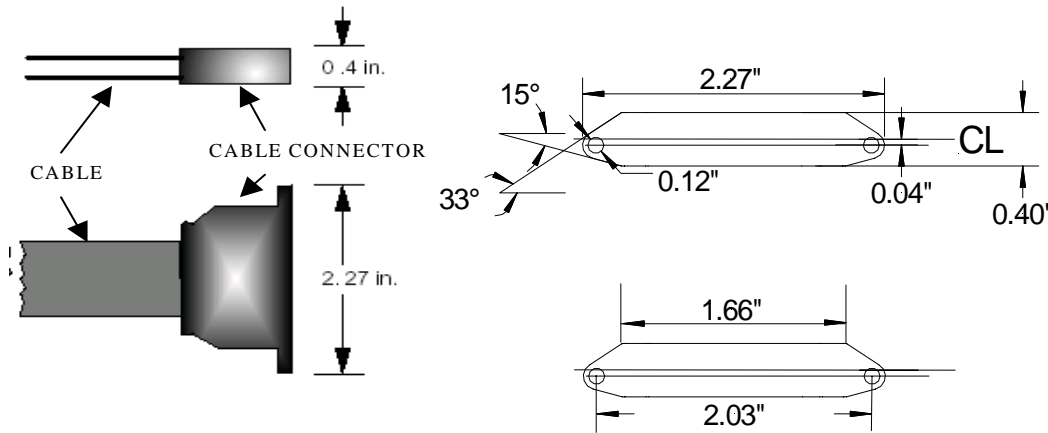


Figure 8 Cable Connector Dimensions that Determine Keep Out Area

### Pin out information

#### 8 Bit Connector Layout

Table 1 below shows the 8 bit HyperTransport 3M 80 pin Connector Pin Signal List for TX and RX links. Note that the CTL and CLK signals cannot be moved. The CAD signal pairs can be swapped with other CAD signal pairs; however, do not change the relative \_H/\_L pin assignment.

#### 16 Bit Connector Layout

Table 2 below lists the 16 bit HyperTransport Robinson Nugent Connector Pin Signal List. Note that the CTL and CLK signals cannot be moved. The CAD[0-7] signal pairs can be swapped with other CAD[0-7] signal pairs and CAD[8-15] signal pairs can be swapped with other CAD[8-15] signal pairs, however, do not change the relative \_H/\_L pin assignment. The BIAS pin should be connected to a 1K ohm resistor to ground (pull down). Upper clock is the clock for bits 15-8. Lower clock is the clock for bits 7-0

Signal Name	Pin #	Pin #	Signal Name
RESET# (optional)	1	2	PWROK (optional)
LDTSTOP# (optional)	3	4	LDTREQ# (optional)
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
RX_CAD_L[0]	11	12	TX_CAD_L[0]
RX_CAD_H[0]	13	14	TX_CAD_H[0]
GND	15	16	GND
RX_CAD_L[1]	17	18	TX_CAD_L[1]
RX_CAD_H[1]	19	20	TX_CAD_H[1]
GND	21	22	GND
RX_CAD_H[2]	23	24	TX_CAD_H[2]
RX_CAD_L[2]	25	26	TX_CAD_L[2]
GND	27	28	GND
RX_CAD_H[3]	29	30	TX_CAD_H[3]
RX_CAD_L[3]	31	32	TX_CAD_L[3]
GND	33	34	GND
RX_CTL_L	35	36	TX_CTL_L
RX_CTL_H	37	38	TX_CTL_H
GND	39	40	GND
RX_CLK_H	41	42	TX_CLK_H
RX_CLK_L	43	44	TX_CLK_L
GND	45	46	GND
RX_CAD_H[4]	47	48	TX_CAD_H[4]
RX_CAD_L[4]	49	50	TX_CAD_L[4]
GND	51	52	GND
RX_CAD_H[5]	53	54	TX_CAD_H[5]
RX_CAD_L[5]	55	56	TX_CAD_L[5]
GND	57	58	GND
RX_CAD_L[6]	59	60	TX_CAD_L[6]
RX_CAD_H[6]	61	62	TX_CAD_H[6]
GND	63	64	GND
RX_CAD_L[7]	65	66	TX_CAD_L[7]
RX_CAD_H[7]	67	68	TX_CAD_H[7]
GND	69	70	GND
GND	71	72	GND
GND	73	74	GND
GND	75	76	GND
GND	77	78	GND
GND	79	80	GND

Do not ground pins 1 - 4

Table 1 - 8 bit HyperTransport Robinson Nugent Connector (FS2240) Pin Signal List

Signal Name	Pin #	Pin #	Signal Name
RESET# (optional)	1	2	PWROK (optional)
LDTSTOP# (optional)	3	4	LDTREQ# (optional)
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
CAD_L[8]	11	12	CAD_L[0]
CAD_H[8]	13	14	CAD_H[0]
GND	15	16	GND
CAD_L[9]	17	18	CAD_L[1]
CAD_H[9]	19	20	CAD_H[1]
GND	21	22	GND
CAD_H[10]	23	24	CAD_H[2]
CAD_L[10]	25	26	CAD_L[2]
GND	27	28	GND
CAD_H[11]	29	30	CAD_H[3]
CAD_L[11]	31	32	CAD_L[3]
GND	33	34	GND
GND	35	36	CTL_L
BIAS	37	38	CTL_H
GND	39	40	GND
UPPER_CLK_H	41	42	LOWER_CLK_H
UPPER_CLK_L	43	44	LOWER_CLK_L
GND	45	46	GND
CAD_H[12]	47	48	CAD_H[4]
CAD_L[12]	49	50	CAD_L[4]
GND	51	52	GND
CAD_H[13]	53	54	CAD_H[5]
CAD_L[13]	55	56	CAD_L[5]
GND	57	58	GND
CAD_L[14]	59	60	CAD_L[6]
CAD_H[14]	61	62	CAD_H[6]
GND	63	64	GND
CAD_L[15]	65	66	CAD_L[7]
CAD_H[15]	67	68	CAD_H[7]
GND	69	70	GND
GND	71	72	GND
GND	73	74	GND
GND	75	76	GND
GND	77	78	GND
GND	79	80	GND

Do not ground pins 1 - 4

Table 2 - 16 bit HyperTransport Robinson Nugent Connector (FS2240) Pin Signal List

## Method of Probing – FS2241

The FS2241 uses Samtec connectors for probing a HyperTransport link, which is more useful for probing 4 layer target boards. This is because the alternate probe design uses 2 smaller connectors and places the tip resistors in the probe cable instead of on the target.

The drawback of this approach is that the application of the Etch Length Rules detailed earlier in this document is harder to achieve because of the added length through the connector to the tip resistors on the cable, and the unequal trace lengths established by placing the connector pins directly on top of the HyperTransport link etches. This limits the FS2241 to a maximum data transfer rate of 400 MT/s. Because of the smaller connector size of this alternate approach, each connector provides only 8 data bits, 1 CTL, and 1 CLK signal.

This design uses **2 Samtec QSH-20-DP connectors** which connect to 8 bits each and are recommended to be placed as close to the receive side of the link as possible. The spacing of the Samtec DP leads matches up well to the signal spacing recommended in the HyperTransport Design Guidelines.

The design is available in two different configurations. The F configuration is designed to be used on HyperTransport links where the first 4 CAD bits and last 4 CAD bits are routed on top of each other on different layers of the target board. This configuration is recommended to be probed from the bottom of the board. The pinout for the F configuration is as follows on *Table 3*:

Pin	Signal		Signal	Pin
		Gnd		
1	CAD_H(0)		LDTREQ_L	2*
3	CAD_L(0)		LDTSTOP_L	4*
5	nc		CAD_H(4)	6
7	nc		CAD_L(4)	8
9	CAD_H(1)		nc	10
11	CAD_L(1)		nc	12
13	nc		CAD_H(5)	14
15	nc		CAD_L(5)	16
17	CAD_H(2)		nc	18
19	CAD_L(2)		nc	20
21	nc		CAD_H(6)	22
23	nc		CAD_L(6)	24
25	CAD_H(3)		nc	26
27	CAD_L(3)		nc	28
29	nc		CAD_H(7)	30
31	nc		CAD_L(7)	32
33	CLK_H		nc	34
35	CLK_L		nc	36
37	Gnd		CTL_H	38
39	nc		CTL_L	40
		Gnd		

\* PWR\_OK and LDTRST\_L are probed on pin 2 and 4 of the second connector

Table 3 8 bit HyperTransport Samtec probe F configuration Pin Signal List

The H configuration of the probe connector is more suitable for HyperTransport links where all 8 bits are routed on the same layer of the pcb. In this situation the connectors should be on the side of the pcb with the signals. Please refer to *Table 4*.

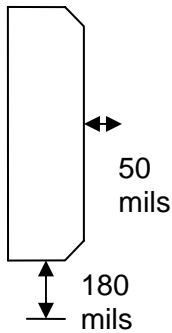
Pin	Signal		Signal	Pin
		Gnd		
1*	PWR_OK		CTL_L	2
3*	LDTRST_L		CTL_H	4
5	CAD_L(7)		nc	6
7	CAD_H(7)		nc	8
9	nc		CAD_L(6)	10
11	nc		CAD_H(6)	12
13	CAD_L(5)		nc	14
15	CAD_H(5)		nc	16
17	nc		CAD_L(4)	18
19	nc		CAD_H(4)	20
21	CLK_L		nc	22
23	CLK_H		nc	24
25	nc		CAD_L(3)	26
27	nc		CAD_H(3)	28
29	CAD_L(2)		nc	30
31	CAD_H(2)		nc	32
33	nc		CAD_L(1)	34
35	nc		CAD_H(1)	36
37	CAD_L(0)		Gnd	38
39	CAD_H(0)			40
		Gnd		

\* LDTREQ\_L and LDTSTOP\_L are probed on pin 1 and 3 of the second connector

Table 4 8 bit HyperTransport Samtec H configuration Pin Signal List

The Samtec QSH-20-DP connector has a center ground conductor, which should be only connected at the ends (pins 1, 2, 39, and 40) of the connector. The pads for this ground conductor should be made as large as possible without interfering with the path of the signals on the HyperTransport link.

Keepout Requirements – There should be no components within 180 mils of ends of the connector and within 50 mils of the long sides.



Samtec Connector layout – The recommended connector to use is a Samtec QSH-20-DP. The .020” pitch of the connector allows pads to be placed on the standard HT link layout without changing the 5 mil spacing of a differential pair. This minimizes the impact to a target board design when implementing a probe connection.

Connector and footprint information can be found at <http://www.samtec.com>. The pad layout for the QSH-20-DP is shown below in *Figure 9*. It is recommended to leave out the pads for no connects as they can interfere with routing the HT signals. The connector should be oriented so that the side with the chamfered corners will be pointing away from the receiver. Vias to bring signals from the opposite side of the board should be made as small as possible.

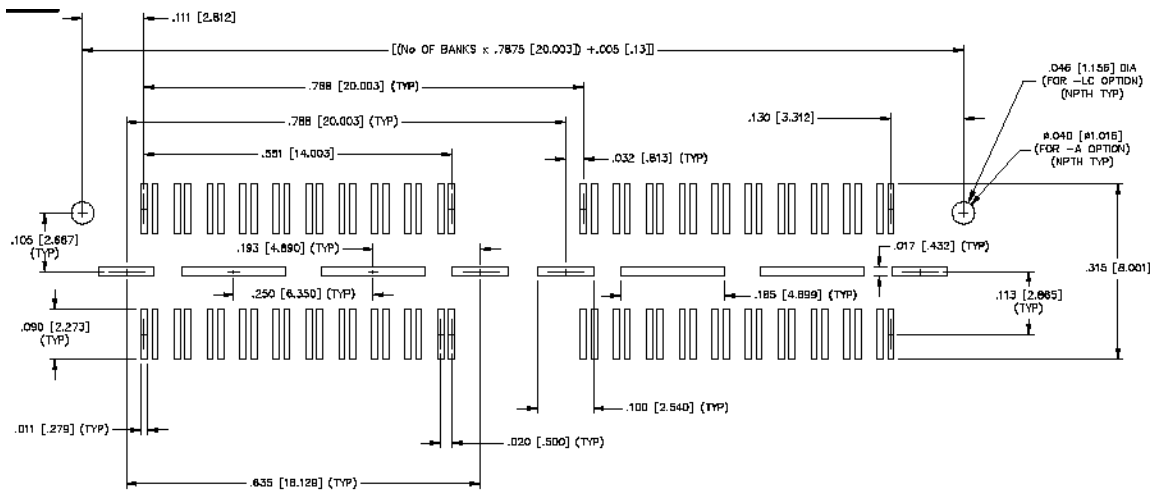


Figure 9 Samtec QSH – DP connector footprint

Two aspects of the alternate probe design impact its use above 400MT/s. The first is the fact that because the tip resistors are placed across the QSH/QTH mated pair they are approximately .400 inches from the HyperTransport Link (length B in the Figure 3).

The second impact is that the connector is placed directly on the HyperTransport Link therefore there can be small differences in the lengths of the differential pairs on one side of the connector when compared to the other. Figure 10 shows a Probe F configuration on a target board. Note that the differential pairs for CAD4 are probing the Link at a different location than CAD1 is probed. This offset can be as much as .140" if it is not accounted for in the layout of the connector pads.

Routing etches to the connector pads to minimize length differences and simulation of the connection at target speeds above 400MT/s is recommended. Figure 10 provides an example of the trace routing.

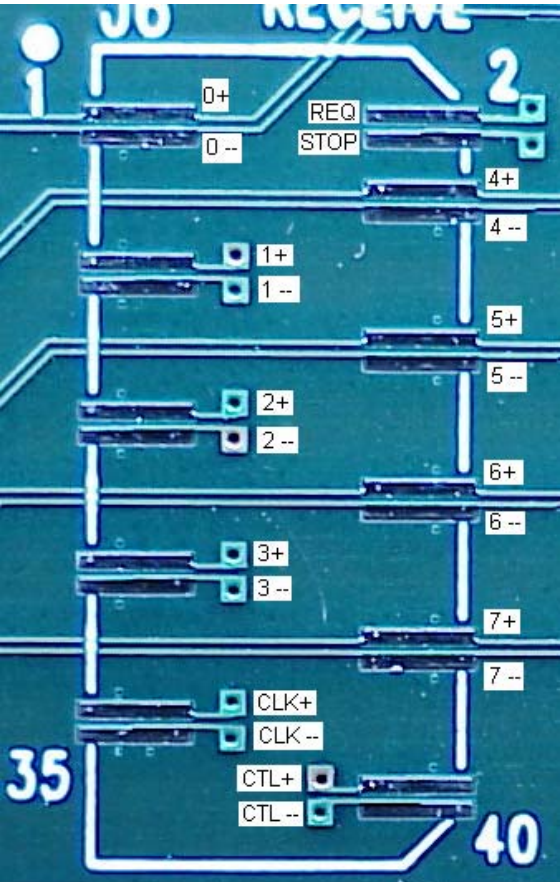


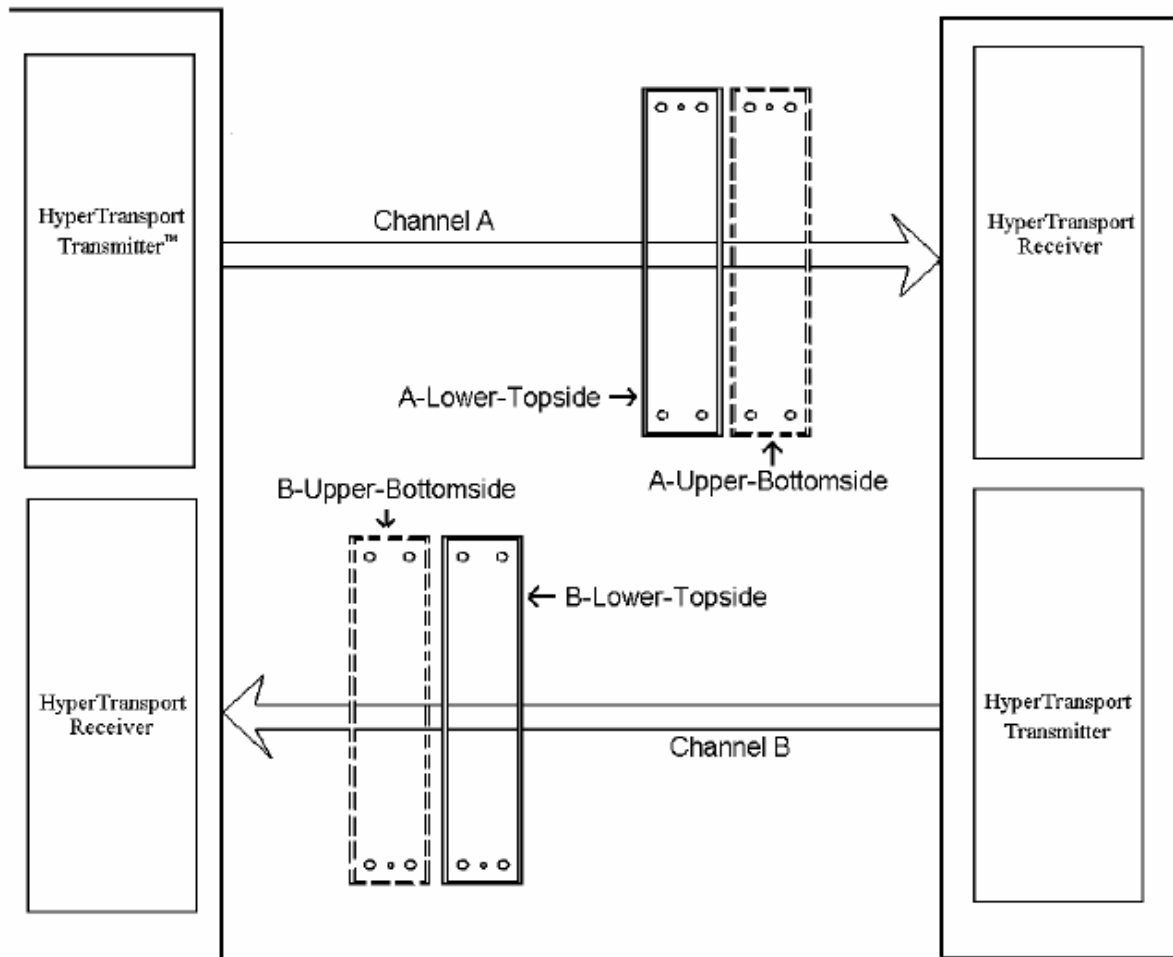
Figure 10 – Samtec connector layout on target

## Soft Touch Connectorless Method of Probing – FS2243

The FS2243 uses a “connectorless” approach for probing HyperTransport links. This method is easier to implement on targets with low layer counts and/or tight space requirements, because it does not require tip resistors on the target and only brings 10 bits to each of the 2 probing locations required per link. Additionally, it can be implemented using standard PCB pad features and can therefore be designed into a target board at no cost increase and used when needed with little additional commitment of time and money.

In order to probe 8 bit (TX **and** RX) or a 16 bit HT link (TX **or** RX), 2 separate connectorless probing locations are needed. The overall placement strategy is to place one of each of the probing locations on each side of the board as close as possible to the Receive end of the link. It is recommended that A Lower and B Lower be placed on the top side and A and B Uppers be placed on the bottom side of the target board.

This layout was designed to minimize the impact of probing a HT link utilizing a microstrip layout where the upper and lower bytes are routed on different layers.



NOTE – dashed lines for “Upper-Bottomside” connectors for use when probing TX and RX on 16 bit links

## Soft Touch probing footprint

The footprint designed for use with the FS2243 is shown below in *Figure 11*: Please note that not all probe pads are required, reference the A and B pinouts described in this document.

Layout guidelines:

Vias in pads are not recommended. A via that is tangential to the pad is allowed. There must be a solder mask between all pads. Recommended pad finish is HASL, immersion silver, or gold over nickel.

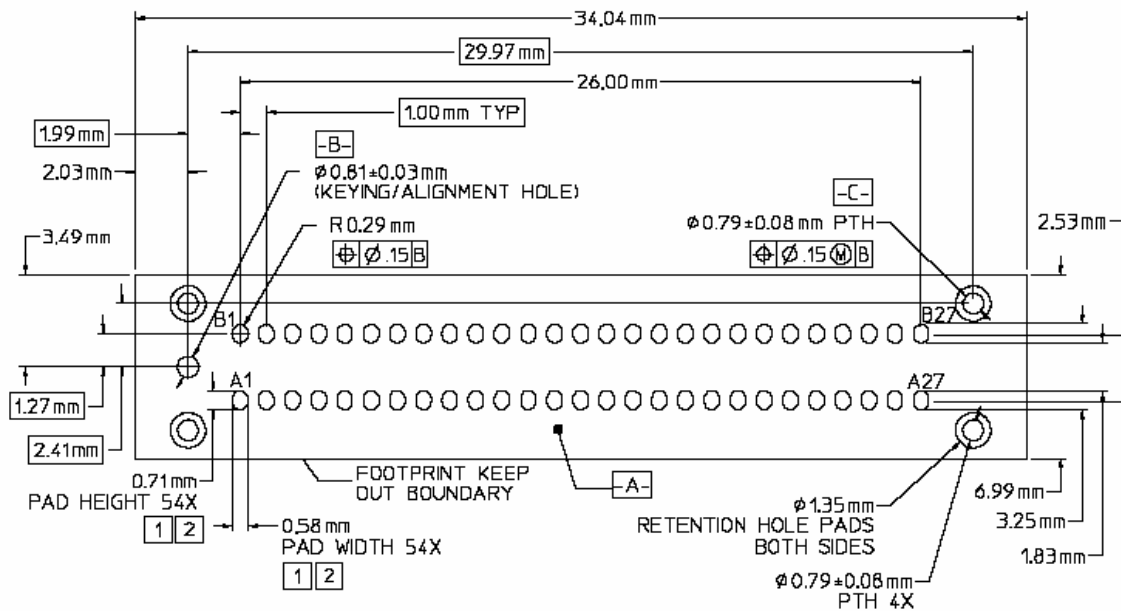


Figure 11 – Mechanical layout for FS2243 connectorless probing

### Retention module

A retention module (*Figure 12*) is required to provide the mechanical support of the connectorless probe to the target board. The module is simply attached to the board by soldering its legs to the plated through holes that are part of the footprint described above. The FS2243 is then connected to the target by placing the probe head into the retention clip, taking care to maintain polarity, and screw down the captive fasteners. Five pcs of the retention module are provided with your probe. Additional retention modules can be ordered from FuturePlus Systems. The PI part number is 600-0117-01. The Agilent part number is E5387-68701.

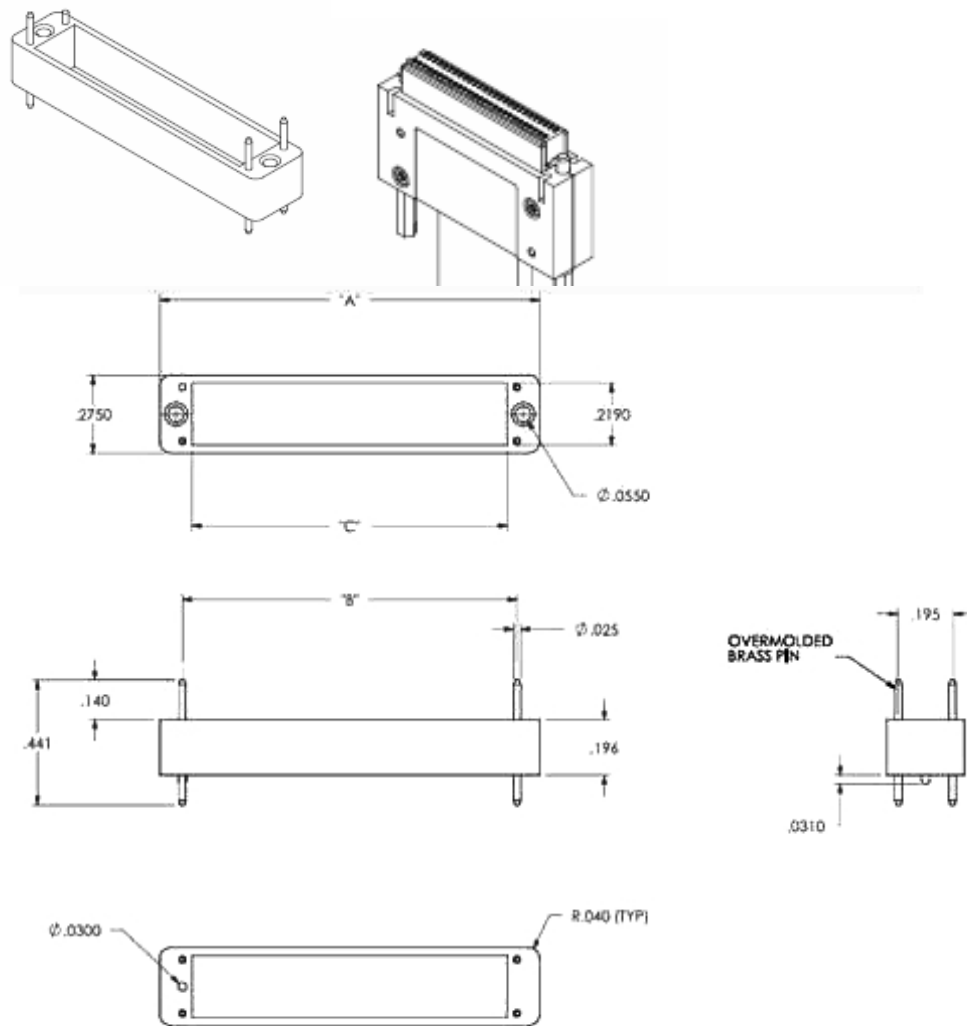
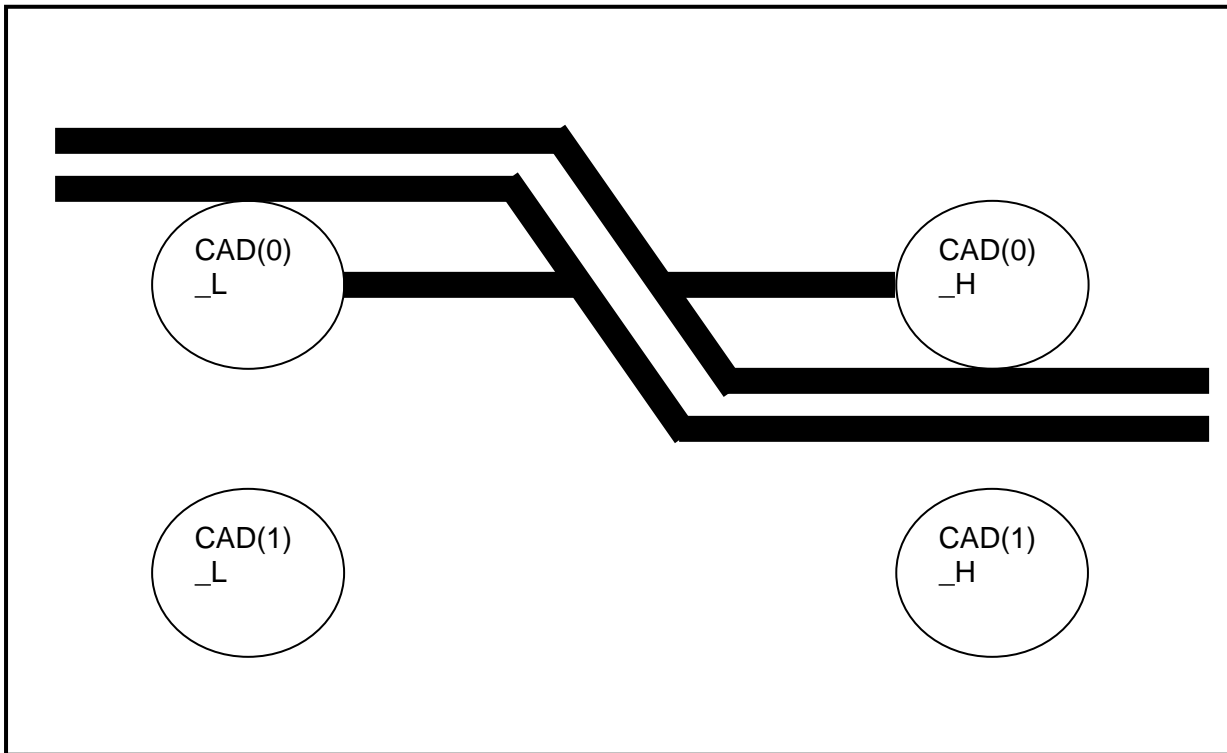


TABLE 1			
POSITION	"A"	"B"	"C"
-27	1.340	1.1800	1.110
-48	2.206	2.0460	1.976

Figure 12 – Retention Module

Connector - less probe trace routing – Differential signals in same row, different columns

The goal is to minimize the disruption to the standard HT differential pair routing between devices and to minimize any differences in position on the link where each signal is probed, as well as introduce only a minimal and equal length stub to each pad. It is also important to maintain the spacing between signals in a pair. The following is an example of a layout for 1 pair where the signals are in the same row but different columns, which is how the FS2243 probe is arranged:



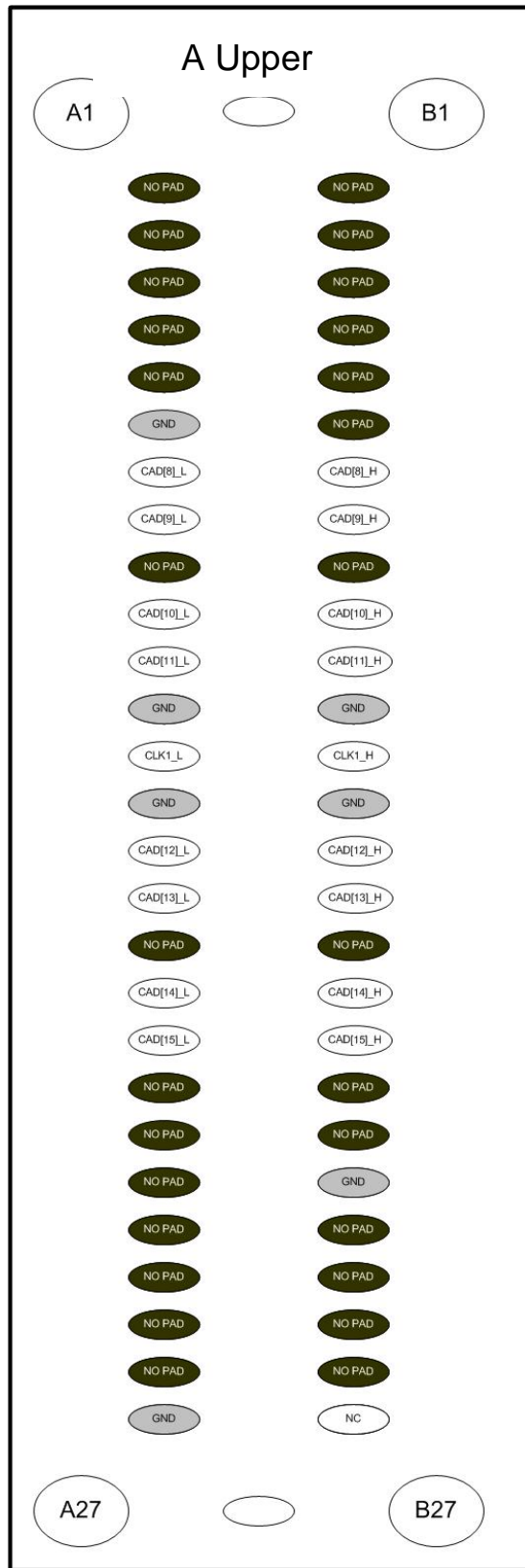
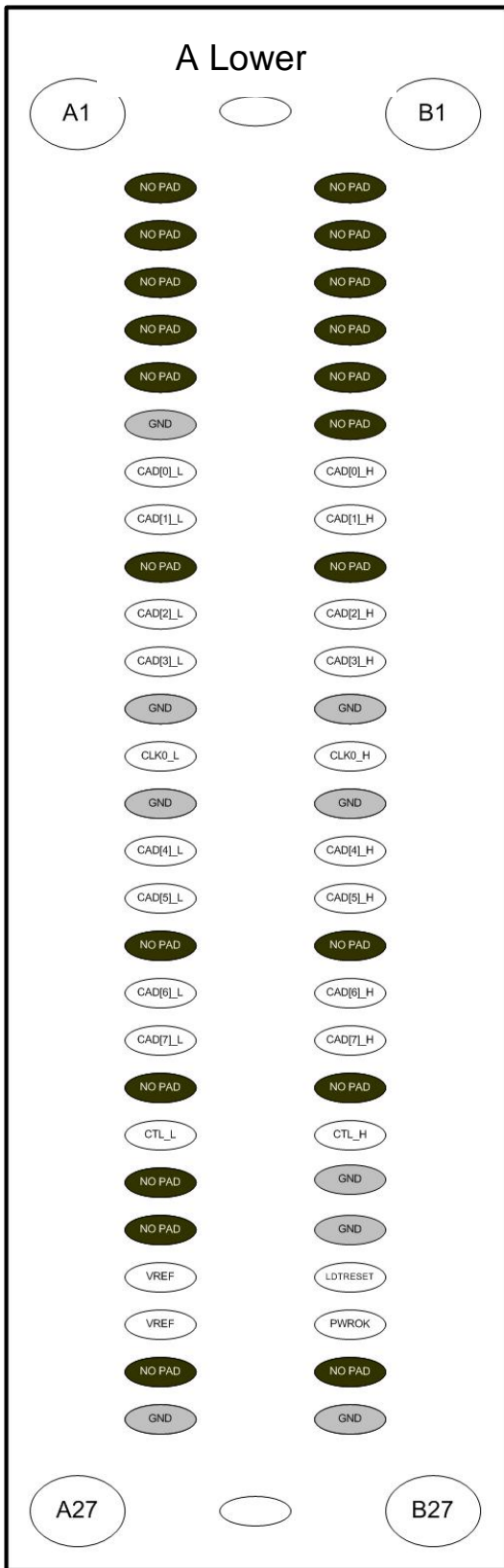
The following pages show a detailed pin out for 4 probing connections required for capturing both Receive and Transmit traffic simultaneously on a 16 bit HT link.

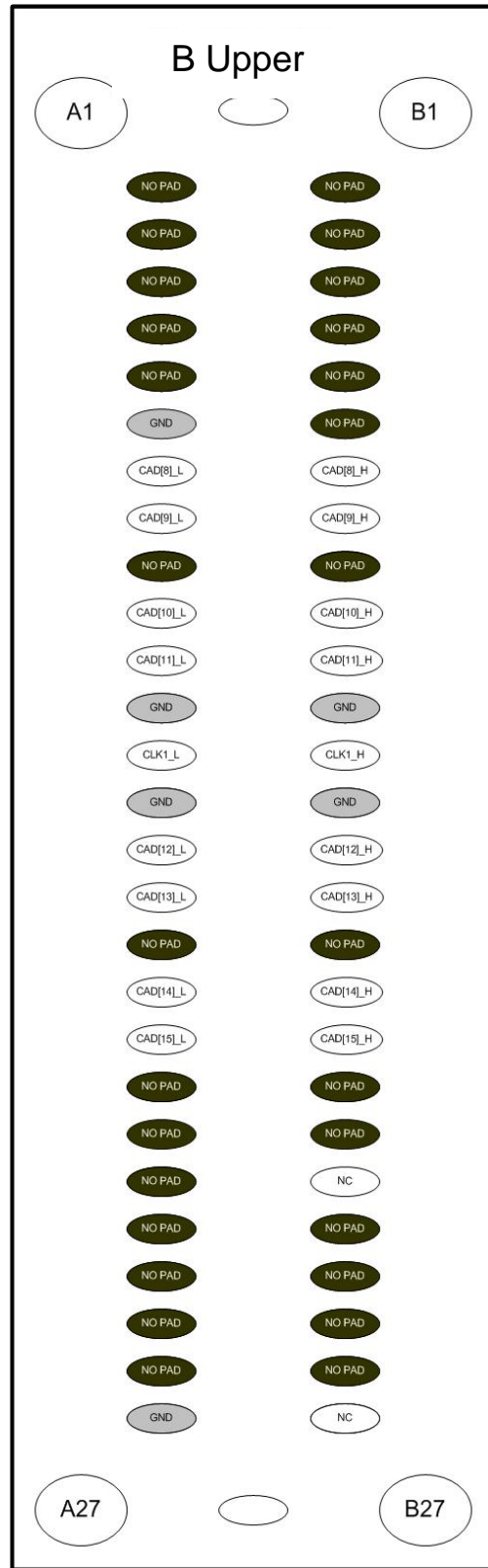
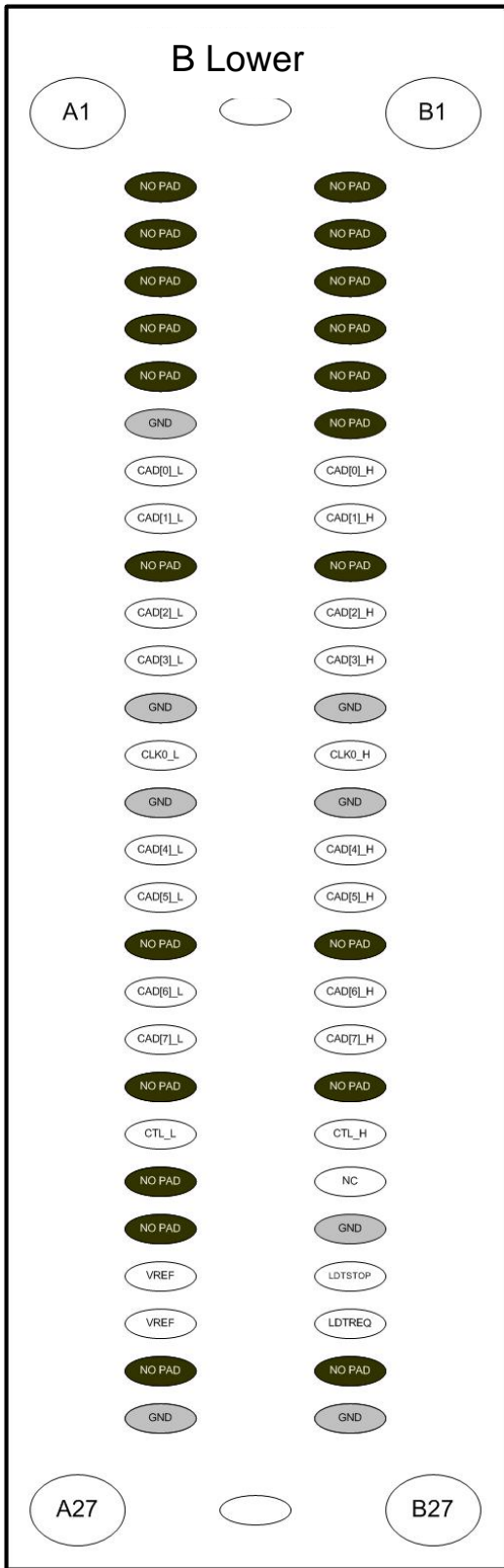
For 8 bit TX and RX data capture use A Lower for TX and B Lower for RX.

For 16 bit TX only, two probing connections are required – A Lower and A Upper.  
For 16 bit RX only, two probing connections are required – B Lower and B Upper.

Signals must be routed to the pads specified. If there is a problem, please contact FuturePlus Systems for more information.

The following diagrams describe certain probing positions as “NO PAD” and others as “NC”. NC indicates the presence of a pad but no connection to circuitry. NO PAD indicates that there is no physical pad on the board. Only pads with signal names need to be created on the board, which may ease trace routing.



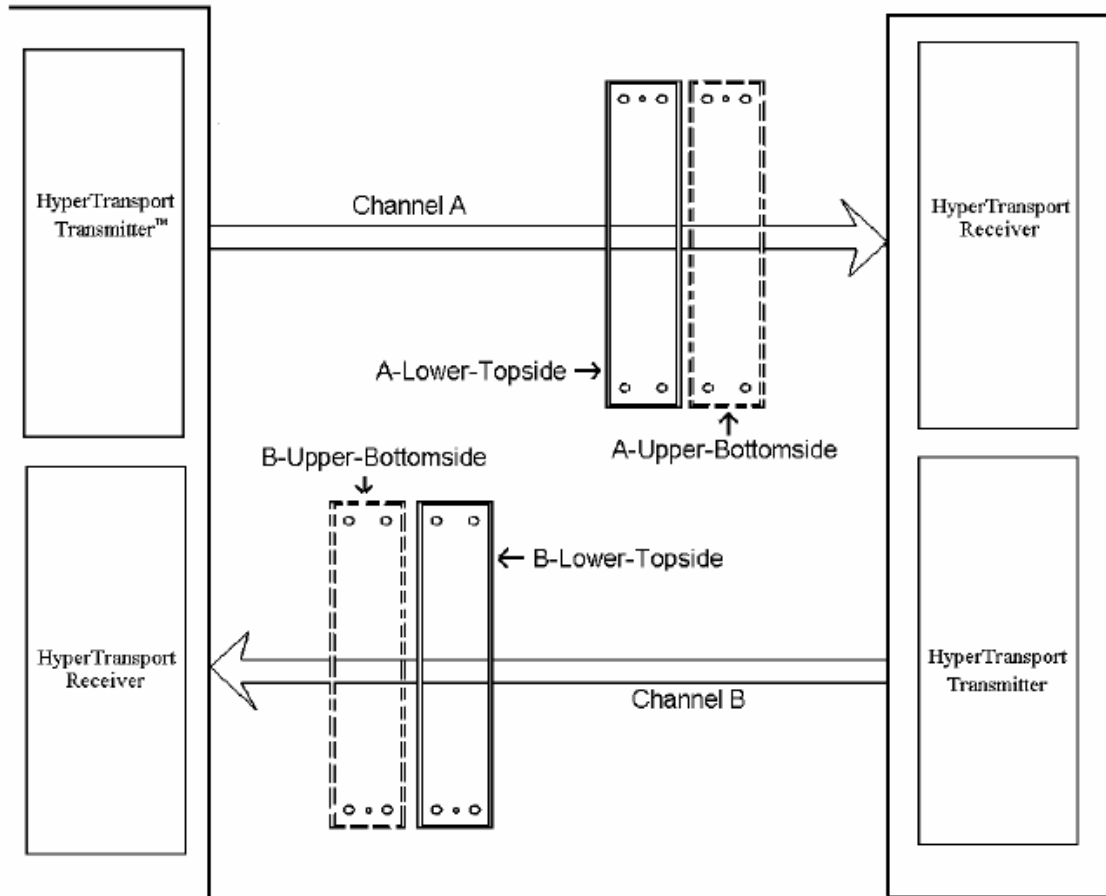


## Industry-Standard Connectorless Method of Probing – FS2244

The FS2244 uses an “Industry-Standard connectorless” approach for probing HyperTransport links. This is similar to the technology and approach described for the FS2243 probe, but it differs in its geometry and its pinout. Like the FS2243, this method is easier to implement on targets with low layer counts and/or tight space requirements, because it does not require tip resistors on the target and only brings 10 bits to each of the 2 probing locations required per link. Additionally, it can be implemented using standard PCB pad features and can therefore be designed into a target board at no cost increase and used when needed with little additional commitment of time and money.

Refer to the discussion in the previous section for placement of the probing locations. It is recommended that A Lower and B Lower be placed on the top side and A Upper and B Upper be placed on the bottom side of the target board.

This layout was designed to minimize the impact of probing a HT link utilizing a microstrip layout where the upper and lower bytes are routed on different layers.



NOTE – dashed lines for “Upper-Bottomside” connectors for use when probing TX and RX on 16 bit links

## Industry-Standard Connectorless probing footprint

The footprint designed for use with the FS2244 is shown below in *Figure 13*: Please note that not all probe pads are required, reference the pinouts described in this document.

Layout guidelines:

Vias in pads are not recommended. A via that is tangential to the pad is allowed. There must be a solder mask between all pads. Recommended pad finish is HASL, immersion silver, or gold over nickel.

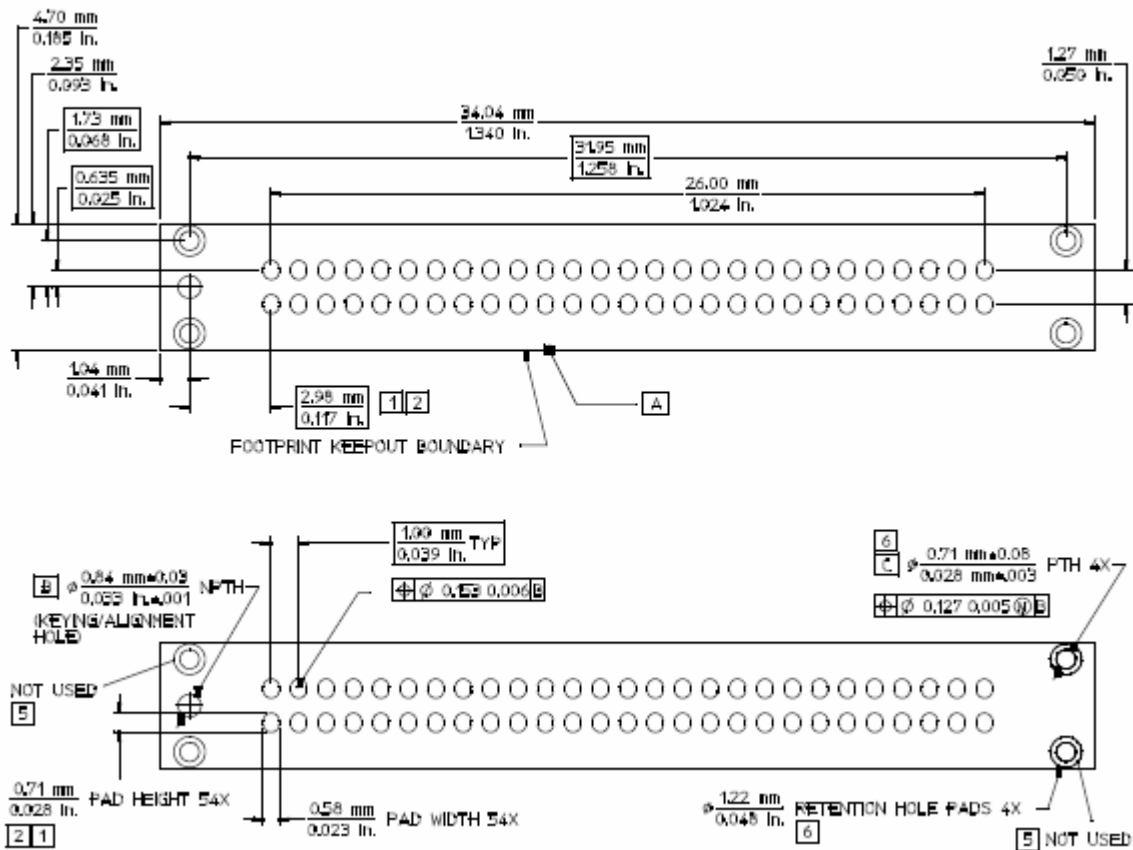


Figure 13 – Mechanical layout for FS2244 Industry-Standard connectorless probing

### Retention module

A retention module (*Figure 14*) is required to provide the mechanical support of the connectorless probe to the target board. The module is simply attached to the board by soldering its legs to the plated through holes that are part of the footprint described above. The FS2244 is then connected to the target by placing the probe head into the retention clip, taking care to maintain polarity, and screw down the captive fasteners. Five pcs of the retention module are provided with your probe. Additional retention modules can be ordered from FuturePlus Systems. They can also be ordered in a kit of 5 pcs from Agilent (part number E5403A) or from Precision Interconnect/Tyco (part number is 600-0153-01).

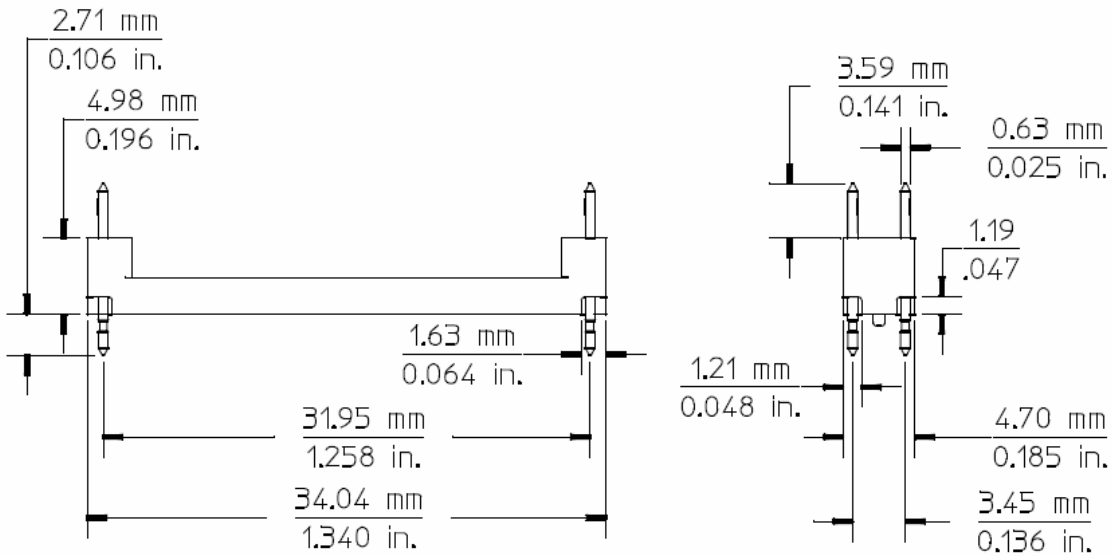
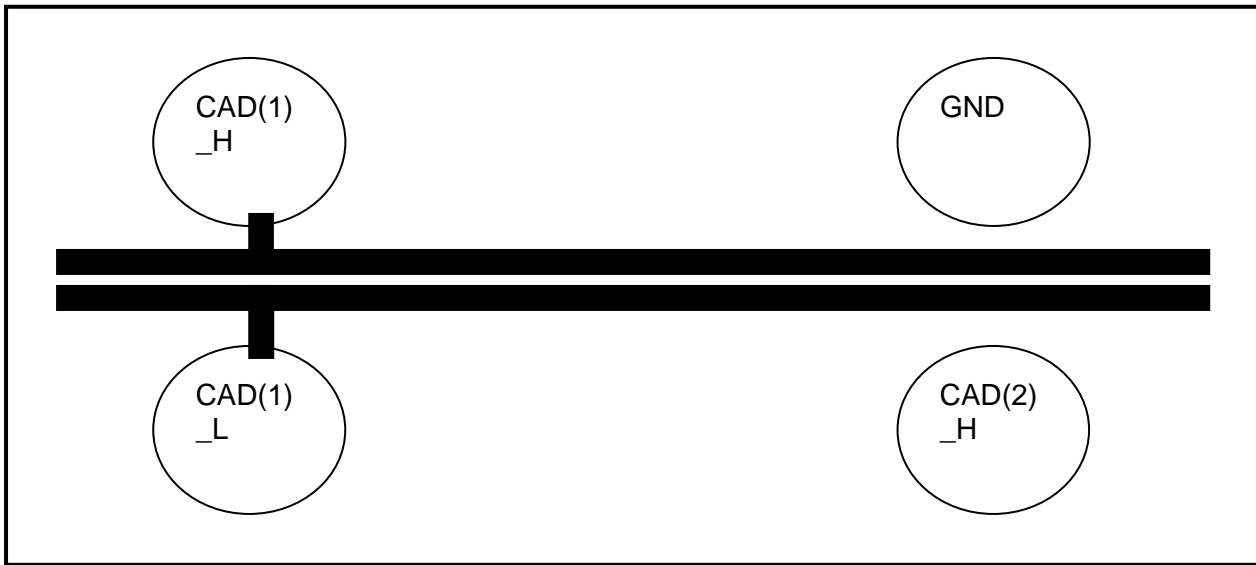


Figure 14 – Mechanical layout for FS2244 Industry-Standard connectorless probing retention module

Connector - less probe trace routing – Differential signals in same column, different row

The goal is to minimize the disruption to the standard HT differential pair routing between devices and to minimize any differences in position on the link where each signal is probed, as well as introduce only a minimal and equal length stub to each pad. It is also important to maintain the spacing between signals in a pair. The following is an example of a layout for 1 pair where the signals are in the **same column** but **different rows**, which is how the FS2244 probe is arranged:



The following pages show a detailed pin out for 4 probing connections required for capturing both Receive and Transmit traffic simultaneously on a 16 bit HT link.

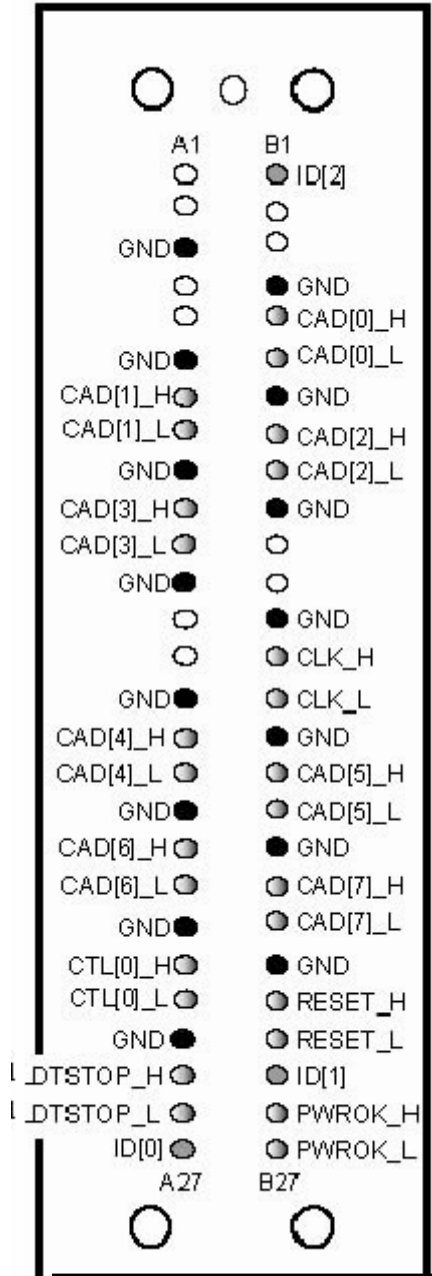
For 8 bit TX and RX data capture use A Lower for TX and B Lower for RX.

For 16 bit TX only, two probing connections are required – A Lower and A Upper.

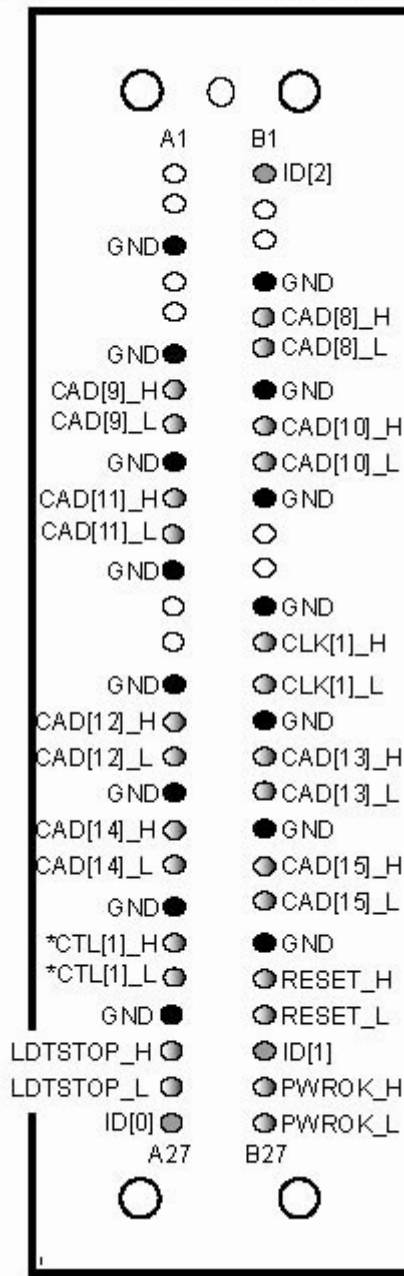
For 16 bit RX only, two probing connections are required – B Lower and B Upper.

Signals must be routed to the pads specified. If there is a problem, please contact FuturePlus Systems for more information.

The following diagrams describe certain probing positions as “NO PAD” and others as “NC”. NC indicates the presence of a pad but no connection to circuitry. NO PAD indicates that there is no physical pad on the board. Only pads with signal names need to be created on the board, which may ease trace routing.



A or B Lower



A or B Upper

Sideband signals – The sideband signals can be brought to either the Lower or Upper footprint, but they do not need to be brought to both. The FS2244 probe provides Flying Leads for the connection of the \*\_H side of the 3 sideband signals (LDTSTOP, RESET, and PWROK) to a **separate logic analyzer card**. The \*\_L side of these signals is not probed.

## 7.0 References

FS2240 Quickstart, FuturePlus Systems, Bedford, NH, [www.futureplus.com](http://www.futureplus.com)

FS2240 Product Description, FuturePlus Systems, Bedford, NH, [www.futureplus.com](http://www.futureplus.com)

FS2240 User's Guide, FuturePlus Systems, Bedford, NH, [www.futureplus.com](http://www.futureplus.com)

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[www.agilent.com](http://www.agilent.com)

FuturePlus® Systems Corporation  
6455 N Union Blvd Suite 202  
Colorado Springs, CO 80918  
719 278-3540

[sales@futureplus.com](mailto:sales@futureplus.com)  
[www.futureplus.com](http://www.futureplus.com)

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