

# FS1140 & FS1141 DDR Protocol Checking & Performance Tool



FuturePlus Systems

Power Tools For Bus Analysis



**Agilent Technologies**

— *Premier Solution Partner*

# Overview

- The FS1140 & FS1141 are new DDR Protocol Checking and Performance Tools that work in conjunction with FuturePlus DDR Analysis Probes. The FS1140 & FS1141 enhance the usability and value of the Agilent logic analyzer by checking acquired data for protocol violations and also execute several performance measurements.
- The FS1140 & FS1141 operate within the Agilent B4606A or B4607A Advanced Customization Environment (ACE) for 1680, 1690, and 16900 Series logic analysis systems. The B4606A or B4607A allow you to quickly sift through large amounts of data during your digital system validation.
- With the B4606A development and runtime package, you can customize your logic analyzer's data analysis and displays as well as create scripts and interactive dialogs to automate repetitive tasks. The seamless integration of Microsoft's® Visual Basic for Applications (VBA) into the logic analyzer application makes this possible.
- The B4607A contains a runtime only package for execution of previously developed applications like the FS1140 & FS1141.

## FS1140 & FS1141 Compatibility

- The FS1140 is compatible with the FS2332 DDR2 DIMM and FS2337 DDR2 SO-DIMM analysis probes.
- The FS1141 is compatible with the FS2336 DDR1 DIMM and FS2333 DDR1 SO-DIMM analysis probes.

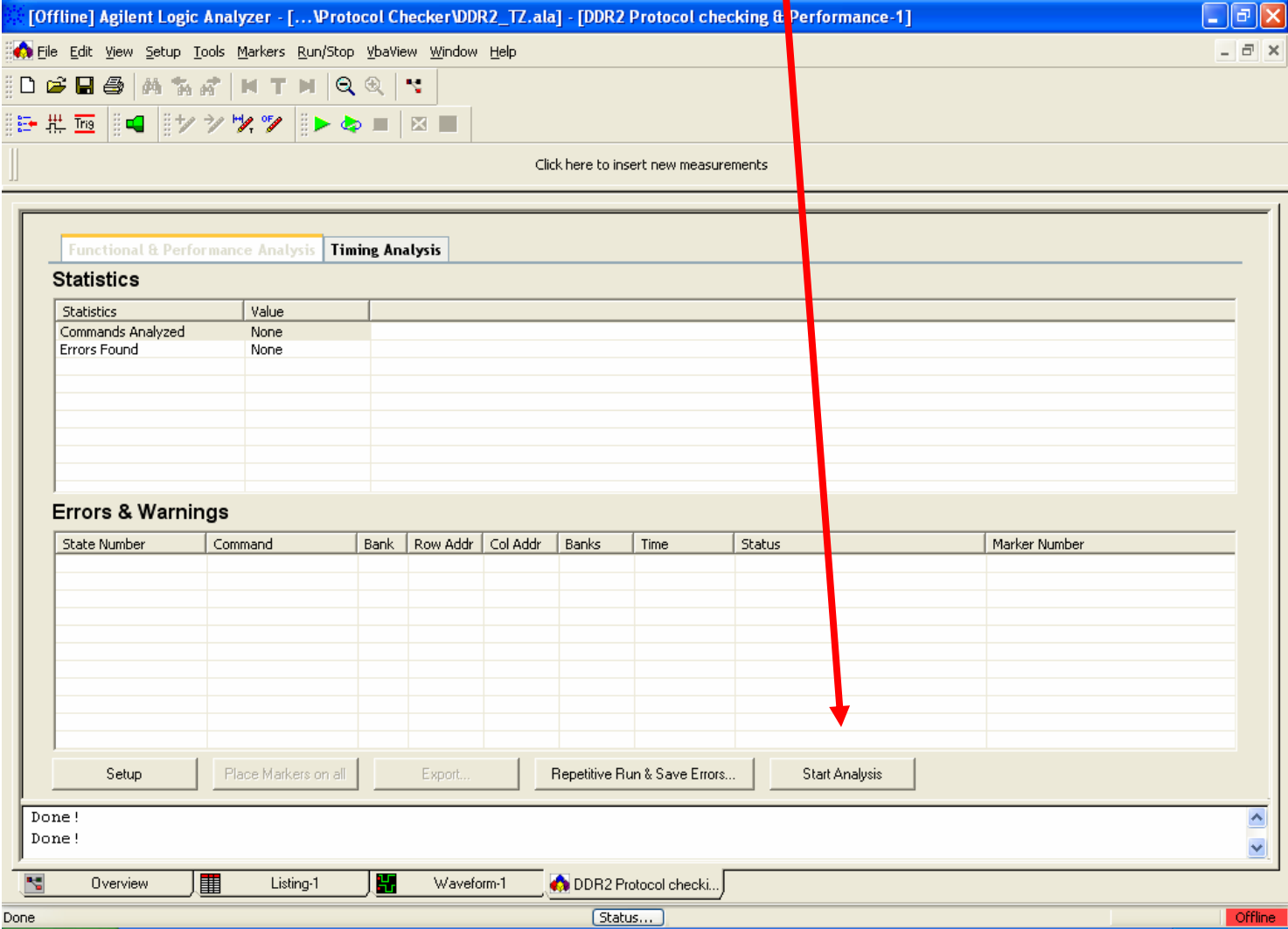
# FS1140 & FS1141 Software Requirements

- The FS1140 & FS1141 require the latest version of the Agilent Logic Analyzer Software, Version 03.20.0000 or higher
- The FS1140 & FS1141 require the Agilent B4606A or B4607A Advanced Customization Environment (ACE) to be installed in the logic analyzer
- At this time it is not possible to install a demo version of the ACE in the logic analyzer. Therefore it is also not possible to install a demo version of the FS1140 and FS1141 in the logic analyzer



# What the new tool looks like continued

- Click on the Start Analysis tab



# What the new tool looks like continued

- You can see the Statistics and the errors found

The screenshot displays the Agilent Logic Analyzer interface. The main window is titled "[Offline] Agilent Logic Analyzer - [...\Protocol Checker\DDR2\_TZ.ala] [DDR2 Protocol checking & Performance-1]". The interface includes a menu bar (File, Edit, View, Setup, Tools, Markers, Run/Stop, YbaView, Window, Help), a toolbar with various analysis tools, and a central workspace. The workspace is divided into two tabs: "Functional & Performance Analysis" and "Timing Analysis". The "Statistics" section is active, showing a table of performance metrics. Below it, the "Errors & Warnings" section displays a table of detected errors. At the bottom, there are buttons for "Setup", "Place Markers on all", "Export...", "Repetitive Run & Save Errors...", and "Start Analysis". A status bar at the bottom indicates "Done!" and "Status...".

Statistics	Value
Commands Analyzed	896
Errors Found	504
Average Refresh Time	100 ns
Min Refresh Time	100 ns
Max Refresh Time	100 ns
Total Clocks	2048
Number of Read Clocks	128
Number of Write Clocks	128
% Clocks w/Valid Cnds	44%
% of Clocks w/Valid Data	50%

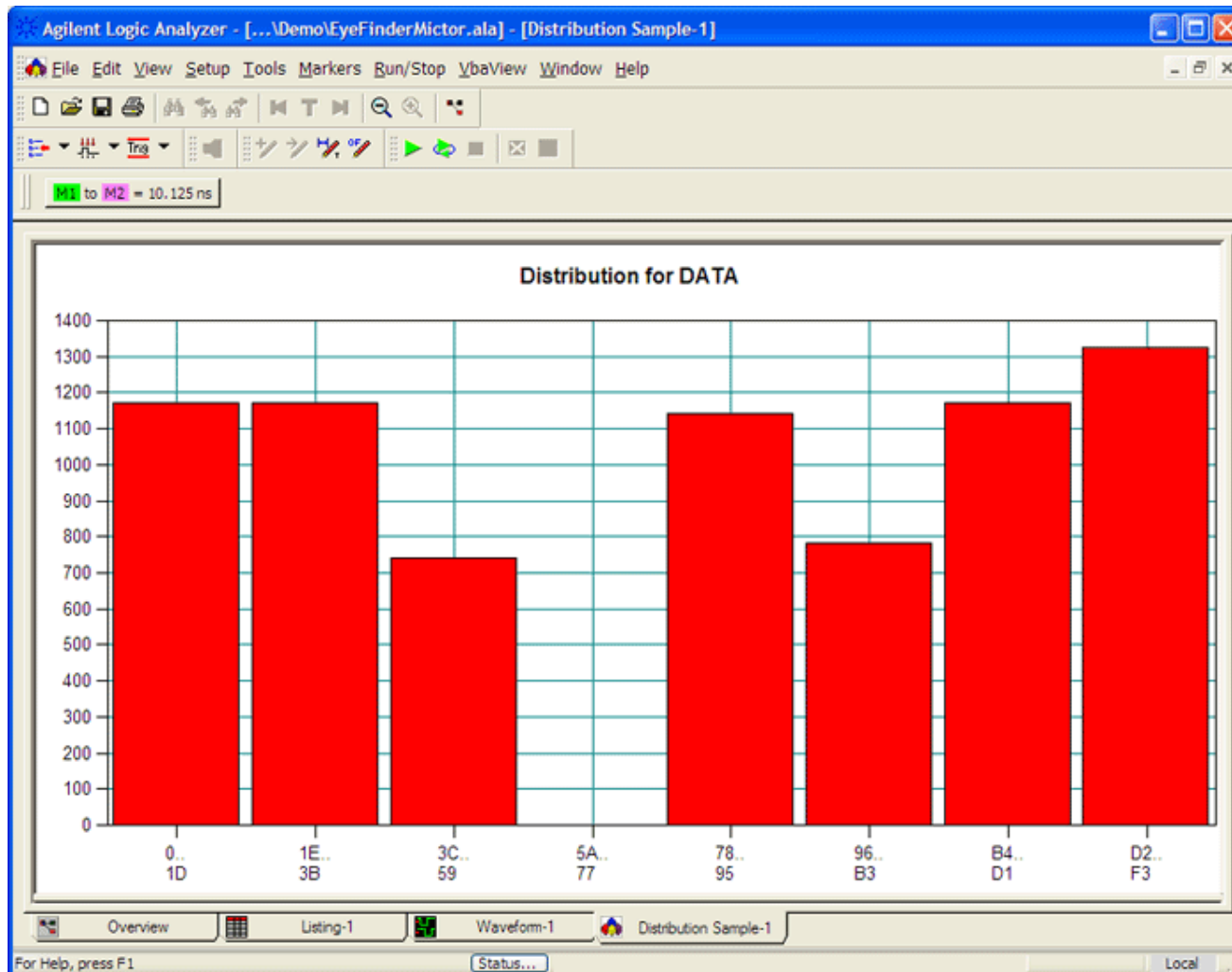
State Number	Command	Bank	Row Addr	Col Addr	Banks	Time	Status	Marker Number
-1120	Active	0	294		APPP	-56 us	Error - Bank not precharged before ...	DDR1
-1118	Active	0	292		APPP	-55.9 us	Error - Bank not precharged before ...	DDR2
-1116	Active	0	296		APPP	-55.8 us	Error - Bank not precharged before ...	DDR3
-1114	Active	0	290		APPP	-55.7 us	Error - Bank not precharged before ...	DDR4
-1112	Active	0	294		APPP	-55.6 us	Error - Bank not precharged before ...	DDR5
-1110	Active	0	292		APPP	-55.5 us	Error - Bank not precharged before ...	DDR6
-1108	Active	0	296		APPP	-55.4 us	Error - Bank not precharged before ...	DDR7
-1106	Active	0	291		APPP	-55.3 us	Error - Bank not precharged before ...	DDR8
-1104	Active	0	295		APPP	-55.2 us	Error - Bank not precharged before ...	DDR9
-1102	Active	0	293		APPP	-55.1 us	Error - Bank not precharged before ...	DDR10

## Functional and Performance Analysis Detail

- **The performance analysis of the DDR bus over the entire captured trace file is displayed in the “Statistics” section. This shows information regarding the total number of clock cycles and Commands that are included in the analyzed trace file, as well as the total number of errors found. The error count is based on the errors selected in the Setup. Also, included in this display is information on the Read, Write and Data activity occurring during the captured trace file.**
- **This section of the tool displays comprehensive information about the location and nature of each selected error found in the captured trace file. The user can scroll through the error listing and either select on error by left clicking on the error to set a “DDR” marker in the State and Waveform listings, or the user can select the “Place Markers on All” button which will place uniquely numbered markers (DDR<sub>x</sub>) on all identified errors. The error markers allow the user to switch between the Tool, State and Waveform information easily during the analysis of the activity related to an error.**

# Export Function

- This function takes the data captured and exports it in .csv format to a user-selected location. The user can then produce graphs such as the following:



# What the new tool looks like continued

## Now select the Timing Analysis Measurement

The screenshot displays the Agilent Logic Analyzer interface. A red arrow points to the 'Timing Analysis' tab in the 'Functional & Performance Analysis' section. Below this, the 'Statistics' table shows various performance metrics, and the 'Errors & Warnings' table lists specific timing errors.

**Statistics**

Statistics	Value
Commands Analyzed	896
Errors Found	504
Average Refresh Time	100 ns
Min Refresh Time	100 ns
Max Refresh Time	100 ns
Total Clocks	2048
Number of Read Clocks	128
Number of Write Clocks	128
% Clocks w/Valid Cmds	44%
% of Clocks w/Valid Data	50%

**Errors & Warnings**

State Number	Command	Bank	Row Addr	Col Addr	Banks	Time	Status	Marker Number
-1120	Active	0	294		APPP	-56 us	Error - Bank not precharged before ...	DDR1
-1118	Active	0	292		APPP	-55.9 us	Error - Bank not precharged before ...	DDR2
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Buttons: Setup, Place Markers on all, Export..., Repetitive Run & Save Errors..., Start Analysis

Copying data to window  
Done!

Overview | Listing-1 | Waveform-1 | DDR2 Protocol checki... | Status... | Offline



# What the new tool looks like continued

## Select attributes of your bus

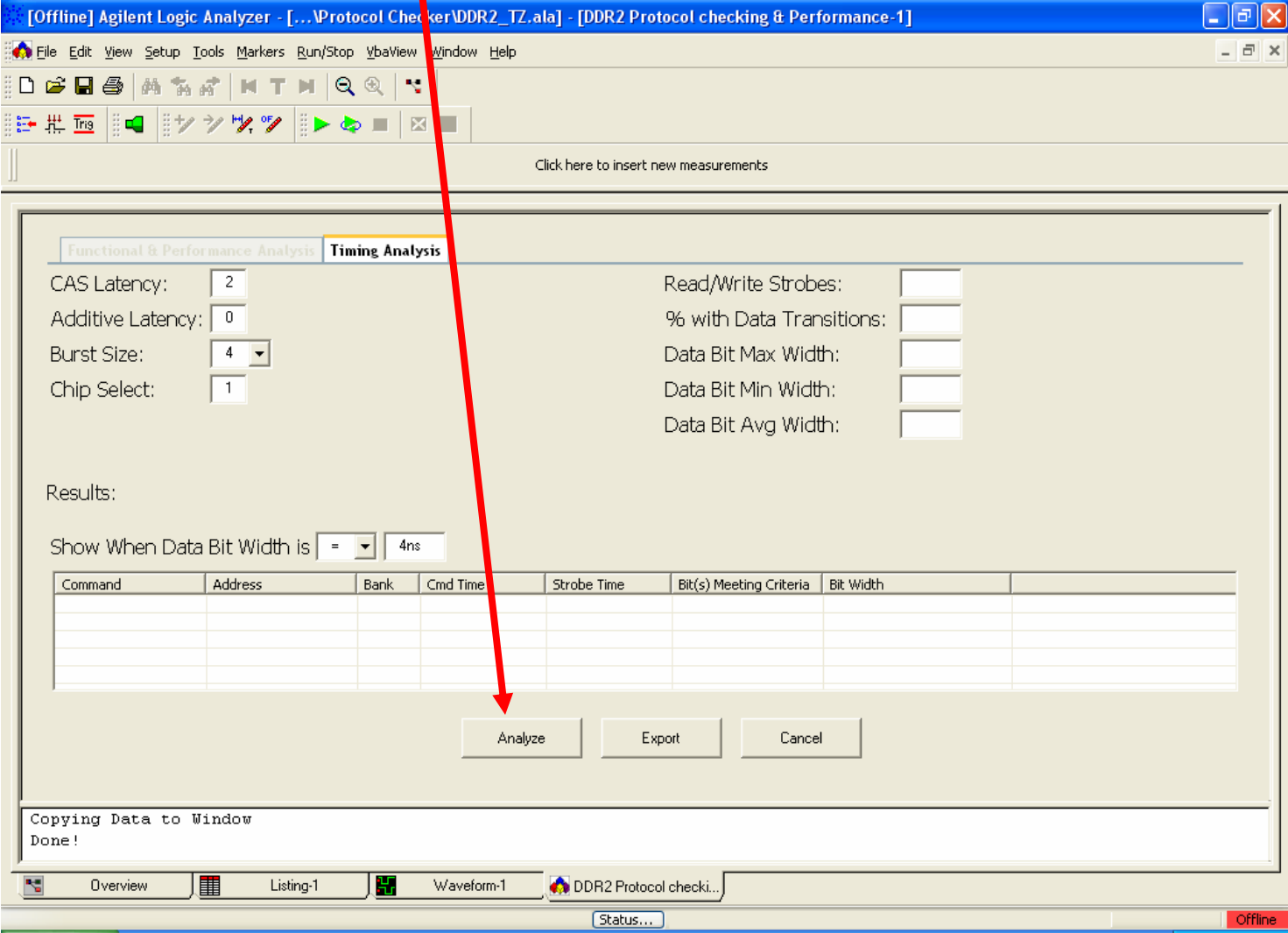
The screenshot shows the 'Timing Analysis' window in the Agilent Logic Analyzer. The window title is '[Offline] Agilent Logic Analyzer - [...\Protocol Checker\DDR2\_TZ.ala] - [DDR2 Protocol checking & Performance-1]'. The menu bar includes File, Edit, View, Setup, Tools, Markers, Run/Stop, WaveView, Window, and Help. The toolbar contains various icons for file operations, analysis, and navigation. Below the toolbar is a text prompt: 'Click here to insert new measurements'. The main area is divided into two tabs: 'Functional & Performance Analysis' and 'Timing Analysis'. The 'Timing Analysis' tab is active and contains the following settings:

- CAS Latency: 2
- Additive Latency: 0
- Burst Size: 4 (dropdown)
- Chip Select: 1
- Read/Write Strobes: [ ]
- % with Data Transitions: [ ]
- Data Bit Max Width: [ ]
- Data Bit Min Width: [ ]
- Data Bit Avg Width: [ ]

Below these settings is a 'Results:' section with a dropdown menu set to '=' and a text box containing '4ns'. Below this is a table with the following columns: Command, Address, Bank, Cmd Time, Strobe Time, Bit(s) Meeting Criteria, and Bit Width. The table is currently empty. At the bottom of the window are three buttons: 'Analyze', 'Export', and 'Cancel'. A status bar at the bottom shows 'Copying Data to Window Done!' and a 'Status...' button. The bottom right corner of the window has a red 'Offline' indicator.

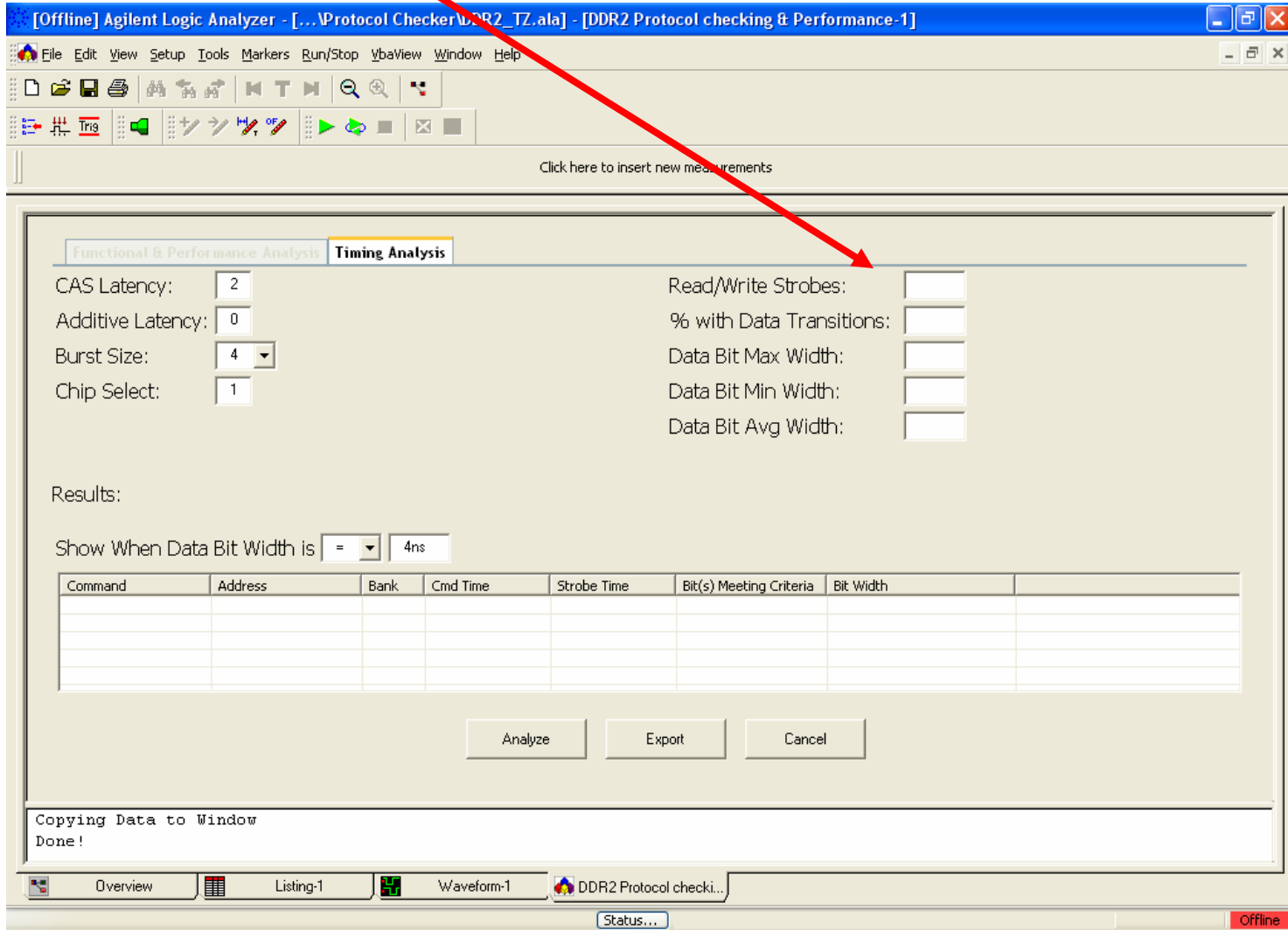
# What the new tool looks like continued

■ Click on Analyze tab:



# What the new tool looks like continued

- Read/write strobes will increment to end of file



# What the new tool looks like continued

## ■ The final screen will look like:

The screenshot shows the 'Timing Analysis' tab in the Agilent Logic Analyzer. The configuration parameters are as follows:

CAS Latency:	2	Read/Write Strokes:	1024
Additive Latency:	0	% with Data Transitions:	50%
Burst Size:	4	Data Bit Max Width:	1.67 ns
Chip Select:	1	Data Bit Min Width:	1.67 ns
		Data Bit Avg Width:	1.67 ns

Results:

Show When Data Bit Width is

Command	Address	Bank	Cmd Time	Strobe Time	Bit(s) Meeting Criteria	Bit Width
Read	0 1318	0	1.972063 us	1.983732 us	0,4,18,40,41	1.67 ns
Read	0 1318	0	1.972063 us	1.997068 us	0,4,18,40,41	1.67 ns
Read	0 1318	0	1.972063 us	2.010404 us	0,4,18,40,41	1.67 ns
Read	0 1318	0	1.972063 us	2.02374 us	0,4,18,40,41	1.67 ns
Read	0 131C	0	1.975397 us	1.983732 us	0,4,18,40,41	1.67 ns

Buttons: Analyze, Export, Cancel

Copying Data to Window  
Done!

Overview | Listing-1 | Waveform-1 | DDR2 Protocol checki... | Status... | Offline

# Timing Analysis Detail

- **The timing analysis window provides an analysis of each Data bit's window during every data burst across an entire TimingZoom trace. The user can set a threshold criteria in this window and then select whether the data windows to be identified should be equal to, greater than or equal to, or less than or equal to that value. All data bits during any burst captured in a TZ trace will be listed in the Timing Analysis window.**
- **Additionally the tool provides some overall statistics on what was measured in the TZ trace that was analyzed. This includes the number of Read and Write strobcs analyzed, the % of data strobcs with data transitions occurring, as well as the maximum, minimum and average Data Bit widths across all bits during all bursts in the TZ trace.**

# Summary

The FS1140 & FS1141 check the following DDR protocol violations:

- Refresh with active banks
- Write to a bank that is not active
- Read to a bank that is not active
- Mode register set with active banks
- Bank not Pre-charged before being Activated
- Data Burst interrupted by a Command

# Summary continued

The FS1140 & FS1141 display summary statistics of the transactions captured in the trace file

- Percent of Write and Read commands
- Percent of clock cycles with data activity

The FS1140 & FS1141 display measurements of the Data Window eye width on a bit by bit basis across all Timing Zoom data in the trace file.

- Signals with the smallest eye width identified

# To place your order

United States:

## FuturePlus Systems

Power Tools For Bus Analysis

6455 N. Union Blvd. Ste 202  
Colorado Springs, CO 80918  
719 278 3540  
[www.futureplus.com](http://www.futureplus.com)

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