



Serial Rapid I/O Logic Analyzer Probing Design Guide for the FS441x

FuturePlus Systems® Corporation
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1.0 Introduction

The FuturePlus Systems® flexible Serial Probe is a logic analyzer pre-processor capable of non-intrusively probing 8 channels of serial communication interfaces. Through the use of a flexible SERDES device and FPGA, it is able to receive and decode a variety of single and multi-lane protocols.

The FS441X is the Serial Rapid I/O or SRIO version of the product and supports serial data rates of 1.25Gbps to 3.125 Gbps. Considerable flexibility allows various mid-bus probe lane arrangements (i.e. pad assignments) to be accommodated.

The FS441X is designed to handle two directions of a link, or a single direction from each of two unrelated links (A and B), at lane widths of 1 or 4. The probe hardware and Protocol Decode software treat the two links individually. For analysis of interactions between two directions of a link, the logic analyzer inter-machine triggering function is used.

Users are expected to have performed electrical simulation on their design with the SRIO footprint and probe model in place to ensure proper signal quality.

1.1 Objectives

This document is intended to provide FuturePlus Systems customers with information needed for the integration of Logic Analyzer Probing for SRIO into their designs. The solutions given here only concern a mid-bus probing solution in which the LAI footprint is designed into the target system. If other probing solutions are required please contact FuturePlus Systems for more information.

Although information concerning SRIO topology and specifications will be given, this document is not intended to take the place of other SRIO design documentation. It is assumed that a design team utilizing this document for their design constraints will validate their designs through pre and post route electrical simulation and keepout volume analysis.

1.2 Nomenclature

LAI refers to the Analysis Probe, FS441X. A “channel” refers to either a transmit differential pair OR receive differential pair for a given lane. A “link”, according to the standard, is the set of differential pairs that makes up both directions of the SRIO interconnect. When used in FS441X documentation, a “link” is considered to be the set of differential pairs that make up a single direction of the sRIO interconnect.

2.0 Overview and Configuration Support

2.1 Link Configuration Support

The FS441X provides support for the half size or full size mid-bus direct probing footprint. Flexibility is given to the platform designer to configure a probing solution that best meets the needs of the system. With a single FS441X the following configurations may be probed:

- Both directions of a link (i.e. up and downstream)
- A single direction of a link
- Single directions of 2 unrelated links

When probing both directions of a link, the data may be merged into a single listing display on the Analyzer, to view requests and associated responses.

The FS441X cannot probe a x1 link and a x4 link in one FS441X box.

The FS441X supports the standard patterns of channel assignments to the pads of the PCI Express Mid-Bus probe footprint. These are described in section 4.2.5. Additional unspecified patterns may also be supported. Contact FuturePlus Systems directly for more information.

2.2 Reference Clock(s) To the FS441X

The Serial RapidIO standard does not include a reference clock connection between transmitter and receiver. The FS441X provides an internal reference clock generator that supports probe operation at the following link frequencies and accuracy:

1.25 Gbps	within 100 PPM as required by sRIO specification
2.5 Gbps	within 100 PPM as required by sRIO specification
3.125 Gbps	within 100 PPM as required by sRIO specification

There are some cases where the FS441X requires an external reference clock connection when probing Serial RapidIO. It is required for any of the following conditions:

Link transmitter frequency accuracy is outside of 100 PPM.
Link transmitter frequency is other than 1.25, 2.5, or 3.125 Gbps.
During 10-bit mode probe operation

When an external reference clock connection is required, the FS441X reference clock probe must be connected to a properly terminated, low jitter reference clock source on the target. The reference clock probe is a high-impedance type and may be connected anywhere a clean wave shape is available. The quality of the received clock can be verified by observing the buffered signal at the Ref Clock Out connector with an oscilloscope.

When external reference clock is used, if the target has only one reference clock for both directions (common clocking), the FS441X only needs one reference clock probe connected (Reference clock probe A). If the target has separate oscillators for both directions (distinct clocking), the FS441X would need both reference clock probes connected (Reference clock probes A and B).

When using external reference clocks, the FS441X has flexibility in supporting reference clock multipliers. The default reference clock multiplier mode is:

20x reference clock frequency multiplier	Usable from 1.2 to 3.125 Gbps
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If necessary, the FS441X can also support the following reference clock multiplier. Contact FuturePlus Systems for information on how to run the probe in this mode:

25x reference clock frequency multiplier	Usable from 1.2 to 2.8 Gbps
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In the FS441X, the selection of reference clocking modes is always set the same for both directions (for both link processors A and B). These modes include internal versus external reference clock, internal reference clock speed, and external reference clock multiplier.

Note that this clock can be a dedicated clock. Alternately, the signals may be a tap off an existing clock, since the probes are designed to not significantly load the signals. In all cases, appropriate line terminations must be provided on the target. However, this needs to be verified by the system platform designers to verify proper functionality. At all times the FS4400 must be presented with a reference clock that has a clean wave shape. See Reference Clock Model (Fig. 7) for more information.

3.0 Mechanical Design

This section contains mechanical design details (footprint dimensions, keepout volumes, and part numbers) of the midbus LAI and the reference clock pin header.

3.1 Midbus Logic Analyzer interface

The FuturePlus Systems FS441X utilizes the Samtec Spirit probing technology. This technology is applied in 2 different footprints.

3.1.1 Full size Footprint Dimensions and Specifications

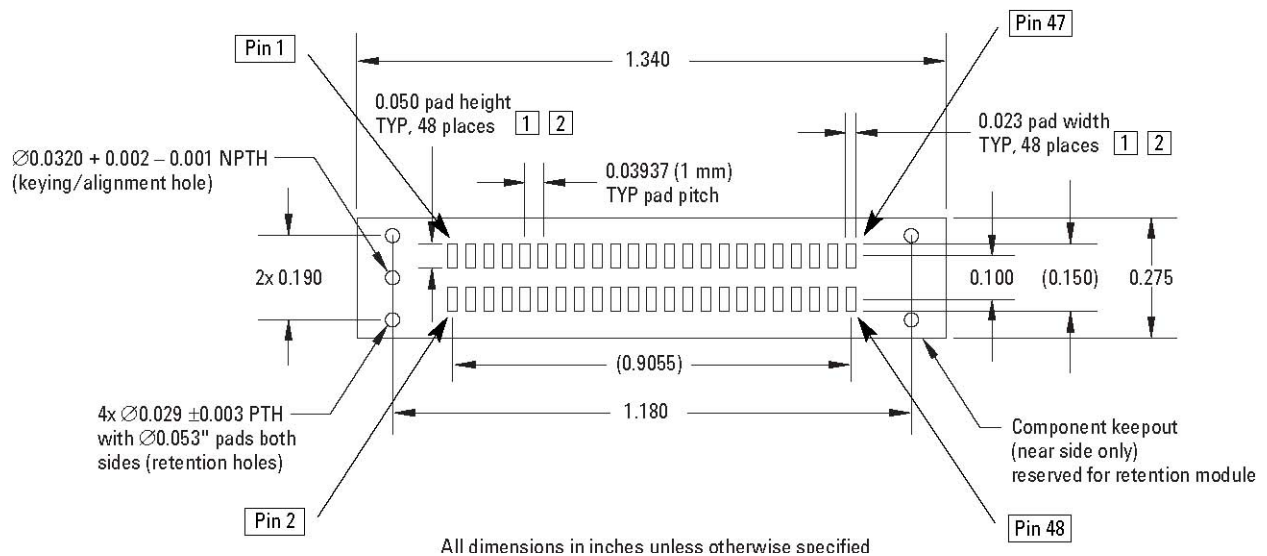


Figure 1 - SRIO LAI industry standard full size footprint dimensions, pin numbering, and specification

3.1.2 1/2 Size midbus Footprint Dimensions and Specifications

Both of the following footprints (Fig. 2 and 3) are compatible with the FS441X product.

NOTES:

1. MUST MAINTAIN A SOLDBRASK WEB BETWEEN PADS WHEN TRACES ARE ROUTED BETWEEN THE PADS ON THE SAME LAYER. HOWEVER, SOLDBRASK MAY NOT ENCRACH ONTO THE PADS WITHIN THE PAD DIMENSIONS SHOWN.
2. VIA-IN-PAD NOT ALLOWED ON THESE PADS. HOWEVER, VIA BODIES MAY BE TANGENT TO THE PAD EDGES.
3. PERMISSIBLE SURFACE FINISHES ON PADS ARE HASL, IMMERSION SILVER, OR GOLD OVER NICKEL.

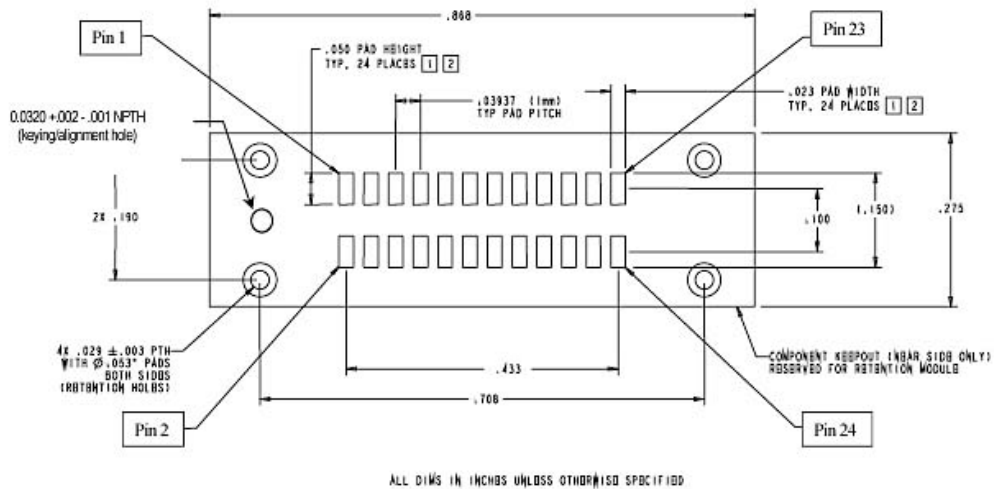


Figure 2 - SRIO LAI industry standard half size footprint dimensions, pin numbering, and specification

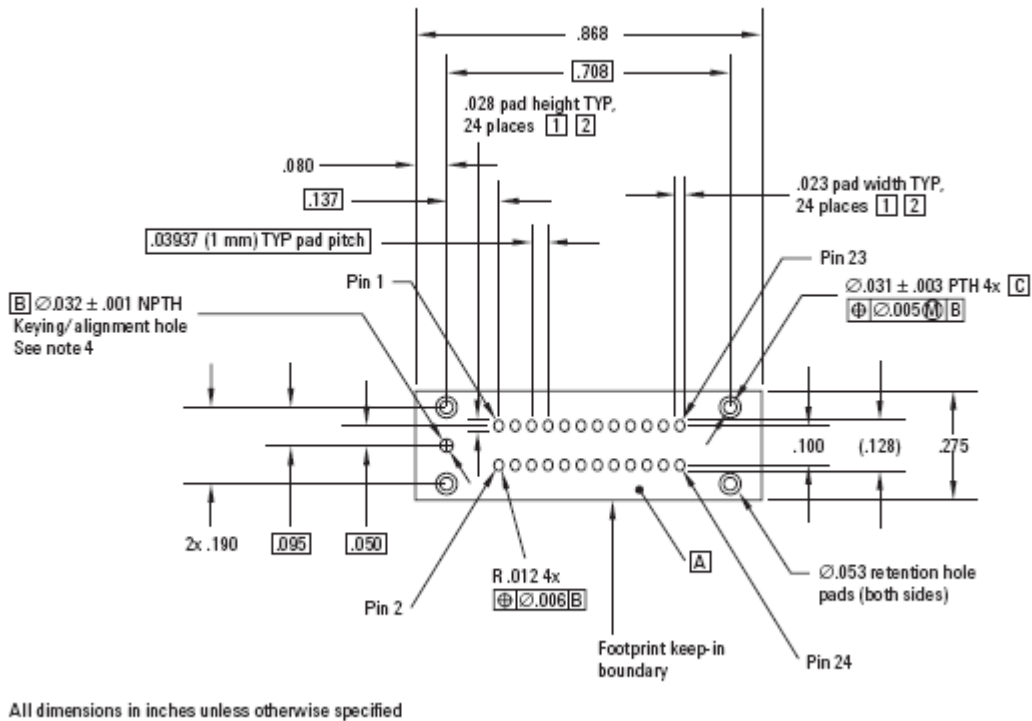


Figure 3- SRIO LAI industry standard compatible but Agilent specific half size footprint dimensions, pin numbering, and specification

3.1.3 Keepout Volume - Full Size Footprint

Keepout volume for the SRIO full size footprint LAI is given in Figure 4.

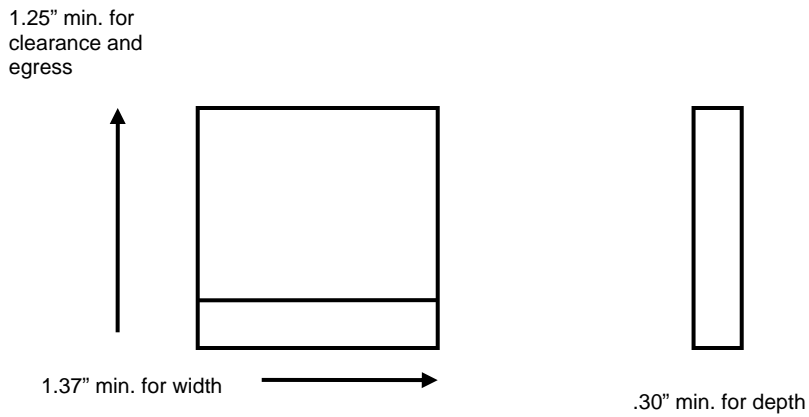


Figure 4- SRIO Full size Footprint LAI Keepout Volume

3.1.4 Keepout Volume - Half Size footprint

Keepout volume for the SRIO half size footprint LAI is given in Figure 5.

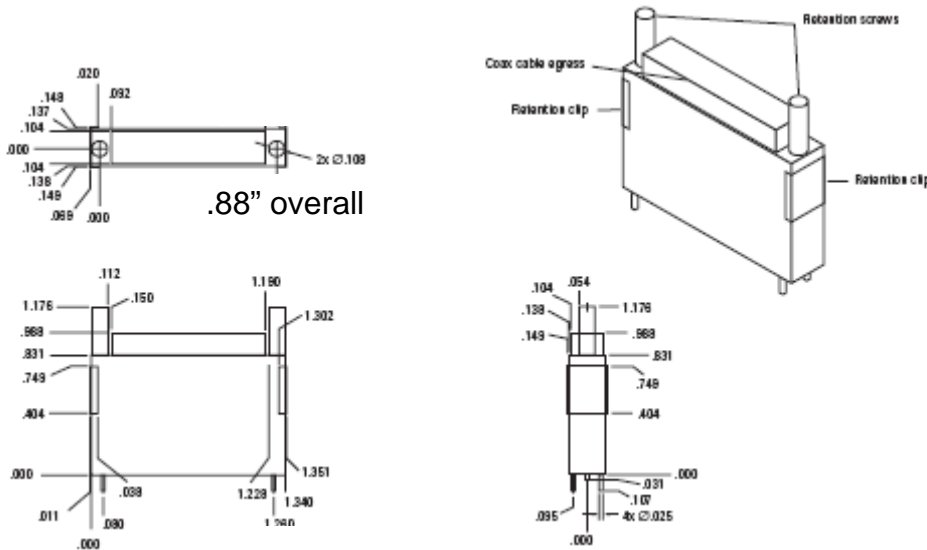


Figure 5- SRIO half size Footprint LAI Keepout Volume

3.2 Reference Clock

3.2.1 Reference Clock Header

If a reference clock is necessary the target must supply a 3-pin header (1 by 3, 0.050" center spacing) for the connection of the reference clock to the LAI. A small high impedance clock probe from the LAI will connect to this header and carry the REFCLKp and REFCLKn signals to the LAI. Note that an individual reference clock header is required for each SRIO clock domain on the system.

The following are recommended part numbers for through-hole and surface mount versions of the 3-pin header for reference clock:

Through-hole: Samtec TMS-103-02-S-S or MilMax 850-10-003-10-001000

Surface mount: Samtec FTR-103-02-S or MilMax 850-10-003-30-001000

Table 1- Reference Clock header pinout

Signal	Pin Number
REFCLKp	1 (or 3) ₁
GND or N/C	2
REFCLKn	3 (or 1) ₁

Note: The LAI is not sensitive to the polarity of the reference clock. Therefore, the probe can be plugged onto the pin header in either orientation.

3.2.2 LAI Reference Clock Probe Keepout Volume

Keepout volumes for the reference clock probes are given in Figure 6. The pin headers reside symmetrically within the keepout volume on the target system.

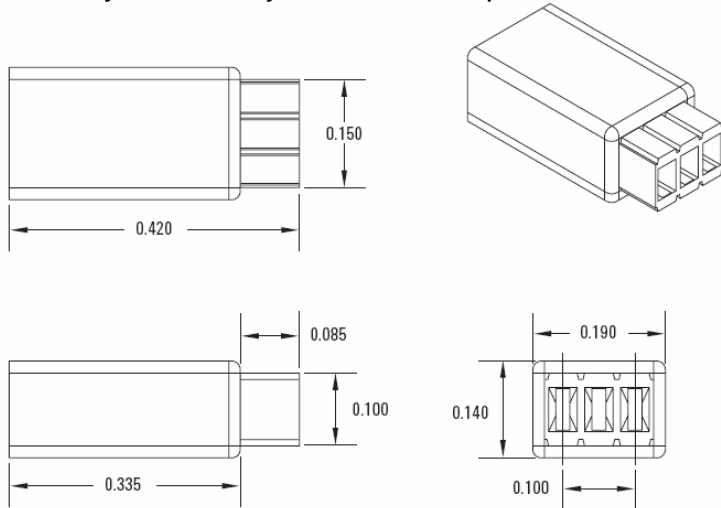


Figure 6- SRIO Reference Clock Probe Keepout Volume

4.0 Electrical Design

This section contains electrical design details of the midbus LAI and the reference clock pin header. These details include LAI eye requirement definition, system impact due to LAI probe presence, LAI routing suggestions, load models, and pin assignments.

4.1 Reference Clock

4.1.1 LAI Reference Clock Electrical Requirements

In cases where a reference clock is used (see section 2.2) the following requirements must be met.

Table 2- LAI electrical requirements on the differential reference clock signals

LAI Requirement	Symbol	Min	Max	Comments
Differential Voltage at Ref Clock Attach Point	Vdiff	800 mVp-p	2V	

Table 3- Reference Clock Frequency

Reference Clock Multiplier	sRIO Data Rate Range	Reference Clock Frequency Range
20 X	1.2 - 3.125 Gbps	60 - 156.25 MHz
25 X	1.2 - 2.8 Gbps	48 - 112 MHz

4.1.2 LAI Reference Clock Probe Load Model

Load models for the reference clock probe are given in this section. System designers will be expected to perform simulations of the reference clock networks with the header and LAI load models to ensure good signal integrity of the reference clocks at the header to the LAI. The pin header parasitics may be obtained from the connector vendor.

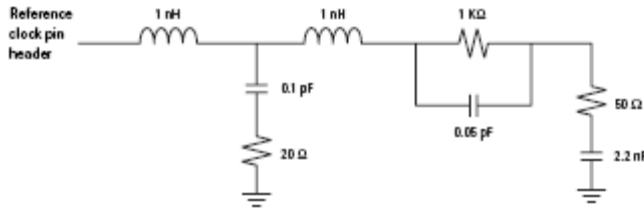


Figure 7- SRIO Reference Clock Probe Load Model

4.2 Midbus LAI

Logical probing of the SRIO bus is achieved through tapping a small amount of energy off the probed signals and channeling this energy to the logic analyzer. In order to avoid excessive loading conditions, the use of tip, or isolation, resistors is employed. These tip resistors are part of the LAI probing interface. These relatively high impedance tip resistors enable the logic analyzer to sample bus traffic without significantly loading the probed signals. A high-level block diagram of a generic SRIO bus with LAI is given in Figure 8. Note that this would be repeated for each differential pair

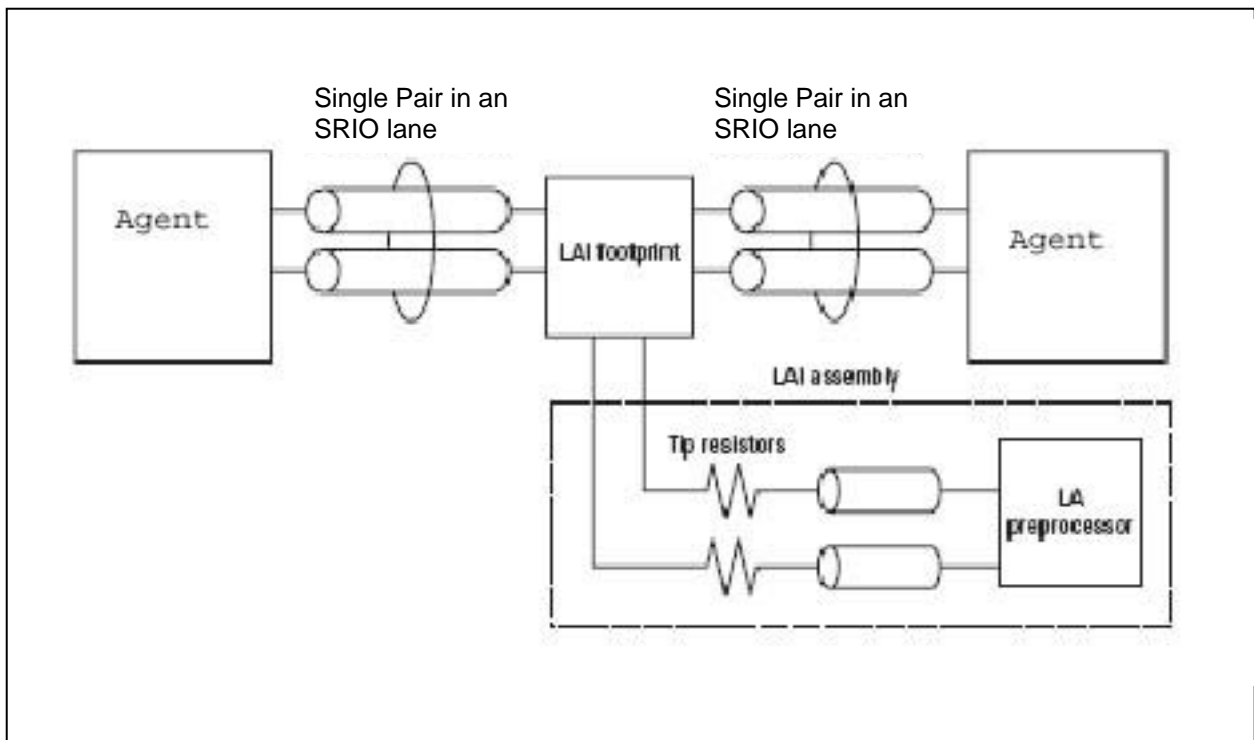


Figure 8- Block diagram example of a generic SRIO bus with a LAI

In order for the LAI to reliably capture logical transactions on the bus, adequate signal eye must be made available to the LAI. It is incumbent upon the platform designers to ensure that sufficient signal eye is available to the LAI while the LAI load is in place so that proper signal tracing is enabled. This must be verified via electrical simulation utilizing the load model provided in Figure 12.

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are described pictorially in Figure 9.

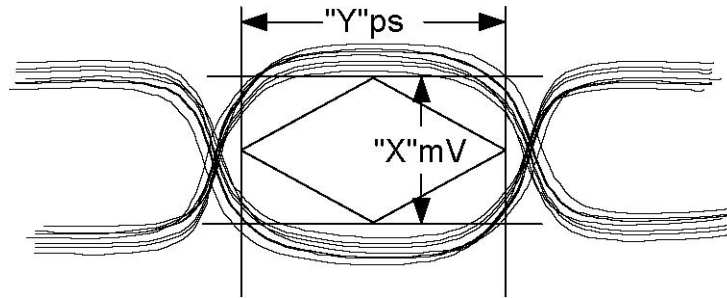


Figure 9-Example of eye specifications as seen at the LAI pad

Table 4 details the specific eye requirements for the FS441X.

Table 4- SRIO LAI Footprint Placement Interconnect Specification

Description	Specification for 1.25Gbps	Specification for 2.5Gbps	Specification for 3.125Gbps
Min Eye height at LAI pad ¹	175mV Vdiff p-p	175mV Vdiff p-p	175mV Vdiff p-p
Min Eye Width at LAI pad, in UI	.29 (jitter tolerance of .71 UI)	.35 (jitter tolerance of .65 UI)	.40 (jitter tolerance of .6 UI)
Length Matching Requirements- Differential Pair	5mil ²	5mil ²	5mil ²
Skew tolerated between lanes of a link-direction.	22ns	9ns	7ns

Note:

- 1- Measured in differential units, e.g. Vdiff p-p = 2x single ended swing
- 2- Differential Interconnect must length match within 5 mils from midbus probe pads to the nearest discontinuities in both directions, e.g. via, capacitor, driver or receiver. Matching within 5 mils on every segment of the SRIO trace is highly recommended. Segments are bounded by: drivers, receivers, capacitors, vias and mid bus probe pads.

In general, special PWB design techniques are required for successful 3 Gbps links. These are beyond the scope of this document.

The eye characteristics given in Table 3 must be maintained for all probed links. Overall, these LAI placement specifications limit the electrical distance between the driver pin and the LAI attach point. Conceivably, probing both directions in lanes of a long SRIO link may require two separate footprints and LAI assemblies, while probing both directions of relatively short links may be accomplished with one LAI. Regardless of implementation, refer to usage restrictions as listed in section 2 - Overview and Configuration Support. The same LAI eye requirements exist for all links substrates (e.g. FR4, cables, etc.)

4.2.1 Impact on SRIO Channel due to Probe Presence

The FS441X should provide minimal impact on the target if the guidelines in this document are adhered to. However, FuturePlus Systems does not guarantee that the probe will not affect system operation when placed in the circuit. With the FS441X installed a system may see a slight increase in BER and may activate receiver detect on unconnected links. (Receiver detect is a function in some serial standards such as PCI-Express.)

4.2.2 Routing Considerations Near/Through SRIOLAI Footprint

4.2.2.1 Surface Layer Routing (on same side as LAI)

Figure 10 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the same side of the board as the LAI.

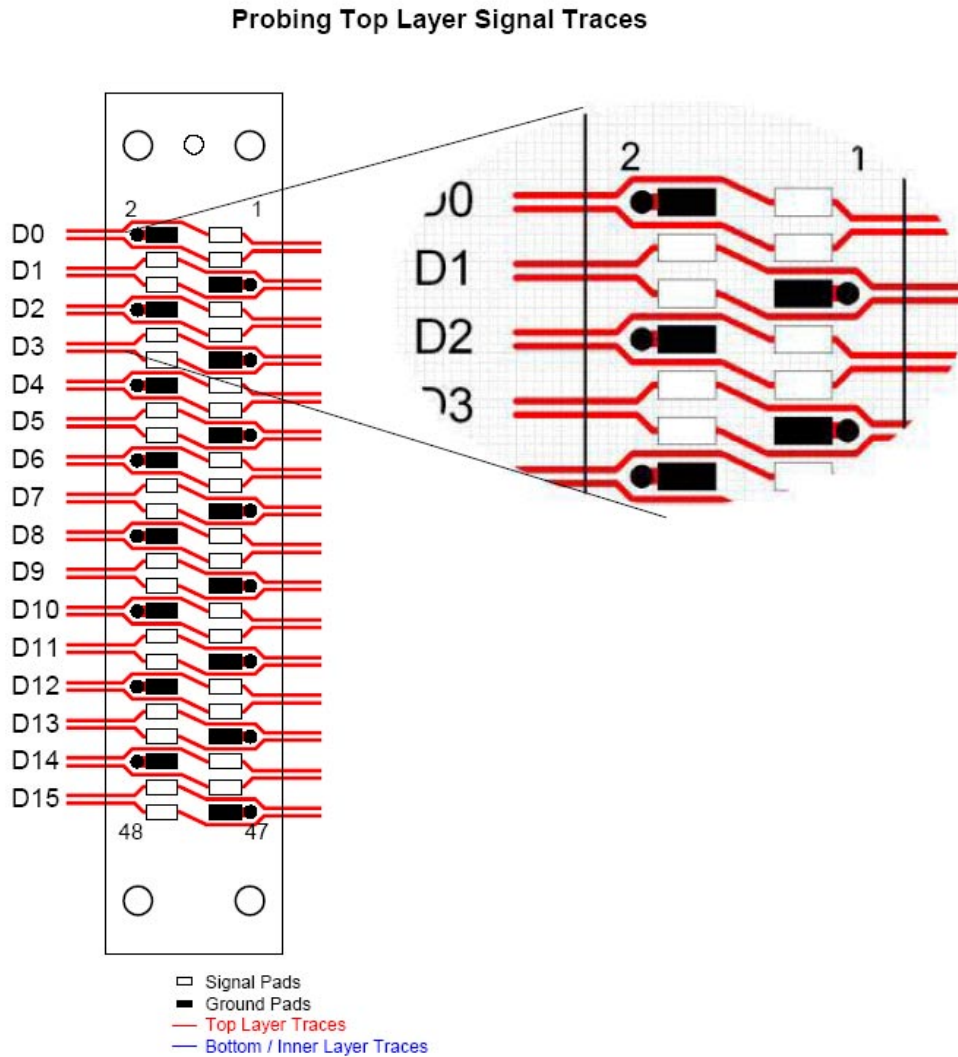


Figure 10-Suggested routing for microstrip traces on same layer as LAI

4.2.2.2 Inner layer and secondary side routing (surface layer opposite of LAI)

Figure 11 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the opposite side of board as LAI.

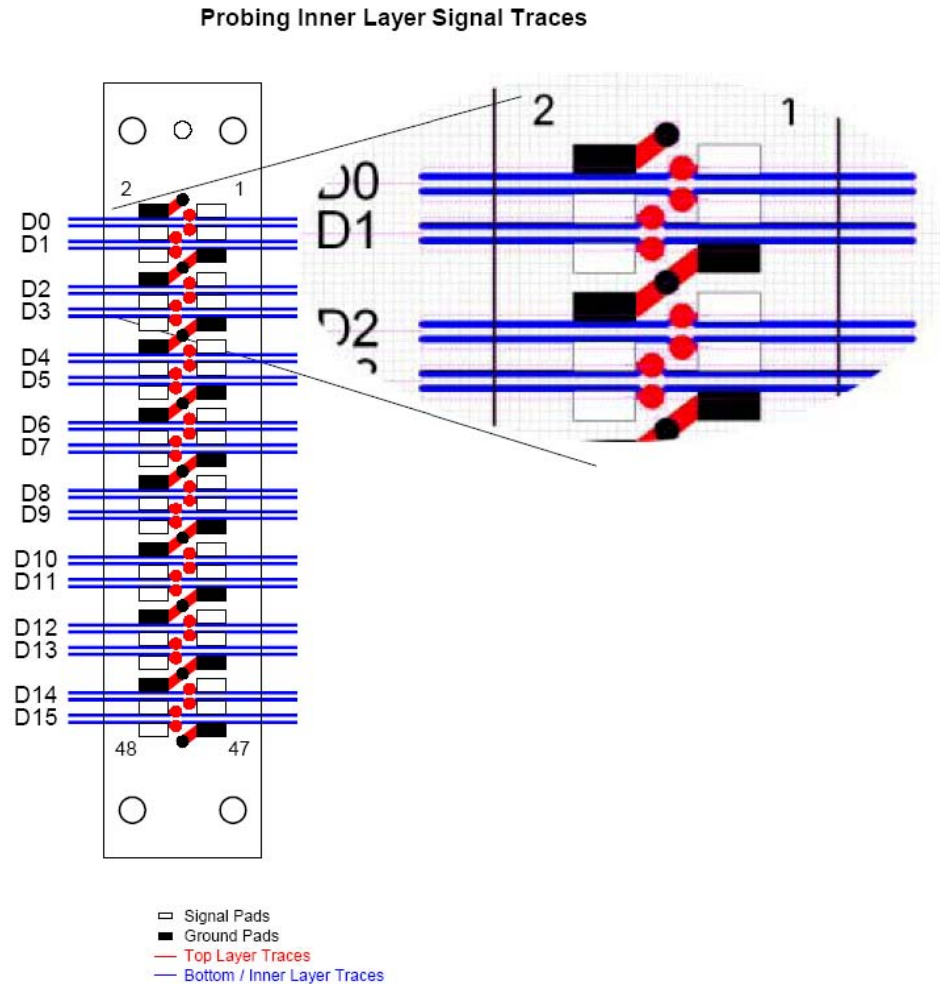


Figure 11-Suggested routing for stripline traces on inner layer and microstrip traces on the surface layer opposite of LAI

4.2.3 Load Models

4.2.3.1 FS441X Load Model

The load model for the midbus LAI is given in Figure 12. A Touchstone model is available from Samtec.

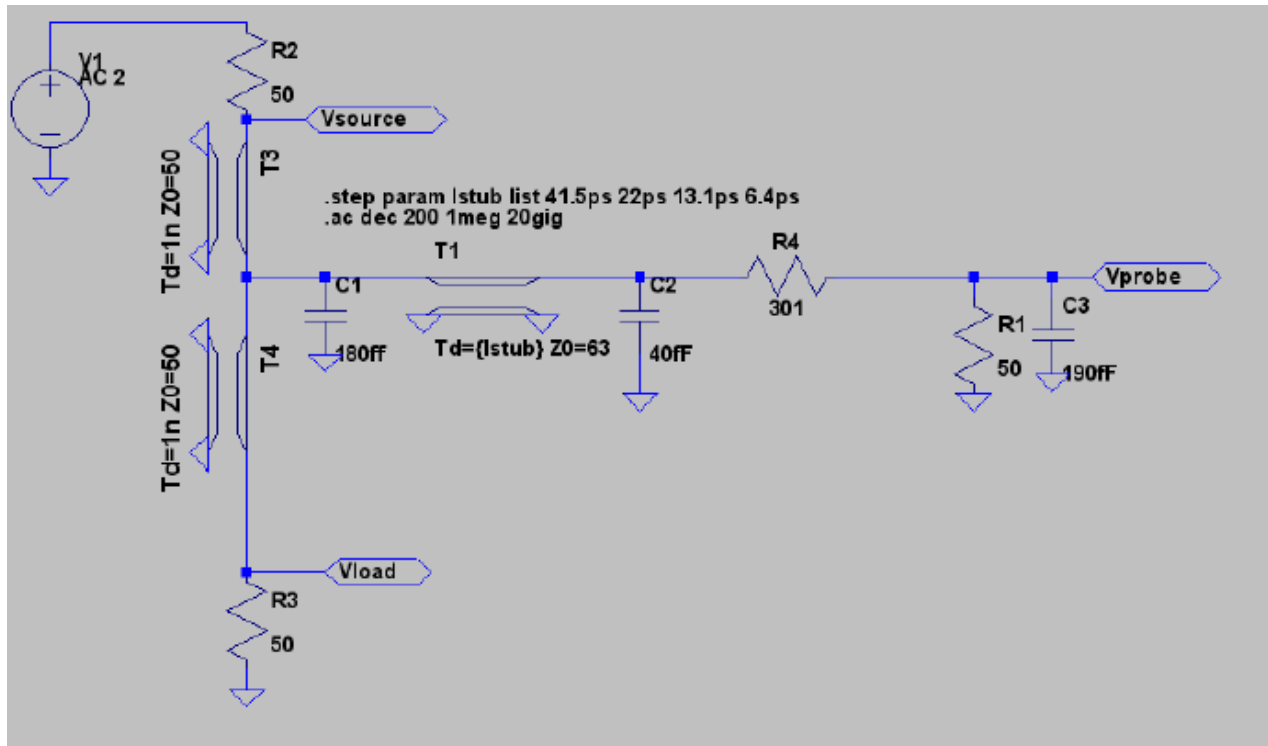


Figure 12-Load model for LAI

4.2.3.2 Load Model without LAI Installed

The model of the parasitic load on the system due to the LAI midbus footprint only (i.e. no LAI installed) is represented simply by a 0.2pF capacitor to ground. Note that if vias are associated with tapping the link for the LAI, those via parasitics would also need to be considered here in addition to the 0.2pF pad load.

4.2.4 SRIOLAI Pad Assignments

The mid-bus footprints (half and full sized) used for SRIO are the same industry standard footprints used for PCI Express.

Even though the locations of generic GND and Differential Signal pads are fixed (see table 5), there is much flexibility in the assignment of specific lanes to signal pads.

Flexibility in overall link arrangement on the footprint is provided partially by the variety of Mid-Bus Probe Cables available. The particular probe cable to use is selected based on the way PWB artwork design groups lanes of a link together on the pads of the footprint. See the charts on the following pages and in Appendix A.

Additional flexibility is provided by the probe. Some of the lane-to-pad assignment options can be varied by the user under Probe Manager control when the probe is run:

- Each lane may individually be inverted or not (p and n signals may be swapped).
- Each link may individually be lane-reversed or not.

- Where there are multiple links in a footprint, specific links may be selected.

4.2.4.1 – Full Size Midbus Pin Assignment

Table 5- General 16 Channel Pinout

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C _A p
4	C _B p	3	C _A n
6	C _B n	5	GND
8	GND	7	C _C p
10	C _D p	9	C _C n
12	C _D n	11	GND
14	GND	13	C _E p
16	C _F p	15	C _E n
18	C _F n	17	GND
20	GND	19	C _G p
22	C _H p	21	C _G n
24	C _H n	23	GND
26	GND	25	C _I p
28	C _J p	27	C _I n
30	C _J n	29	GND
32	GND	31	C _K p
34	C _L p	33	C _K n
36	C _L n	35	GND
38	GND	37	C _M p
40	C _N p	39	C _M n
42	C _N n	41	GND
44	GND	43	C _P p
46	C _Q p	45	C _P n
48	C _Q n	47	GND

Table 5 shows the generic location of probe points in the full sized footprint.

Channel= either direction A OR direction B differential pair for a given lane.

C<letter>= the designator for a Channel which accepts a given differential pair of signals

C<letter><p or n>= the two signals of the differential pair.

If interested in any arrangement not specified on the following pages, please contact FuturePlus Systems directly for possible support.

Table 6- x4 specific fullsize SRIO LAI Pinout (FS1031)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	7	C1p- Direction A 1
10	C1p- Direction B 1	9	C1n- Direction A 1
12	C1n- Direction B 1	11	GND
14	GND	13	C2p- Direction A 1
16	C2p- Direction B 1	15	C2n- Direction A 1
18	C2n- Direction B 1	17	GND
20	GND	19	C3p- Direction A 1
22	C3p- Direction B 1	21	C3n- Direction A 1
24	C3n- Direction B 1	23	GND
26	GND	25	C0p- Direction A 2
28	C0p- Direction B 2	27	C0n- Direction A 2
30	C0n- Direction B 2	29	GND
32	GND	31	C1p- Direction A 2
34	C1p- Direction B 2	33	C1n- Direction A 2
36	C1n- Direction B 2	35	GND
38	GND	37	C2p- Direction A 2
40	C2p- Direction B 2	39	C2n- Direction A 2
42	C2n- Direction B 2	41	GND
44	GND	43	C3p- Direction A 2
46	C3p- Direction B 2	45	C3n- Direction A 2
48	C3n- Direction B 2	47	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, channel 0 - direction A may be swapped in above table with channel 3 - direction A, channel 1 - direction A with channel 2 - direction A, etc.
3. Single link configuration also supported.
4. Only ONE of the above shaded configurations can be supported by a single FS441X. All pads for the unselected footprint must be present and will be connected to the inputs of the FS441X. All grounds shall be present.
5. For additional x4 probing options, see Appendix A.

Table 7- x1 specific SRIOLAI Pinout

(FS1031)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	1	C0p- Direction A 2
10	C0p- Direction B 2	3	C0n- Direction A 2
12	C0n- Direction B 2	5	GND
14	GND	1	C0p- Direction A 3
16	C0p- Direction B 3	3	C0n- Direction A 3
18	C0n- Direction B 3	5	GND
20	GND	1	C0p- Direction A 4
22	C0p- Direction B 4	3	C0n- Direction A 4
24	C0n- Direction B 4	5	GND
26	GND	25	C0p- Direction A 5
28	C0p- Direction B 5	27	C0n- Direction A 5
30	C0n- Direction B 5	29	GND
32	GND	1	C0p- Direction A 6
34	C0p- Direction B 6	3	C0n- Direction A 6
36	C0n- Direction B 6	5	GND
38	GND	1	C0p- Direction A 7
40	C0p- Direction B 7	3	C0n- Direction A 7
42	C0n- Direction B 7	5	GND
44	GND	1	C0p- Direction A 8
46	C0p- Direction B 8	3	C0n- Direction A 8
48	C0n- Direction B 8	5	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Single link configuration also supported.
3. Only ONE of the above shaded configurations can be supported by a single FS441X. All pads for the unselected footprint must be present and will be connected to the inputs of the FS441X. All grounds shall be present.
4. For additional x1 probing options see Appendix A.

4.2.4.2 Half Size Midbus Pin Assignment

Table 8- General 8 Channel Pinout

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND

Table 8 shows the generic location of probe points in the half sized footprint.

Channel= either direction A OR direction B differential pair for a given lane.

C<letter>= the designator for a Channel which accepts a given differential pair of signals

C<letter><p or n>= the two signals of the differential pair.

If interested in any arrangement not specified on the following pages, please contact FuturePlus Systems directly for possible support.

Table 9- x4 specific 8 Channel SRIO LAI Pinout (FS1032)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A
4	C0p- Direction B	3	C0n- Direction A
6	C0n- Direction B	5	GND
8	GND	7	C1p- Direction A
10	C1p- Direction B	9	C1n- Direction A
12	C1n- Direction B	11	GND
14	GND	13	C2p- Direction A
16	C2p- Direction B	15	C2n- Direction A
18	C2n- Direction B	17	GND
20	GND	19	C3p- Direction A
22	C3p- Direction B	21	C3n- Direction A
24	C3n- Direction B	23	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, channel 0 - direction A may be swapped in above table with channel 3 - direction A, channel 1-direction A with channel 2-direction A , etc.
3. Single link configuration also supported.
4. Currently there is no uni-directional (row-oriented versus column oriented) 4-lane pad arrangement for the half-sized footprint. Contact FuturePlus Systems if one is required.

Table 10 - x1 specific 8 Channel SRIO LAI Pinout (FS1032)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	1	C0p- Direction A 1
10	C0p- Direction B 1	3	C0n- Direction A 1
12	C0n- Direction B 1	5	GND
14	GND	1	C0p- Direction A 1
16	C0p- Direction B 1	3	C0n- Direction A 1
18	C0n- Direction B 1	5	GND
20	GND	1	C0p- Direction A 1
22	C0p- Direction B 1	3	C0n- Direction A 1
24	C0n- Direction B 1	5	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Single link configuration also supported.
3. Only ONE of the above shaded configurations can be supported by a single FS441X at a time (user-selectable). All pads for the selected footprint must be present and will be connected to the inputs of the FS441X. All grounds shall be present.

5.0 Appendix A – Supported Mid-bus footprint configurations

Key to the charts:

The FS441X can process two single-direction links, referred to as A and B.

A second FS441X can process two more single-direction links, referred to as C and D.

With the FS1039 or FS1038 cable and two FS441Xs, a total of 4 single-direction links may be probed in 1 footprint.

A	Link direction A
B	Link direction B

C	Link direction C in second FS44XX
D	Link direction D in second FS44XX

The mid-bus probe footprint is represented by a rectangular array, where each square is a differential signal probe point, and oriented so that pin 1 is on the left.

Half-Sized Mid-bus Probing options with FS1032 cable and one FS441X: (4-lane and 1-lane for sRIO)

4-lane links:

B	B	B	B
A	A	A	A

1-Lane Links:

B			
A			

	B		
	A		

		B	
		A	

			B
			A

Notes:

- The x4 link lane order may be: 0123 or 3210.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- These are referred to as bidirectional shapes.
- If interested in a uni-directional X4 shape (x4 link A packed into one end, and x4 link B packed into the other end), contact FuturePlus Systems directly.

**Full-Sized Mid-bus Probing options with FS1031 cable and one FS441X:
(4-lane and 1-lane for sRIO)**

4-Lane Links:

B	B	B	B				
A	A	A	A				

				B	B	B	B
				A	A	A	A

1-Lane Links:

B							
A							

				B			
				A			

	B						
	A						

					B		
					A		

		B					
		A					

						B	
						A	

			B				
			A				

							B
							A

Notes:

- The x4 link lane order may be: 0123 or 3210.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- These are referred to as bidirectional shapes.

Full-Sized Mid-bus Probing options with FS1038 cable and two FS441Xs:
(4-lane and 1-lane for sRIO)

4-Lane Links:

C	C	C	C	D	D	D	D
A	A	A	A	B	B	B	B

1-Lane Links:

C				D			
A				B			

	C				D		
	A				B		

		C				D	
		A				B	

			C				D
			A				B

	C				D		
A				B			

		C				D	
A				B			

			C				D
A				B			

C				D			
A				B			

		C				D	
A				B			

			C				D
A				B			

C				D			
	A				B		

	C				D		
	A				B		

			C				D
			A				B

C				D			
			A				B

	C				D		
			A				B

		C				D	
			A				B

Notes:

- The x4 link lane order may be: 0123 or 3210.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- Cable FS1038 has two instrument ends for use with two FS441Xs. It can be used with a single FS441X; the user will have a choice between the A/B link patterns shown above OR the C/D link patterns depending on which end is connected.

Full-Sized Mid-bus Probing options with FS1039 cable and two FS441Xs:
(4-lane and 1-lane for sRIO)

4-Lane Links:

A	A	B	B	C	C	D	D
A	A	B	B	C	C	D	D

1-Lane Links:

A		B		C		D	

A		B		C		D	

	A		B		C		D

	A		B		C		D

A		B					
				C		D	

A		B				C	D

A		B					
					C		D

				C		D	
A		B					

					C		D
A		B					

A		B			C		D

	A		B	C		D	

	A		B				
				C		D	

	A		B				
					C		D

				C		D	
A		B					

	A		B	C		D	

					C		D
A		B					

Notes:

- The x4 link lane order may be: 0 2 OR 3 1
1 3 2 0.
- The x4 pattern shown above is known as a “unidirectional” shape and has some advantages in PWB design of serial links.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- Cable FS1039 has two instrument ends for use with two FS441Xs. It can be used with a single FS441X; the user will have a choice between the A/B link patterns shown above OR the C/D link patterns depending on which end is connected.

6.0 Appendix B- SRIO Probing Design Review Checklist

The following tables serve as a guide to review a platform (schematics and layout) with regard to SRIO probing.

6.1 General Considerations

PASS	FAIL	NA	ISSUE
			Ideally, all SRIO links in the system should be observable with LA tools either using “mid-bus” probing
			If any SRIO links are not observable with LA tools (see previous item) then the design and validation team(s) should agree that this is acceptable.

6.2 Mid-bus Probing Configurations

PASS	FAIL	NA	ISSUE
			For each mid-bus footprint in the system, the number of links and sizes of those links within a footprint must meet the requirements of section 2.1 of the probing design guide.
			If the configuration of the links within a mid-bus footprint does not meet the requirements of the previous item, then this configuration must be confirmed with FuturePlus Systems.
			If a reference clock is required by the LAI then a connector for the reference clock must be provided for each SRIO reference clock domain.
			Reference clock is required if the link frequency is intentionally run outside of the standard +/-100ppm tolerance.
			Reference clock is required if the link frequency is intentionally run at other than the three nominal sRIO speed grades.
			For each reference clock provided to the LAI, is the clock properly terminated in the system?

6.3 Mechanical Considerations

6.3.1 Mid-bus Footprint(s)

PASS	FAIL	NA	ISSUE
			Verify that each mid-bus footprint matches the specifications in the probing design guide:
			<ul style="list-style-type: none">• Pad size, spacing, arrangement.
			<ul style="list-style-type: none">• Hole sizes, locations, tolerance, plating.
			<ul style="list-style-type: none">• Solder mask requirements.
			<ul style="list-style-type: none">• Pad plating requirements.
			<ul style="list-style-type: none">• Pin numbering.
			<ul style="list-style-type: none">• Component keepout requirements.
			Probe keepout requirements are met. This includes VERTICAL height.
			Verify that egress for probe cables is provided.

6.3.2 Reference Clock Header(s)

PASS	FAIL	NA	ISSUE
			Verify that each reference clock header matches the specifications in the probing design guide:
			<ul style="list-style-type: none"> Verify footprint against the Samtec specification for either the SMT header (FTR-103-02-S-S) or the through-hole header (TMS-103-02-S-S). Check pad and hole size, spacing, arrangement, etc.
			<ul style="list-style-type: none"> Verify pinout (pin 1 - REFCLKp, pin 2 - GND/NC, pin3 - REFCLKn or visa-versa)
			Reference clock probe keepout requirements are met.
			Verify that egress for reference clock probe cables is provided.

6.4 Electrical Considerations

6.4.1 Mid-bus Footprint(s):

PASS	FAIL	NA	ISSUE
			For each mid-bus footprint, have loss and jitter numbers at the LAI footprint pads been calculated and do they meet the requirements for the LAI tools?
			Have the constraints on AC coupling capacitor location for probing been met? (Each pair of capacitors may be placed on either side of the LAI footprint for each differential signal pair, but the location relationship can be varied for different differential pairs in the link.)
			For each link probed, system simulations must be performed with LAI load models included in order to verify that the system will work with LAI attached. Verify that the loss and jitter at the system receivers is within spec when the LAI load is installed.

			For each link probed using a mid-bus footprint, system simulations must be performed with the footprint model included in order to verify that the system will work with the footprint without the LAI attached
			Does system layout follow the guidelines on via and trace characteristics in the probing design guide?
			Does system layout follow the routing guidelines in the probing design guide? Are the differential pairs routed appropriately? (matched length, identical paths/vias, etc.)
			Verify pin assignment of the mid-bus footprint against the specifications in the probing design guide:
			<ul style="list-style-type: none"> All channels of a single direction of a link must connect to the same footprint.
			<ul style="list-style-type: none"> It is preferable (but not required) that both directions of a link connect to the same footprint.
			<ul style="list-style-type: none"> All unused signal pads on the LAI may be left unconnected but grounds must be connected
			<ul style="list-style-type: none"> Verify specific pinouts against tables in this probing design guide.

6.4.2 Reference Clock Header(s)

PASS	FAIL	NA	ISSUE
			Are LAI reference clock electrical requirements met?
			<ul style="list-style-type: none"> Differential Voltage
			<ul style="list-style-type: none"> Absolute Voltage
			<ul style="list-style-type: none"> Frequency
			Simulations of the reference clock network(s) must be performed using load models for the LAI reference clock probe to ensure good signal integrity to the LAI:
			<ul style="list-style-type: none"> Sims with load models look good?