PCI Express™ Logic Analyzer Probing Design Guide for the FS440x

FuturePlus® Systems Corporation
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1.0 Introduction

The FuturePlus® Systems flexible Serial Probe is a low-cost logic analyzer pre-processor capable of non-intrusively probing 8 channels of serial communication interfaces. Through the use of a flexible SERDES device and FPGA, it is able to receive and decode a variety of single and multi-lane protocols.

The FS440X is the PCI Express version of the product and supports serial data rates of 2.5 Gbps. Considerable flexibility allows various mid-bus probe lane arrangements (i.e. pad assignments) to be accommodated.

The probe is designed to handle two directions of a link, or a single direction from each of two unrelated links, using two link-processors (A and B), at lane widths of 1, 2, or 4; or a single direction at lane width of 8. The probe hardware and Protocol Decode software treat the two links individually. For analysis of interactions between two directions of a link, the logic analyzer inter-machine triggering function is used.

Users are expected to be familiar with the PCI Express™ specifications and to have performed electrical simulation to ensure proper signal quality.

1.1 Objectives

This document is intended to provide FuturePlus Systems customers with information needed for the integration of Logic Analyzer Probing for PCI Express™ into their designs. The solutions given here only concern a mid-bus probing solution in which the LAI footprint is designed into the target system. FuturePlus Systems also provides low intrusion interposer/extender cables to support slot connectors and ExpressCard™ on the PCI Express™ bus. Please refer to the FuturePlus Systems web site at www.FuturePlus.com for more information.

Although information concerning PCI Express™ topology and specifications will be given, this document is not intended to take the place of other PCI Express design documentation.

It is assumed that a design team utilizing this document for their design constraints will validate their designs through pre and post route electrical simulation and keepout volume analysis. To enable proper consideration of the numerous design parameters, a layout/schematic checklist has been developed and is included as an appendix in this document.

1.2 Nomenclature

LAI refers to the Analysis Probe, FS440X. A “channel” refers to either a transmit differential pair OR receive differential pair for a given lane. A link is the set of differential pairs that makes up one direction of the PCI Express implementation.

2.0 Overview and Configuration Support

2.1 Link Configuration Support

The FS440X provides support for the half size or full size mid-bus direct probing solution. Flexibility is given to the platform designer to configure a probing solution that best meets the needs of the system. With the FS440X the following configurations may be probed:

- Both directions of a link (i.e. up and downstream)
- A single direction of a link
- Single directions of 2 unrelated links

The FS440X supports the standard patterns of channel assignments to the pads of the PCI E Mid-Bus probe footprint. These are described in section 4.2.5. Additional unspecified patterns may also be supported. Contact FuturePlus Systems directly for more information.

2.2 Reference Clock(s) to the FS440X

The FS440X provides an internal reference clock generator that supports probe operation at the following link frequency and accuracy:

2.5 Gbps	Within 100 PPM, tighter than as required by the PCIe specification.

In most cases the FS440X requires an external reference clock connection when probing PCI-Express. It is required for any of the following conditions:

Link transmitter frequency accuracy is outside of 100 PPM.
Link transmitter frequency is other than 2.5 Gbps.
During spread spectrum operation.
During 10-bit mode probe operation.

When an external reference clock connection is required, the FS440X reference clock probe must be connected to a properly terminated, low jitter reference clock source on the target. The reference clock probe is a high-impedance type and may be connected anywhere a clean wave shape is available. Quality of the received clock can be verified by observing the buffered signal at the Ref Clock Out connector with an oscilloscope.

When external reference clock is used, if the target has only one reference clock for both directions (common clocking), the FS440X only needs one reference clock probe connected (Reference clock probe A). If the target has separate oscillators for both directions (distinct clocking), the FS440X would need both reference clock probes connected (Reference clock probes A and B). Distinct Clocking is only supported on the FS4400.

When using external reference clocks, the FS440X has flexibility in supporting reference clock multipliers. The default reference clock multiplier mode is:

25x reference clock frequency multiplier	Usable from 1.2 to 2.8 Gbps

If necessary, the FS440X can also support the following reference clock multiplier. Contact FuturePlus Systems for information on how to run the probe in this mode:

20x reference clock frequency multiplier	Usable from 1.2 to 2.8 Gbps

In the FS440X, the selection of reference clocking mode is always set the same for both directions (for both link processors A and B). These modes include internal versus external reference clock, internal reference clock speed, and external reference clock multiplier.

Note that this clock can be a dedicated clock. Alternately, the signals may be a tap off an existing clock, since the probes are designed to not significantly load the signals. In all cases, appropriate line terminations must be provided on the target. However, this needs to be verified by the system platform designers to verify proper functionality. At all times the FS440X must be presented with a reference clock that has a clean wave shape. See Reference Clock Model (Fig. 7) for more information.

3.0 Mechanical Design

This section contains mechanical design details (footprint dimensions, keepout volumes, and part numbers) of the midbus LAI and the reference clock pin header.

3.1 Midbus Logic Analyzer interface

The FuturePlus Systems FS440X utilizes the Samtec "Spirit" probing technology. This technology is applied in 2 different footprints.

3.1.1 Full size Footprint Dimensions and Specifications

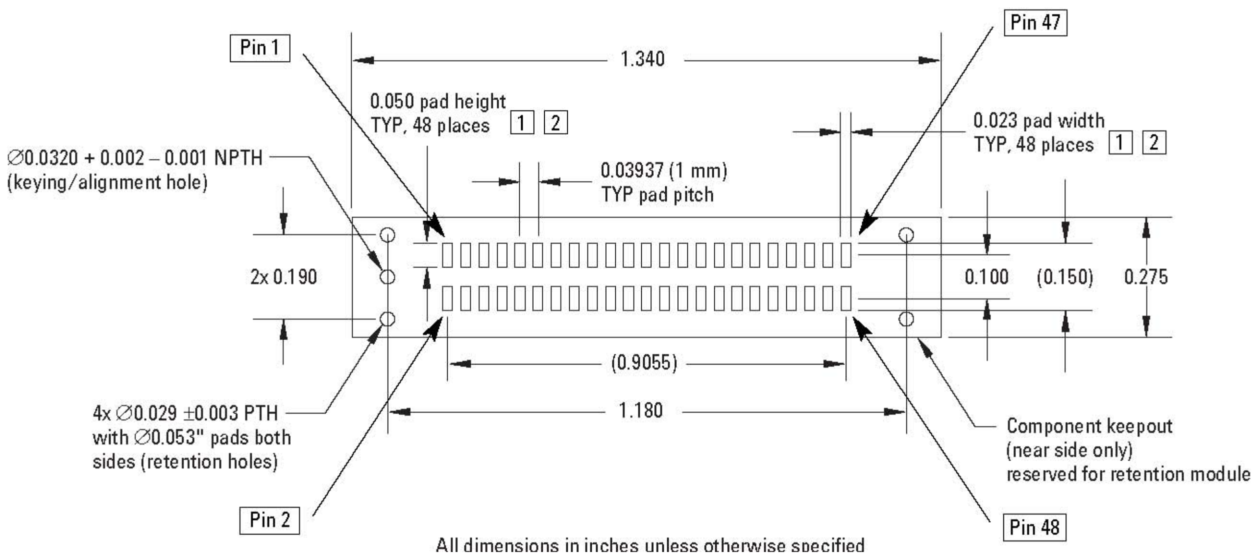

Figure 1 - PCI Express™ LAI industry standard full size footprint dimensions, pin numbering, and specification

3.1.2 ½ Size midbus Footprint Dimensions and Specifications

The following footprint (Fig. 2) is compatible with the FS440X product.

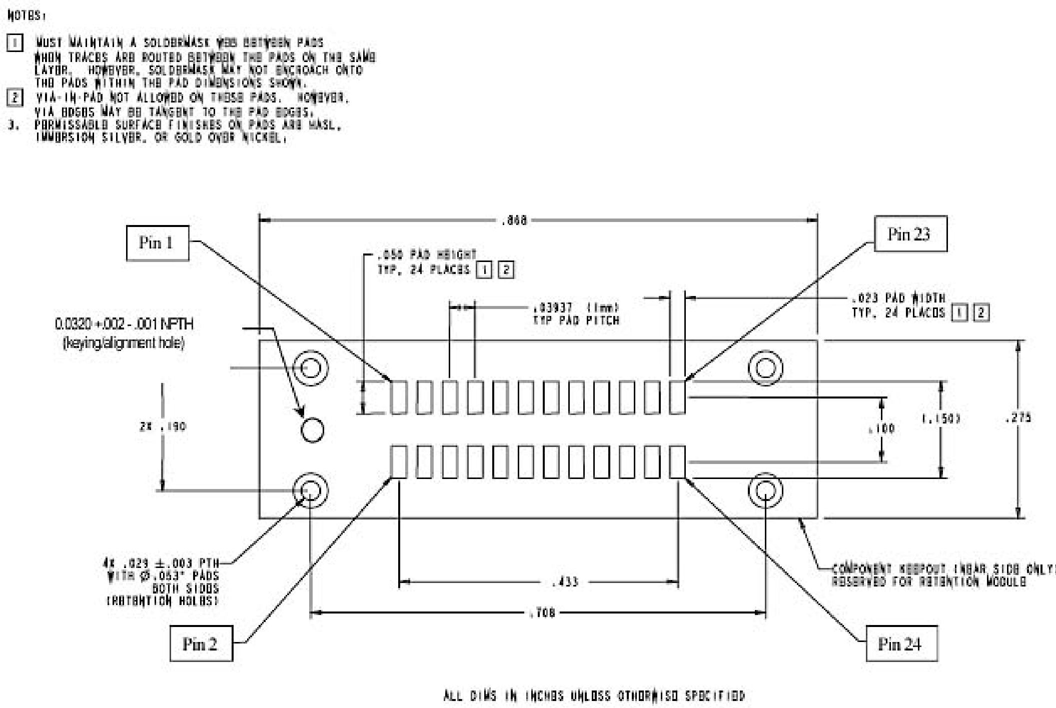

Figure 2 - PCI Express™ LAI industry standard half size footprint dimensions, pin numbering, and specification

3.1.3 Keepout Volume - Full Size Footprint

Keepout volume for the PCI Express™ full size footprint LAI is given in Figure 3.

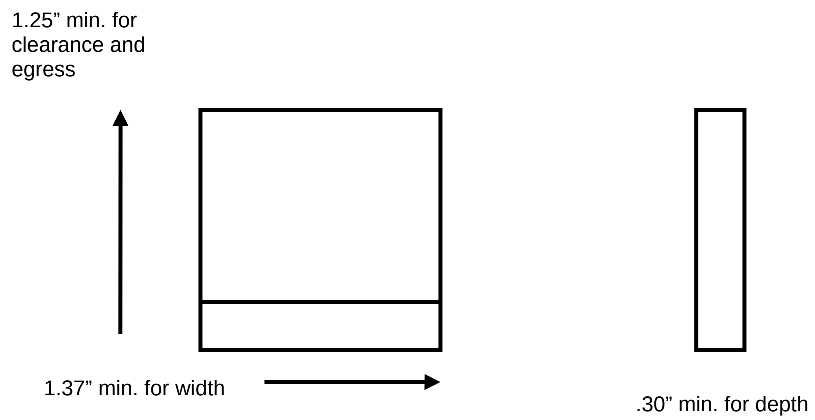

Figure 3- PCI Express™ Full size Footprint LAI Keepout Volume

3.1.4 Keepout Volume- Half Size footprint

Keepout volume for the PCI Express™ half size footprint LAI is given in Figure 4.

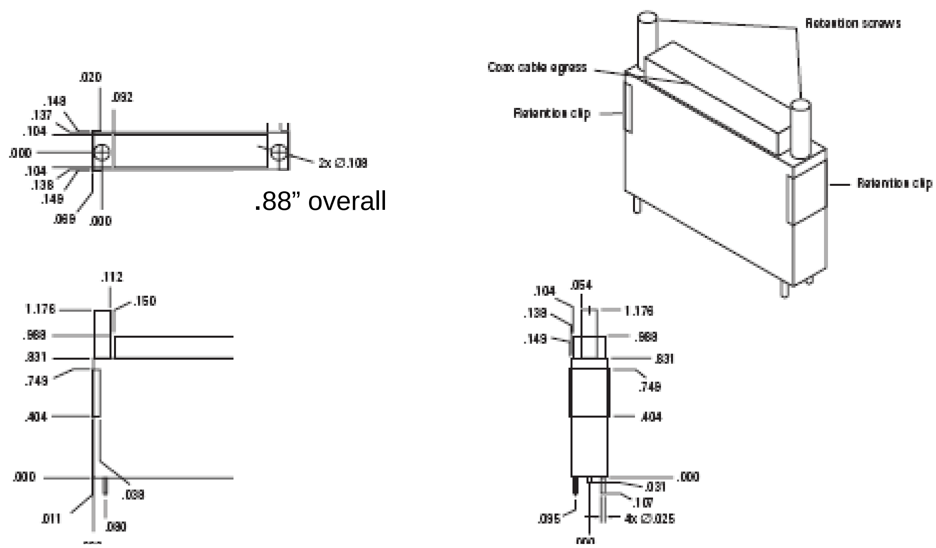

Figure 4- PCI Express™ half size Footprint LAI Keepout Volume

3.2 Reference Clock

3.2.1 Reference Clock Header

A 3-pin header (1 by 3, 0.050” center spacing) will provide the connection for the reference clock to the LAI. A small high impedance clock probe from the LAI will connect to this header and carry the REFCLKp and REFCLKn signals to the LAI. Note that an individual reference clock header is required for <u>each</u> PCI Express™ clock domain on the system.

The following are recommended part numbers for through-hole and surface mount versions of the 3-pin header for reference clock:

Through-hole: Samtec TMS-103-02-S-S or MilMax 850-10-003-10-001000
Surface mount: Samtec FTR-103-02-S or MilMax 850-10-003-30-001000

Table 1- Reference Clock header pinout

Signal	Pin Number
REFCLKp	1 (or 3) [1]
GND or N/C	2
REFCLKn	3 (or 1) [1]

Note: The LAI is not sensitive to the polarity of the reference clock. Therefore, the probe can be plugged onto the pin header in either orientation.

3.2.2 LAI Reference Clock Probe Keepout Volume

Keepout volumes for the reference clock probes are given in Figure 5. The pin headers reside symmetrically within the keepout volume on the target system.

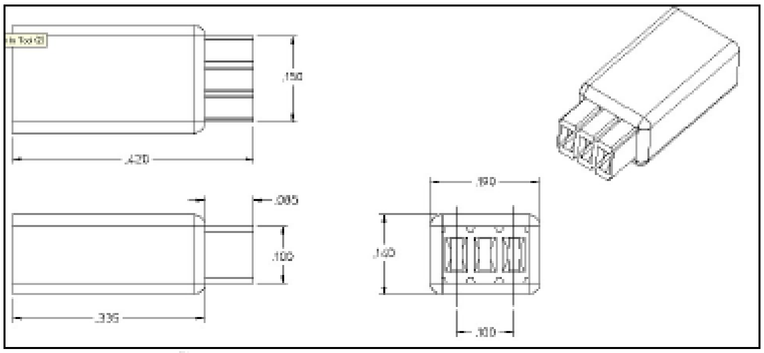

Figure 5- PCI Express™ Reference Clock Probe Keepout Volume

4.0 Electrical Design

This section contains electrical design details of the midbus LAI and the reference clock pin header. These details include LAI eye requirement definition, system impact due to LAI probe presence, LAI routing suggestions, load models, and pin assignments.

4.1 Reference Clock

4.1.1 LAI Reference Clock Electrical Requirements

In cases where a reference clock is used (see section 2.2) the following requirements must be met.

Table 2- LAI electrical requirements on the differential reference clock signals

LAI Requirement	Symbol	Min	Max	Comments
Differential Voltage at Ref Clock Attach Point	Vdiff	800 mVp-p	2V	

Table 3- Reference Clock Frequency

Reference Clock Multiplier	PCIe Data Rate Range	Reference Clock Frequency Range
25 X PCIe default	1.2 - 2.8 Gbps	48 - 112 MHz
20 X	1.2 - 2.8 Gbps	60 - 140 MHz

4.1.2 LAI Reference Clock Probe Load Model

Load models for the reference clock probe are given in this section. System designers will be expected to perform simulations of the reference clock networks with the header and LAI load models to ensure good signal integrity of the reference clocks at the header to the LAI. The pin header parasitics may be obtained from the connector vendor.

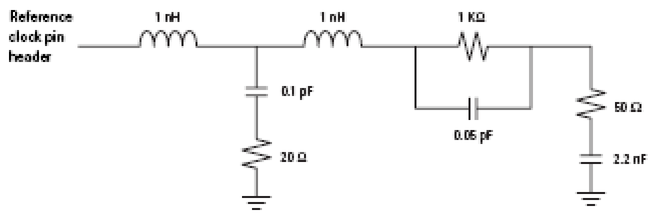

Figure 6- PCI Express™ Reference Clock Probe Load Model

4.2 Midbus LAI

Logical probing of the PCI Express™ bus is achieved through tapping a small amount of energy off the probed signals and channeling this energy to the logic analyzer. In order to avoid excessive loading conditions, the use of tip, or isolation, resistors is employed. These tip resistors are part of the LAI probing interface. These relatively high impedance tip resistors enable the logic analyzer to sample bus traffic without significantly loading the probed signals. A high-level block diagram of a generic PCI Express™ bus with a logic analyzer interface is given in Figure 7. Note that this would be repeated for each differential pair within a PCI Express™ link.

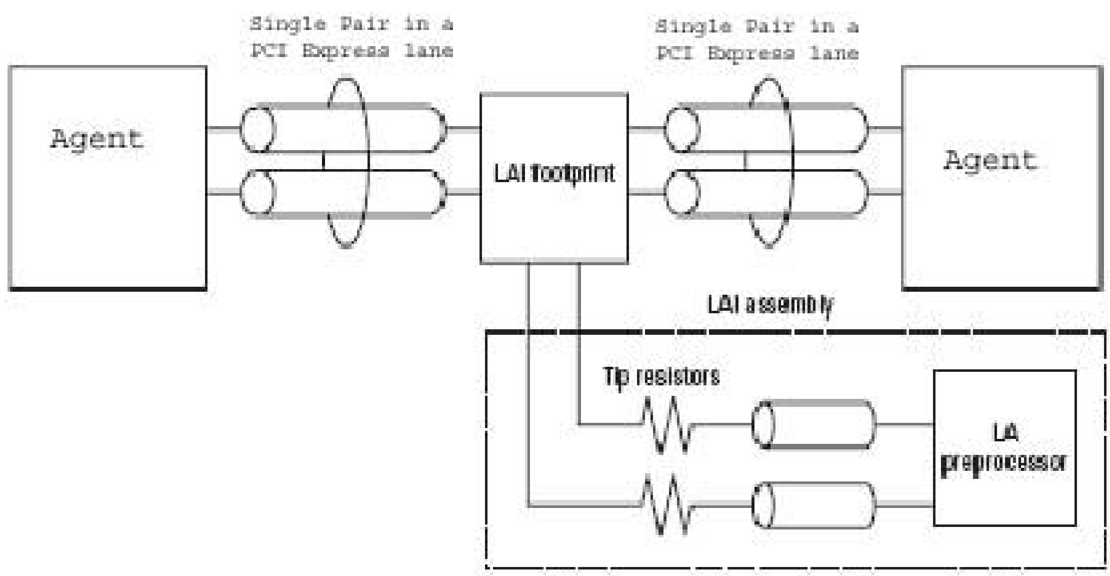

Figure 7- Block diagram example of a generic PCI Express™ bus with a LAI

In order for the LAI to reliably capture logical transactions on the bus, adequate signal eye must be made available to the LAI. It is incumbent upon the platform designers to ensure that sufficient signal eye is available to the LAI while the LAI load is in place so that proper signal tracing is enabled. This must be verified via electrical simulation utilizing the load model provided in Figure 11.

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are listed in Table 3 and described pictorially in Figure 8.

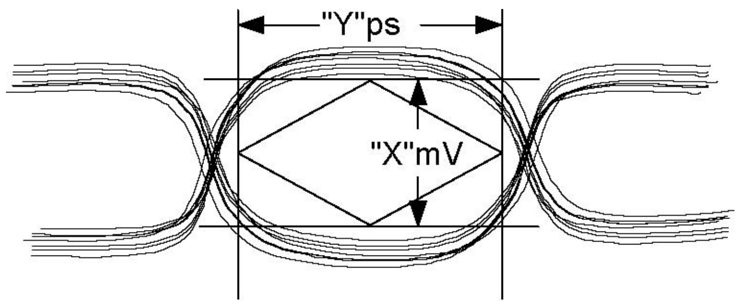

Figure 8-Example of eye specifications as seen at the LAI pad

Table 3 details the specific eye requirements for the FS440X.

Description	Specification for 2.5Gbps
Min Eye height at LAI pad [1]	175mV Vdiff p-p
Min Eye Width at LAI pad	.35 UI (Jitter tolerance of 0.65UI)
Length Matching Requirements-Differential Pair	+/-5mil [2]
Skew tolerated between lanes of a link	24 ns (60 bit times)

Table 3- PCI Express™ LAI Footprint Placement Interconnect Specification

Note:

1. Measured in differential units, e.g. Vdiff p-p = 2x single ended swing
2. Interconnect must length match within 5 mils from midbus probe pads to the nearest discontinuities in both directions, e.g. via, capacitor, driver or receiver. Matching within 5 mils on every segment of the PCIe trace is highly recommended. Segments are bounded by: drivers, receivers, capacitors, vias and mid bus probe pads.
3. The FS440X probe can be operated at 1.2 – 2.8Gbps. Operation above 2.5Gbps requires a minimum eye width of 140ps.

The eye characteristics given in Table 3 must be maintained for all probed links. Overall, these LAI placement specifications limit the electrical distance between the driver pin and the LAI attach point. Conceivably, probing both directions in lanes of a long PCI Express™ link may require two separate footprints and LAI assemblies, while probing both directions of relatively short links may be accomplished with one LAI. Regardless of implementation, refer to usage restrictions as listed in section 2 - Overview and Configuration Support. The same LAI eye requirements exist for all links substrates (e.g. FR4, cables, etc.)

4.2.2 Impact on PCI Express™ Channel due to Probe Presence

The FS440X should provide minimal impact on the target if the guidelines in this document are adhered to. However, FuturePlus Systems does not guarantee that the probe will not affect system operation when placed in the circuit. With the FS440X installed a system may see a slight increase in BER and may activate receiver detect on unconnected links.

4.2.3 Routing Considerations Near/Through PCI Express™ LAI Footprint

4.2.3.1 Surface Layer Routing (on same side as LAI)

Figure 10 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the same side of the board as the LAI.

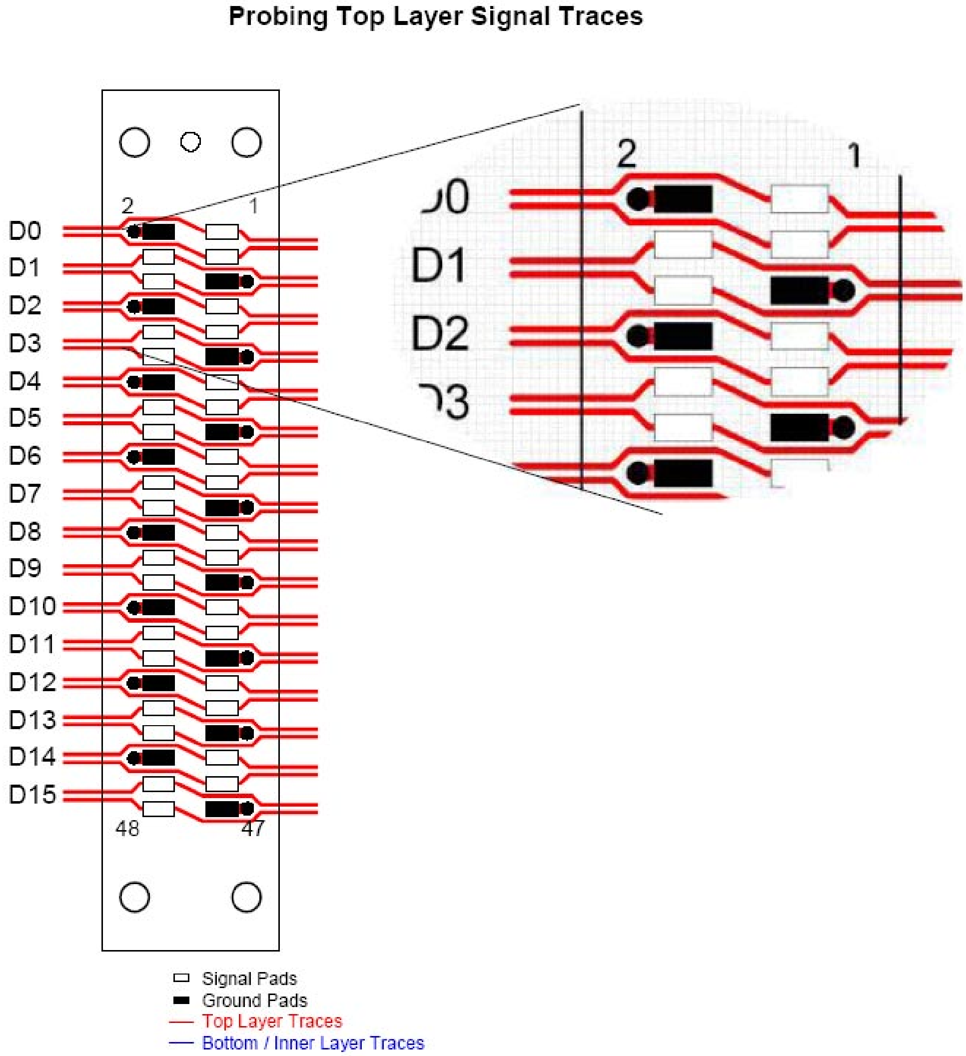

Figure 9-Suggested routing for microstrip traces on same layer as LAI

4.2.3.2 Inner layer and secondary side routing (surface layer opposite of LAI)

Figure 10 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the opposite side of board as LAI.

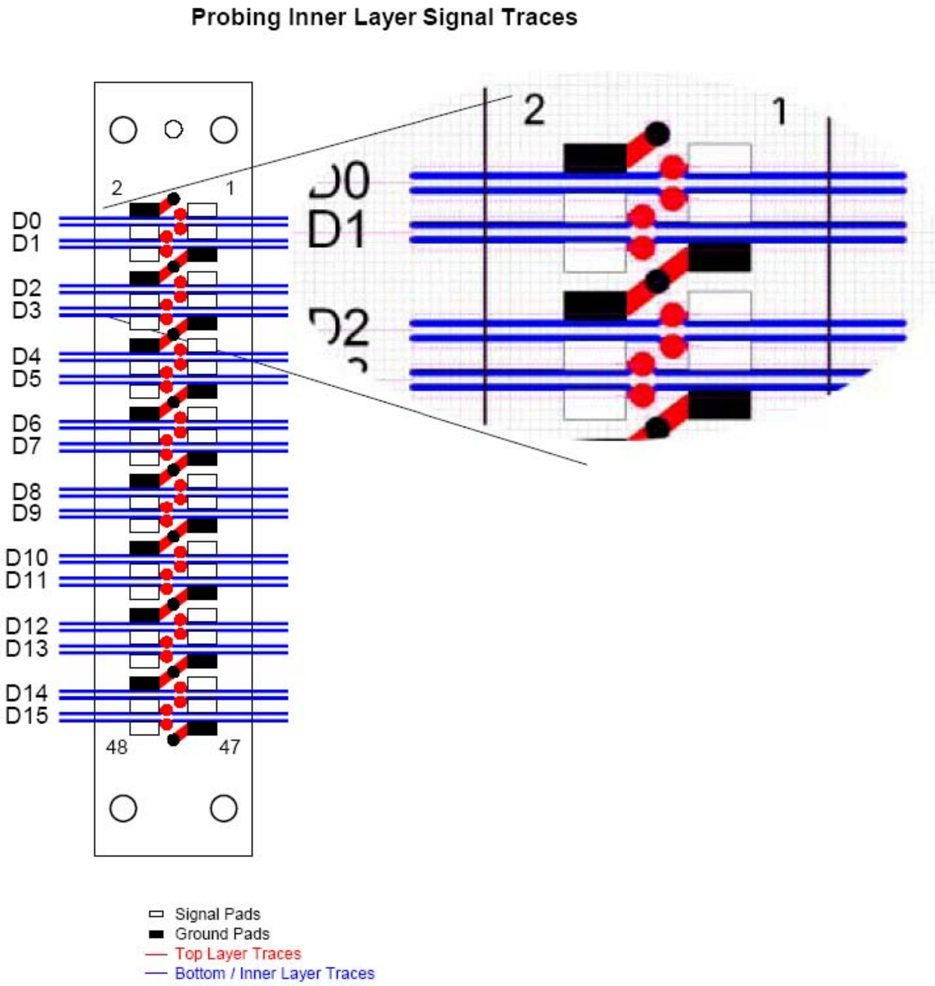

Figure 10-Suggested routing for stripline traces on inner layer and microstrip traces on surface layer opposite of LAI

4.2.4 Load Models

4.2.4.1 FS440X Load Model

The load model for the midbus LAI is given in Figure 11. A Touchstone file of this model is available from Samtec.

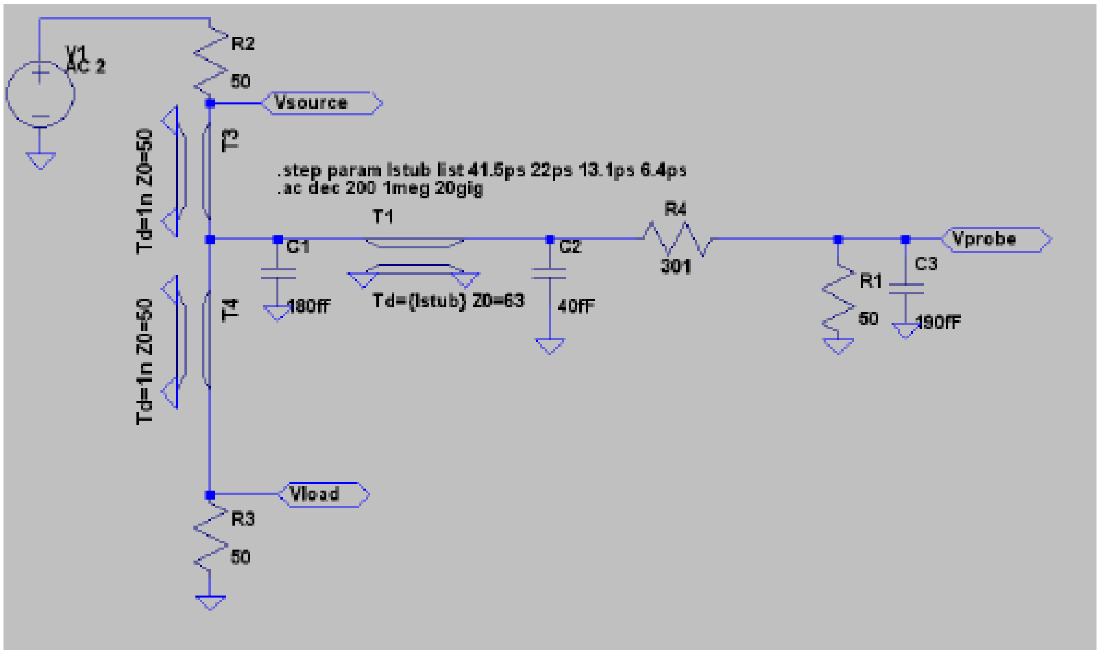

Figure 11-Load model for LAI

4.2.4.2 Load Model without LAI Installed

The model of the parasitic load on the system due to the LAI midbus footprint only (i.e. no LAI installed) is represented simply by a 0.2pF capacitor to ground. Note that if vias are associated with tapping the link for the LAI, those via parasitics would also need to be considered here in addition to the 0.2pF pad load.

4.2.5 PCI Express™ LAI Pad Assignments

The mid-bus footprints (half and fullsized) are industry standard footprints used for PCI Express probing.

Even though the locations of generic GND and Differential Signal pads are fixed (see table 4), there is much flexibility in the assignment of specific lanes to signal pads.

Flexibility in overall link arrangement on the footprint is provided partially by the variety of Mid-Bus Probe Cables available. The particular probe cable to use is selected based on the way PWB artwork design groups lanes of a link together on the pads of the footprint. See the charts on the following pages and in Appendix A.

Additional flexibility is provided by the probe. Some of the lane-to-pad assignment options can be varied by the user under Probe Manager control when the probe is run:

- Each lane may individually be inverted or not (p and n signals may be swapped).
- Each link may individually be lane-reversed or not.
- Where there are multiple links in a footprint, specific links may be selected.

4.2.5.1 – Full Size Midbus Pin Assignment

Table 4- General PCI Express™ 16 Channel Pinout

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND
26	GND	25	CIp
28	CJp	27	CIn
30	CJn	29	GND
32	GND	31	CKp
34	CLp	33	CKn
36	CLn	35	GND
38	GND	37	CMp
40	CNp	39	CMn
42	CNn	41	GND
44	GND	43	CPp
46	CQp	45	CPn
48	CQn	47	GND

Table 4 shows the generic location of probe points in the full sized footprint.

Channel= either direction A OR direction B differential pair for a given lane.
C<letter>= the designator for a Channel which accepts a given differential pair of signals
C<letter><p or n>= the two signals of the differential pair.

If interested in any arrangement not specified on the following pages, please contact FuturePlus Systems directly for possible support.

Table 5- x8 specific PCI Express™ LAI Pinout (FS1038)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	7	C1p- Direction A 1
10	C1p- Direction B 1	9	C1n- Direction A 1
12	C1n- Direction B 1	11	GND
14	GND	13	C2p- Direction A 1
16	C2p- Direction B 1	15	C2n- Direction A 1
18	C2n- Direction B 1	17	GND
20	GND	19	C3p- Direction A 1
22	C3p- Direction B 1	21	C3n- Direction A 1
24	C3n- Direction B 1	23	GND
26	GND	25	C4p- Direction A 1
28	C4p- Direction B 1	27	C4n- Direction A 1
30	C4n- Direction B 1	29	GND
32	GND	31	C5p- Direction A 1
34	C5p- Direction B 1	33	C5n- Direction A 1
36	C5n- Direction B 1	35	GND
38	GND	37	C6p- Direction A 1
40	C6p- Direction B 1	39	C6n- Direction A 1
42	C6n- Direction B 1	41	GND
44	GND	43	C7p- Direction A 1
46	C7p- Direction B 1	45	C7n- Direction A 1
48	C7n- Direction B 1	47	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, Direction B1 lanes 01234567 could become lanes 76543210..
3. Single link configuration also supported.
4. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user-selectable). All pads for the unselected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.
5. For additional x8 probing options, and additional uses for the FS1038 cable, see Appendix A.

Table 6 - x8 specific PCI Express™ LAI Pinout (FS1039)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C1p- Direction A 1	3	C0n- Direction A 1
6	C1n- Direction A 1	5	GND
8	GND	7	C2p- Direction A 1
10	C3p- Direction A 1	9	C2n- Direction A 1
12	C3n- Direction A 1	11	GND
14	GND	13	C4p- Direction A 1
16	C5p- Direction A 1	15	C4n- Direction A 1
18	C5n- Direction A 1	17	GND
20	GND	19	C6p- Direction A 1
22	C7p- Direction A 1	21	C6n- Direction A 1
24	C7n- Direction A 1	23	GND
26	GND	25	C0p- Direction B 1
28	C1p- Direction B 1	27	C0n- Direction B 1
30	C1n- Direction B 1	29	GND
32	GND	31	C2p- Direction B 1
34	C3p- Direction B 1	33	C2n- Direction B 1
36	C3n- Direction B 1	35	GND
38	GND	37	C4p- Direction B 1
40	C5p- Direction B 1	39	C4n- Direction B 1
42	C5n- Direction B 1	41	GND
44	GND	43	C6p- Direction B 1
46	C7p- Direction B 1	45	C6n- Direction B 1
48	C7n- Direction B 1	47	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, Direction A1 lanes 01234567 could become lanes 76543210..
3. Single link configuration also supported.
4. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user-selectable). All pads for the unselected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.
5. For additional x8 probing options, and additional uses for the FS1039 cable, see Appendix A.

Table 7 - x4 specific PCI Express™ LAI Pinout (FS1031)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	7	C1p- Direction A 1
10	C1p- Direction B 1	9	C1n- Direction A 1
12	C1n- Direction B 1	11	GND
14	GND	13	C2p- Direction A 1
16	C2p- Direction B 1	15	C2n- Direction A 1
18	C2n- Direction B 1	17	GND
20	GND	19	C3p- Direction A 1
22	C3p- Direction B 1	21	C3n- Direction A 1
24	C3n- Direction B 1	23	GND
26	GND	25	C0p- Direction A 2
28	C0p- Direction B 2	27	C0n- Direction A 2
30	C0n- Direction B 2	29	GND
32	GND	31	C1p- Direction A 2
34	C1p- Direction B 2	33	C1n- Direction A 2
36	C1n- Direction B 2	35	GND
38	GND	37	C2p- Direction A 2
40	C2p- Direction B 2	39	C2n- Direction A 2
42	C2n- Direction B 2	41	GND
44	GND	43	C3p- Direction A 2
46	C3p- Direction B 2	45	C3n- Direction A 2
48	C3n- Direction B 2	47	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, direction B1 lanes 0123 could become lanes 3210.
3. Single link configuration also supported.
4. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user selectable). All pads for the unselected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.
5. For additional x4 probing options, see Appendix A.

Table 8 - x2 specific PCI Express™ LAI Pinout (FS1031)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	7	C1p- Direction A 1
10	C1p-Direction B 1	9	C1n- Direction A 1
12	C1n- Direction B 1	11	GND
14	**GND**	**1**	**C0p- Direction A 2**
16	**C0p- Direction B 2**	**3**	**C0n- Direction A 2**
18	**C0n- Direction B 2**	**5**	**GND**
20	**GND**	**7**	**C1p- Direction A 2**
22	**C1p-Direction B 2**	**9**	**C1n- Direction A 2**
24	**C1n- Direction B 2**	**11**	**GND**
26	GND	25	C0p- Direction A 3
28	C0p- Direction B 3	27	C0n- Direction A 3
30	C0n- Direction B 3	29	GND
32	GND	31	C1p- Direction A 3
34	C1p-Direction B 3	33	C1n- Direction A 3
36	C1n- Direction B3	35	GND
38	**GND**	**1**	**C0p- Direction A 4**
40	**C0p- Direction B 4**	**3**	**C0n- Direction A 4**
42	**C0n- Direction B 4**	**5**	**GND**
44	**GND**	**7**	**C1p- Direction A 4**
46	**C1p-Direction B 4**	**9**	**C1n- Direction A 4**
48	**C1n- Direction B 4**	**11**	**GND**

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, channel 0 - direction A may be swapped in above table with channel 1 - direction A.
3. Single link configuration also supported.
4. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user-selectable). All pads for the unselected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.
5. For additional x2 probing options, see Appendix A.

Table 9 - x1 specific PCI Express™ LAI Pinout (FS1031)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	1	C0p- Direction A 2
10	C0p- Direction B 2	3	C0n- Direction A 2
12	C0n- Direction B 2	5	GND
14	GND	1	C0p- Direction A 3
16	C0p- Direction B 3	3	C0n- Direction A 3
18	C0n- Direction B 3	5	GND
20	GND	1	C0p- Direction A 4
22	C0p- Direction B 4	3	C0n- Direction A 4
24	C0n- Direction B 4	5	GND
26	GND	25	C0p- Direction A 5
28	C0p- Direction B 5	27	C0n- Direction A 5
30	C0n- Direction B 5	29	GND
32	GND	1	C0p- Direction A 6
34	C0p- Direction B 6	3	C0n- Direction A 6
36	C0n- Direction B 6	5	GND
38	GND	1	C0p- Direction A 7
40	C0p- Direction B 7	3	C0n- Direction A 7
42	C0n- Direction B 7	5	GND
44	GND	1	C0p- Direction A 8
46	C0p- Direction B 8	3	C0n- Direction A 8
48	C0n- Direction B 8	5	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Single link configuration also supported.
3. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user selectable). All pads for the unselected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.
4. For additional x1 probing options see Appendix A.

4.2.5.2. – Half Size Midbus Pin Assignment

Table 10 - General 8 Channel PCI Express Pinout

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND

Table 10 shows the generic location of probe points in the half sized footprint.

Channel= either direction A OR direction B differential pair for a given lane.
C<letter>= the designator for a Channel which accepts a given differential pair of signals
C<letter><p or n>= the two signals of the differential pair.

If interested in any arrangement not specified on the following pages, please contact FuturePlus Systems directly for possible support.

Table 11 - x8 specific 8 Channel PCI Express* LAI Pinout (FS1032)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A
4	C1p- Direction A	3	C0n- Direction A
6	C1n- Direction A	5	GND
8	GND	7	C2p- Direction A
10	C3p- Direction A	9	C2n- Direction A
12	C3n- Direction A	11	GND
14	GND	13	C4p- Direction A
16	C5p- Direction A	15	C4n- Direction A
18	C5n- Direction A	17	GND
20	GND	19	C6p- Direction A
22	C7p- Direction A	21	C6n- Direction A
24	C7n- Direction A	23	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI, in which case the lanes 01234567 become lanes 76543210.
3. For additional probing options, see Appendix A.

Table 12 - x4 specific 8 Channel PCI Express* LAI Pinout (FS1032)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A
4	C0p- Direction B	3	C0n- Direction A
6	C0n- Direction B	5	GND
8	GND	7	C1p- Direction A
10	C1p- Direction B	9	C1n- Direction A
12	C1n- Direction B	11	GND
14	GND	13	C2p- Direction A
16	C2p- Direction B	15	C2n- Direction A
18	C2n- Direction B	17	GND
20	GND	19	C3p- Direction A
22	C3p- Direction B	21	C3n- Direction A
24	C3n- Direction B	23	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI, in which case lanes 0123 become lanes 3210.
3. Single link configuration also supported.
4. Currently there is no uni-directional (row-oriented versus column oriented) 4-lane pad arrangement for the half-sized footprint. Contact FuturePlus Systems if one is required.

Table 13 - x2 specific 8 Channel PCI Express* LAI Pinout (FS1032)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	7	C1p- Direction A 1
10	C1p-Direction B 1	9	C1n- Direction A 1
12	C1n- Direction B 1	11	GND
14	GND	1	C0p- Direction A 1
16	C0p- Direction B 2	3	C0n- Direction A 1
18	C0n- Direction B 2	5	GND
20	GND	7	C1p- Direction A 1
22	C1p-Direction B 2	9	C1n- Direction A 1
24	C1n- Direction B 2	11	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Entire link assignment may be lane reversed in LAI. For example, channel 0 - direction A may be swapped in above table with channel 1 -direction A.
3. Single link configuration also supported.
4. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user selectable). All pads for the unselected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.
5. Currently there is no uni-directional (row-oriented versus column oriented) 2-lane pad arrangement for the half-sized footprint. Contact FuturePlus Systems if one is required.

Table 14 - x1 specific 8 Channel PCI Express* LAI Pinout (FS1032)

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Direction A 1
4	C0p- Direction B 1	3	C0n- Direction A 1
6	C0n- Direction B 1	5	GND
8	GND	1	C0p- Direction A 1
10	C0p- Direction B 1	3	C0n- Direction A 1
12	C0n- Direction B 1	5	GND
14	GND	1	C0p- Direction A 1
16	C0p- Direction B 1	3	C0n- Direction A 1
18	C0n- Direction B 1	5	GND
20	GND	1	C0p- Direction A 1
22	C0p- Direction B 1	3	C0n- Direction A 1
24	C0n- Direction B 1	5	GND

Notes:

1. Polarity (p and n) of any differential pair may be swapped
2. Single link configuration also supported.
3. Only ONE of the above shaded configurations can be supported by a single FS440X at a time (user-selectable). All pads for the selected footprint must be present and will be connected to the inputs of the FS440X. All grounds shall be present.

5.0 Appendix A – Supported Mid-bus footprint configurations

Key to the charts:
The FS440X can process two single-direction links, referred to as A and B.
A second FS440X can process two more single-direction links, referred to as C and D.
With the FS1039 or FS1038 cable and two FS440Xs, a total of 4 single-direction links may be probed in 1 footprint.

A	Link direction A
B	Link direction B

C	Link direction C in second FS44XX
D	Link direction D in second FS44XX

The mid-bus probe footprint is represented by a rectangular array, where each square is a differential signal probe point, and oriented so that pin 1 is on the left.

Half-Sized Mid-bus Probe capabilities with FS1032 cable and one FS44XX:

4-lane links:

B	B	B	B
A	A	A	A

8-lane links:

A	A	A	A
A	A	A	A

2-Lane Links:

B	B		
A	A		

		B	B
		A	A

1-Lane Links:

B			
A			

		B	
		A	

	B		
	A		

			B
			A

Notes:

- The x4 link lane order may be: 0123 or 3210.
- The x2 link lane order may be: 01 or 10.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- These are referred to as bidirectional shapes.
- If interested in a uni-directional X4 shape (x4 link A packed into one end, and x4 link B packed into the other end), contact FuturePlus Systems directly.
- The x8 link lane order may be: 0 2 4 6 OR 7 5 3 1 (uni-directional shape)
1 3 5 7 6 4 2 0.

Full-Sized Mid-bus Probe capabilities with FS1031 cable and one FS44XX:

4-Lane Links

B	B	B	B				
A	A	A	A				

				B	B	B	B
				A	A	A	A

2-Lane Links:

B	B						
A	A						

			B	B			
			A	A			

		B	B				
		A	A				

						B	B
						A	A

1-Lane Links:

B							
A							

				B			
				A			

	B						
	A						

					B		
					A		

		B					
		A					

						B	
						A	

			B				
			A				

							B
							A

Notes:

- The x4 link lane order may be: 0123 or 3210.
- The x2 link lane order may be: 01 or 10.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- These are referred to as bidirectional shapes.

Full-Sized Mid-bus Probe capabilities with FS1038 cable and one or two FS44XXs:

8-Lane Links:

C	C	C	C	C	C	C	C
A	A	A	A	A	A	A	A

4-Lane Links:

C	C	C	C	D	D	D	D
A	A	A	A	B	B	B	B

2-Lane Links:

C	C			D	D		
A	A			B	B		

		C	C			D	D
		A	A			B	B

		C	C			D	D
A	A			B	B		

C	C			D	D		
		A	A			B	B

1-Lane Links:

C				D			
A				B			

	C				D		
	A				B		

		C				D	
		A				B	

			C				D
			A				B

	C				D		
A				B			

		C				D	
A				B			

			C				D
A				B			

C				D			
	A				B		

		C				D	
	A				B		

			C				D
	A				B		

C				D			
		A				B	

	C				D		
		A				B	

			C				D
		A				B	

C				D			
			A				B

	C				D		
			A				B

		C				D	
			A				B

Full-Sized Mid-bus Probe capabilities with FS1038 cable and one or two FS44XXs, Continued:

Notes:

- The x8 Link lane order may be 01234567 or 76543210.
- The x4 Link lane order may be: 0123 or 3210.
- The x2 Link lane order may be 01 or 10.
- Links A and B are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- Cable FS1038 has two instrument ends for use with two FS44XXs, in which case all A, B, C, and D patterns shown may be probed.
- Cable FS1038 has two instrument ends and can be used with a single FS44XX; the user will have a choice between the A/B link patterns shown above OR the C/D link patterns depending on which end is connected.
- These pad arrangements are referred to as bi-directional shapes.

Full-Sized Mid-bus Probe capabilities with FS1039 cable and one or two FS44XXs:

8-Lane Links:

A	A	A	A	C	C	C	C
A	A	A	A	C	C	C	C

4-Lane Links:

A	A	B	B	C	C	D	D
A	A	B	B	C	C	D	D

2-Lane Links:

A		B		C		D	
A		B		C		D	

A		B			C		D
A		B			C		D

	A		B		C		D
	A		B		C		D

	A		B	C		D	
	A		B	C		D	

1-Lane Links:

A		B		C		D	

	A		B		C		D

A		B					
				C		D	

A		B					
					C		D

					C		D
A		B					

	A		B	C		D	

	A		B				
					C		D

	A		B	C		D	

A		B		C		D	

	A		B		C		D

A		B			C		D

				C		D	
A		B					

A		B			C		D

	A		B				
				C		D	

				C		D	
	A		B				

					C		D
	A		B				

Full-Sized Mid-bus Probe capabilities with FS1039 cable and one or two FS44XXs, Continued:

Notes:

- The x8 link lane order may be: 0 2 4 6 OR 7 5 3 1
1 3 5 7 6 4 2 0.
- The x4 link lane order may be: 0 2 OR 3 1
1 3 2 0.
- The x2 link lane order may be: 0 OR 1
1 0.
- Links A, B, C and D are each single direction and may or may not be related to each other.
- Any pair of links (for example, transmit and receive directions) may be displayed together on the Analyzer to observe responses and acknowledgements.
- Cable FS1039 has two instrument ends for use with two FS44XXs, in which case all A, B, C, and D patterns shown may be probed.
- Cable FS1039 has two instrument ends and can be used with a single FS44XX; the user will have a choice between the A/B link patterns shown above OR the C/D link patterns depending on which end is connected.
- These pad arrangements are referred to as uni-directional shapes and have some advantages in PWB design of serial links.

Note:

- Additional footprint pad arrangements may be possible, contact FuturePlus Systems directly for more information.

6.0 Appendix B- PCI Express™ Probing Design Review Checklist

The following tables serve as a guide to review a platform (schematics and layout) with regard to PCI Express™ probing.

6.1 General Considerations

PASS	FAIL	NA	ISSUE
			Ideally, all PCI Express links in the system should be observable with LA tools either using "mid-bus" probing or through an add-in card interposer.
			If any PCI Express™ links are not observable with LA tools (see previous item) then the design and validation team(s) should agree that this is acceptable.

6.2 Mid-bus Probing Configurations

PASS	FAIL	NA	ISSUE
			For each mid-bus footprint in the system, the number of links and sizes of those links within a footprint must meet the requirements of section 2.1 of the probing design guide.
			If the configuration of the links within a mid-bus footprint does not meet the requirements of the previous item, then this configuration must be confirmed with FuturePlus Systems.
			If a reference clock is required by the LAI then a connector for the reference clock must be provided for each PCI Express™ reference clock domain.
			Reference clock is required when spread spectrum clocking (SSC) is used.
			Reference clock is required if the link frequency is outside the range of 2.5Gbps +/- 100 ppm.
			For each reference clock provided to the LAI, is the clock properly terminated in the system?

6.3 Mechanical Considerations

6.3.1 Mid-bus Footprint(s)

PASS	FAIL	NA	ISSUE
			Verify that each mid-bus footprint matches the specifications in the probing design guide:
			• Pad size, spacing, arrangement.
			• Hole sizes, locations, tolerance, plating.
			• Solder mask requirements.
			• Pad plating requirements.
			• Pin numbering.
			• Component keepout requirements.
			Probe keepout requirements are met
			Verify that egress for probe cables is provided.

6.3.2 Reference Clock Header(s)

PASS	FAIL	NA	ISSUE
			Verify that each reference clock header matches the specifications in the probing design guide:
			• Verify footprint against the Samtec specification for either the SMT header (FTR-103-02-S-S) or the through-hole header (TMS-103-02-S-S). Check pad and hole size, spacing, arrangement, etc.
			• Verify pinout (pin 1 - REFCLKp, pin 2 - GND/NC, pin3 - REFCLKn or visa-versa
			Reference clock probe keepout requirements are met.
			Verify that egress for reference clock probe cables is provided.

6.4 Electrical Considerations

6.4.1 Mid-bus Footprint(s):

PASS	FAIL	NA	ISSUE
			For each mid-bus footprint, have loss and jitter numbers at the LAI footprint pads been calculated and do they meet the requirements for the LAI tools?
			Have the constraints on AC coupling capacitor location for probing been met? (Each pair of capacitors may be placed on either side of the LAI footprint for each differential signal pair, but the location relationship can be varied for different differential pairs in the link.)
			For each link probed, system simulations must be performed with LAI load models included in order to verify that the system will work with LAI attached. Verify that the loss and jitter at the system receivers is within spec when the LAI load is installed.

			For each link probed using a mid-bus footprint, system simulations must be performed with the footprint model included in order to verify that the system will work with the footprint without the LAI attached
			Does system layout follow the guidelines on via and trace characteristics in the probing design guide?
			Does system layout follow the routing guidelines in the probing design guide? Are the differential pairs routed appropriately? (matched length, identical paths/vias, etc.)
			Verify pin assignment of the mid-bus footprint against the specifications in the probing design guide:
			• All channels of a single direction of a link must connect to the same footprint.
			• It is preferable (but not required) that both directions of a link connect to the same footprint.
			• All unused pads on the LAI may be left unconnected.
			• Verify specific pinouts against tables in the probing design guide.

6.4.2 Reference Clock Header(s)

PASS	FAIL	NA	ISSUE
			Are LAI reference clock electrical requirements met?
			• Differential Voltage
			• Absolute Voltage
			• Frequency
			Simulations of the reference clock network(s) must be performed using load models for the LAI reference clock probe to ensure good signal integrity to the LAI:
			• Sims with load models look good?