FuturePlus® Systems

Application Note: Embedded DDR2 SDRAM Special Connection Solutions

FS1123 Embedded DDR2 SDRAM Analysis Software for 16700/16702
FS1124 Embedded DDR2 SDRAM Analysis Software for 16900/16902

Version 1.1
October 09, 2008

FuturePlus Systems
http://www.futureplus.com

Table of Contents

Section 1: DDR2 Logic Analysis Support

1.1 DESCRIPTION

This application note describes the methodology required to test a DDR2 SDRAM channel when a DIMM socket is not present. Placement of Samtec or Soft Touch connectors on the board under test is required. Included is a description of the design requirements for the test connection that will enable valid signal capture when using the Agilent Technologies 16700-Series and 16900-Series Logic Analysis Systems. This application note is specific to the Agilent 16700 series of logic analyzers when using the 1675X state/timing analysis modules, or the Agilent 16900 series of logic analyzers when using the 1675X, 16910/911 or 16950 state/timing analysis modules

FuturePlus Systems FS1123 and FS1124 embedded DDR2 SDRAM software provides logic analyzer configuration and transaction level decode of the DDR2 SDRAM memory bus traffic. The transaction decode software includes all data, commands and ECC signals.

The FS1123 and FS1124 User's Manual is an additional valuable reference that should be used in conjunction with this application note.

A thorough knowledge of electrical engineering and PCB design is assumed. While this application note provides guidelines and suggestions, it is not a comprehensive step-by-step design guide. These recommendations assume standard engineering and safety practices. Because each design is unique FuturePlus Systems assumes no liability or responsibility for damage to the system or device under test. This document is subject to change and/or revision without notice.

1.2 FUTUREPLUS® SYSTEMS

FuturePlus Systems designs and manufactures Bus Analysis Probes that are used in conjunction with Agilent Technologies logic analyzers. Bus Analysis Probes are powerful and versatile tools that provide a mechanical, electrical, and software interface between the bus and the logic analyzer. These analysis probes enable the engineer to view bus activity from basic timing waveforms to complete compliance verification. Our products provide measurement solutions for DDR2 SDRAM, PCI-X, USB 2.0, and many other buses.

FuturePlus Systems has been designing analysis probes since 1991. Our products are used worldwide by hundreds of different companies using standard industry buses in PC's, workstations and embedded processor systems. A bus analysis solution from FuturePlus Systems coupled with an Agilent Technologies logic analyzer is clearly the best development tool you can choose.

To learn more about these state of the art analysis tools, visit our website at www.futureplus.com, click on the Products button and select the computer bus of interest. Learn more about product features, specifications and ordering information. You will also find mechanical drawings, photographs of the product, downloadable software, and much more - all designed to help you choose the correct tool for your design.

FuturePlus Systems is proud to be a Premier Solutions Partner of Agilent Technologies' Value-Added Business Program.

1.3 ACKNOWLEDGEMENT

FuturePlus wishes to recognize and thank Perry Keller and Jennie Grosslight of Agilent Technologies for their work in helping to create this document. Without their hard work and technical expertise this document would not have been possible.

1.4 GLOSSARY OF TERMS

Terminology	*Description*
DDR	Double Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SUT	Signal Under Test
SMT	Surface Mount
PCB	Printed Circuit Board
LVTTL	Low Voltage TTL Logic
SSTL-18	Stub Series Terminated Logic (1.8 Volt)
Samtec™	Matched Impedance Connector (Used with termination adapter cables)
Soft Touch	Matched Impedance Connection System (Used with termination adapter cables)
FS1123	DDR2 SDRAM embedded software for 16700/02 (Agilent model number FSI-60093)
FS1124	DDR2 SDRAM embedded software for 16900/02 (Agilent model number FSI-60100)

Logic Analyzer Modules – "Module" – A set of logic analyzer card(s) that have been configured (via cables connecting multiple cards) to operate as a single logic analyzer whose total available channels is the sum of the channels on each card. A trigger within a module can be specified using all of the channels of that module. Each module may be further broken up into "Machines." A single module may not extend beyond a single 5 card 16700 or 16900 series mainframe.

Logic Analyzer Machines – "Machine" – A set of logic analyzer pods from a logic analyzer module grouped together to operate as a single state or timing analyzer. Each logic analyzer module may be partitioned into up to two independent "Machines" (either two state machines, or state and a timing machine), and the pods of a module may be assigned freely to either machine. Each state analyzer machine has its own state clock. Turbo mode (333 MHz for 16750-752, 450 MHz for 16910-911 or 600 MHz for 16753-756 and 16950 cards) operation restricts a module to having only one machine. Cross triggering between modules or machines is done via the Intermodule Bus or via the Flag bits, which will communicate across a 16700 frame and its expander, or a 16900 frame, or across multiple fames if the Multiframe product is used.

Logic Analyzer Requirements – Only 16750-16752, 16753-16756, 16910-16911 and 16950 modules are supported for the solutions described in this application note.

For more information regarding the 16700 and 16900 Logic Analyzers please refer to the Agilent web site at www.agilent.com/find/logicanalyzer .

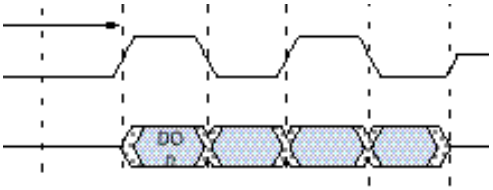
1.5 UNIQUE DDR2 PROBING CONSIDERATIONS

Refer to the FS1123 / FS1124 User's Manual.

DDR Timing Differences for Read or Write

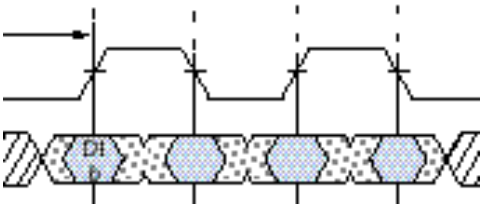
- Strobe edges straddle data for READ

Read



- Strobe edges centered on data for WRITE

Write



Section 2: Timing Analysis Operation

2.1 Select Termination Network and Route Connectors

Refer to Section 4 for optimal termination network requirements and specified logic analyzer probe adapters. Refer to Section 5 for Samtec and Soft Touch connector signal routing.

2.2 Logic analyzer modules and configurations

Refer to the FS1123 / FS1124 User's Manual.
Due to signal loading and signal speed considerations, we recommend the use of either the 16753/4/5/6 or 16950 logic analyzer modules for this application

2.3 Configuring the logic analyzer

Configuration of the logic analyzer can be performed by loading the appropriate FuturePlus FS1123 or FS1124 embedded DDR2 software or by manually configuring the Agilent logic analyzer. For specific details on using the logic analyzer, for example creating symbols or loading files, refer to the 16700 or 16900 Users Manual. For specific details on configuring the logic analyzer and installing the FS1123 or FS1124 software refer to the FS1123/FS1124 embedded DDR2 User's Manual.

2.4 Decoding DDR2 Commands

For specific details on interpreting the DDR2 software display in timing or state mode software refer to the FS1123 or FS1124 embedded DDR2 User's Manual.

2.5 Taking a Trace, Triggering, and Seeing Measurement Result

Timing analysis is the simplest setup, and there are no special factors involved in analyzer trigger setup, initiating a trace, and viewing results. For the Command bus you can use pre-defined symbols to specify mnemonically the command you wish to trigger on.

Section 3: State Analysis Operation

3.1 Select Connectors

Refer to Section 4 for logic analyzer probe adapters. Refer to Section 5 for Samtec and Soft Touch connection signal routing.

3.2 Logic Analyzer Modules and Configurations

Refer to Section 7, Table 7-1 for logic analyzer modules and configurations.

3.3 Logic Analyzer Operating System Requirements

State analysis of DDR2 with 16750 or higher cards requires version A.02.80.00 (or later) of the 16700 System Operating Software or A.02.50.00 (or later) of the 16900 System Operating Software. You can check to see if you already have the correct version by opening the "System Administration" dialog and selecting the "About" button. If you do not have the correct version then you must update your system software. Please consult the 16700 or 16900 system documentation for the SW update procedure. Version A.02.80.00 (or later) of the 16700 System Operating Software or A.02.50.00 (or later) of the 16900 System Operating Software or later is necessary to run dual sample for simultaneous read/write data capture in state mode.

3.4 State Clock Considerations - Probing a Differential Clock

Refer to the FS1123 / FS1124 User's Manual.

3.5 State Mode Trace Capture

Refer to the FS1123 / FS1124 User's Manual.

3.6 Eyescan

Digital designers are becoming increasingly aware of design problems associated with crosstalk, intersymbol interference, as well as clock and data jitter. A designer must understand the concept of a Data Eye when talking about high speed buses. It is important to consider not only the width of the data valid window, measured in time, but its height as well, measured in voltage. The Data Eye is the single measurement that captures both of these considerations. Finding and maintaining the size of the Eye is the principal challenge in designing and validating high speed busses.

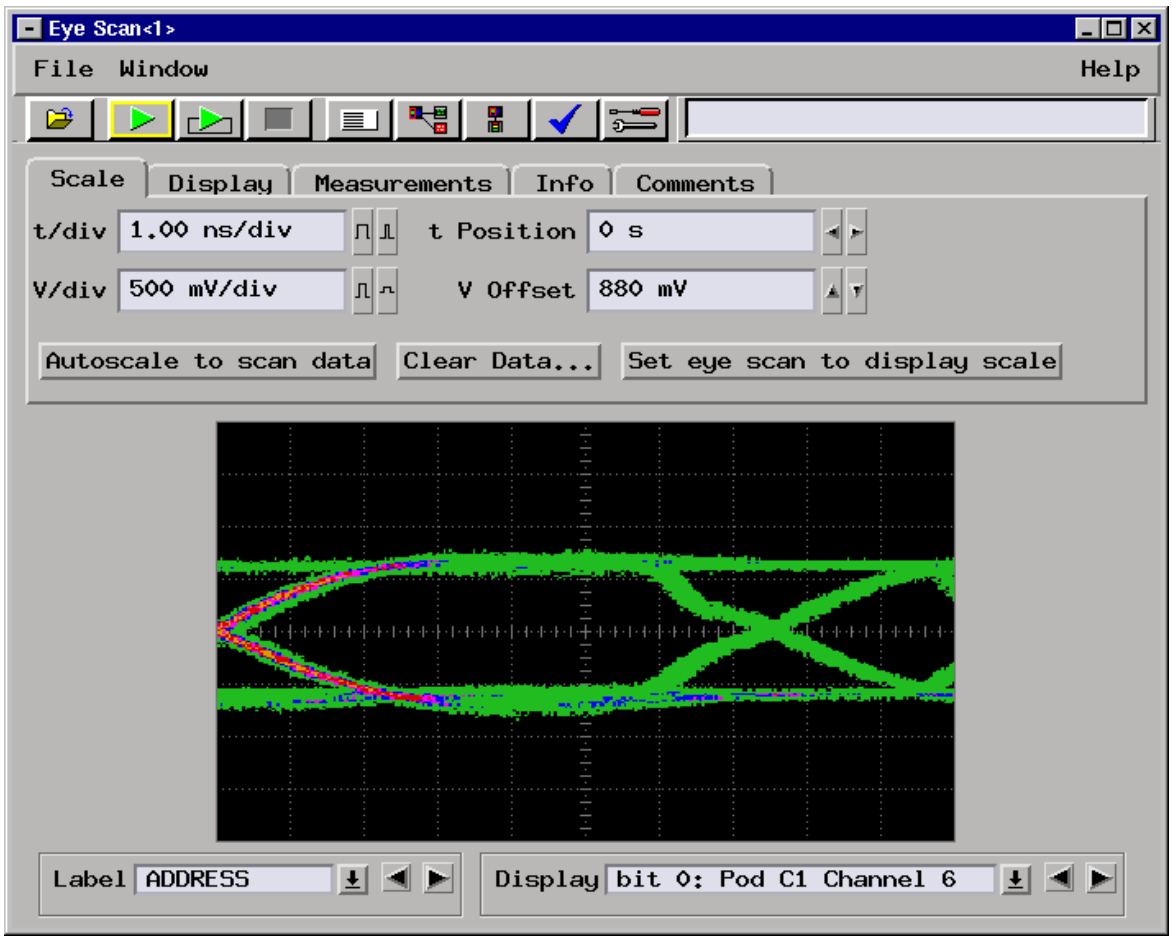
Measuring the Eye

If you put a scope in infinite persistence and let it run repetitively, you build up the familiar eye diagram. The name comes from the fact that it looks like an eye, but also through the eye you can see a lot about the performance characteristics of your circuit and how well it's meeting your signal integrity goals. However, using a scope on multiple signals of a high speed bus can take hours. Agilent has just introduced a new technology called "Eye Scan", which uses the 16700B / 16702B Logic Analysis System or "EyeFinder Pro" in the 16900A / 16902A Logic Analysis System to make the measurements. An Eye Scan of up to 169 signals can take as little as 5 minutes. A list of supported logic analysis modules can be found below.

Eye Scan Benefits

- Compare signal quality on many signals in minutes
- Archive measurements for later examination

- Quickly verify signal integrity during environmental testing
- Reduce project risk due to signal integrity issues
- Deliver a more reliable product in less time



Section 4: Termination

Termination networks are required when probing a digital signal. The termination network isolates the logic analyzer cabling and sensing circuitry from the signal under test and provides a high impedance, low capacitance load at the probe point.

When probing DDR2 without a DIMM socket it is recommended that an adapter cable with built-in termination networks be used.

Built-in termination networks are incorporated in the Agilent termination adapters. Using built-in termination networks requires the least board space. Designers will need to layout the Samtec or Soft Touch connectors and route the signals. Signal rise time and stub length to the connectors will determine the feasibility of using built-in terminations.

Additional information about probing with Agilent logic analyzers can be found at www.agilent.com/find/logicanalyzer.

4.1 Termination Adapter Cables with Built-in Termination Networks (E5378A / E5385A Samtec, E5390A / E5394A Soft Touch, E5404A / E5406A Soft Touch Pro)

The simplest technique for probing the DDR2 channel is to use Agilent termination adapters with the termination networks built into the cable tip. The Samtec connector, the E5385A (FuturePlus FS1015) is for use with 16750-16752 and 16910/911 logic analyzers and the E5378A (FuturePlus FS1014) is for use with 16753-16756 and 16950 logic analyzers.

If you choose to use the Soft Touch connector, the E5394A is for use with 16750-16752 and 16910-911 logic analyzers and the E5390A is for use with 16753-16756 and 16950 logic analyzers.

If you choose to use the Soft Touch Pro connector, the E5404A is for use with 16750-16752 and 16910-911 logic analyzers and the E5406AA is for use with 16753-16756 and 16950 logic analyzers.

Signals are routed on the PCB to the test connectors and terminated internally on the termination adapter connector. Connector placement is critical to minimize the stub length which will in turn minimize reflections on signals with fast rise times. However, even the best routing cannot eliminate the stubs completely since the path to the connector and the cable tip is a stub.

The general rule of thumb is to keep the stub length less than 1/5 the rise time of the signal under test (SUT). Refer to the following equations for deciding whether to use built in termination networks.

$l_{stub} <= 1/5 * t_{risetime} / u_{propspeed}$

$l_{stub} <= 1/5 * t_{risetime} / u_{propspeed} <= 1/5 * 1000ps / (150ps / in) <= 1.3”$ (1 ns rise time)

$l_{stub} <= 1/5 * t_{risetime} / u_{propspeed} <= 1/5 * 500ps / (150ps / in) <= 0.65”$ (500 ps rise time)

Whenever it is possible to route the signals within the previous constraints, use the built in termination networks. They are designed for the Agilent logic analysis systems and are compensated to provide flat frequency response between the signal under test and the logic analyzer input comparators.

SI modeling of the proposed circuit layout can provide a close estimation of the impact of the additional stubs added to the bus when designing in probe footprints. The Agilent documentation for the probes provides models that can be used in this effort.

4.2 ROUTING TECHNIQUES

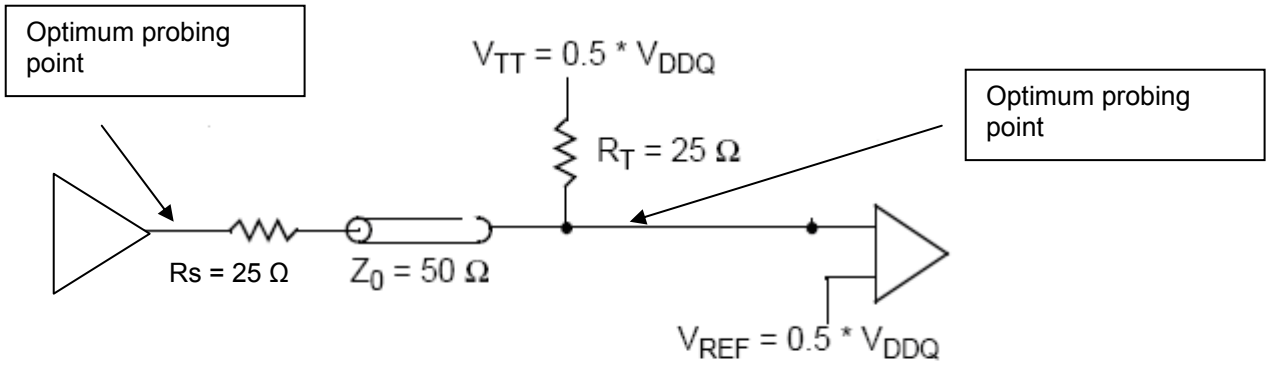
Regardless of whether discrete networks are used or not, the following describes some general guidelines for probing high-speed signals and busses.

4.2.1 SSTL-18

While SSTL-18 provides excellent high-speed signal fidelity during transmission across a PCB board, issues arise that do not normally occur with single-ended LVTTL logic.

The following diagram describes an SSTL-18 transmission line. Please be aware that this is a general example and there can be many different ways to implement an SSTL-18 transmission line for DDR2. This shows a series termination of 25 ohms close to the target driver and a parallel termination of 25 ohms to Vtt **close to the DRAM**. The trace impedance across the system is 50 ohms. This provides termination at both ends of the transmission line which is appropriate for bidirectional signals such as Data bits. Unidirectional signals, such as Address and Command, may only need termination at the receiving end of the transmission line.

In general, it is best to probe the signal at or very near the load termination resistors.



4.2.2 Probe Pinout Tables and Configuration Files

The following tables detail **suggested** DDR signal to probe pin routings. These are suggestions only, every embedded layout is different and the overriding concern for the designer should be stub length, routing complexity, and SI modeling results. The most important requirement is to insure at least one clock, a differential signal, is routed to a J clock input on the Master pod. It is also recommended that the designer bring a Chip Select signal to a clock input for qualification of Command activity. If Eyefinder or Eyescan of data activity is of interest, a Data strobe, generally a differential signal will be needed at a clock input.

The configuration files provided with this product are set-up per the following tables. If your target system is routed differently you just need to edit the configuration files and then save them. No config files changes will be required after that.

4.3 100 PIN SAMTEC CONNECTOR PINOUT

Use this section when 100 pin Samtec connectors are used to connect the SUT to the logic analyzer. The following table describes the pinout required for the 100 pin Samtec connector used with the E5378A and E5385A cables.

Publication # 5988-2989EN "Designing High Speed Digital Systems for Logic Analyzer Probing"
If the design does not use all signals listed in the pinout, e.g. less than 64 data bits on the target, then those pins on the connector should be grounded.

For mechanical and electrical considerations refer to Agilent publication #16760-97012 "Agilent Technologies Connector based Probes"

J1 - Command/Address

LA Odd input	Odd Side Pin	DDR Signal		LA Even input	Even Side Pin	DDR Signal
Gnd	1	Gnd		Gnd	2	Gnd
NC	3	NC		NC	4	NC
Gnd	5	Gnd		Gnd	6	Gnd
Odd D0	7	A0		Even D0	8	CKE
Gnd	9	Gnd		Gnd	10	Gnd
Odd D1	11	A1		Even D1	12	#WE
Gnd	13	Gnd		Gnd	14	Gnd
Odd D2	15	A2		Even D2	16	#CAS
Gnd	17	Gnd		Gnd	18	Gnd
Odd D3	19	A3		Even D3	20	#RAS
Gnd	21	Gnd		Gnd	22	Gnd
Odd D4	23	A4		Even D4	24	BA0
Gnd	25	Gnd		Gnd	26	Gnd
Odd D5	27	A5		Even D5	28	BA1
Gnd	29	Gnd		Gnd	30	Gnd
Odd D6	31	A6		Even D6	32	BA2
Gnd	33	Gnd		Gnd	34	Gnd
Odd D7	35	A7		Even D7	36	#S1
Gnd	37	Gnd		Gnd	38	Gnd
Odd D8	39	A8		Even D8	40	NC
Gnd	41	Gnd		Gnd	42	Gnd
Odd D9	43	A9		Even D9	44	NC
Gnd	45	Gnd		Gnd	46	Gnd
Odd D10	47	A10		Even D10	48	ODT0
Gnd	49	Gnd		Gnd	50	Gnd
Odd D11	51	A11		Even D11	52	ODT1
Gnd	53	Gnd		Gnd	54	Gnd
LA Odd input	**Odd Side Pin**	**DDR Signal**		**LA Even input**	**Even Side Pin**	**DDR Signal**
Odd D12	55	A12		Even D12	56	NC

Gnd	57	Gnd		Gnd	58	Gnd
Odd D13	59	A13		Even D13	60	NC
Gnd	61	Gnd		Gnd	62	Gnd
Odd D14	63	A14		Even D14	64	NC
Gnd	65	Gnd		Gnd	66	Gnd
Odd D15	67	A15		Even D15	68	NC
Gnd	69	Gnd		Gnd	70	Gnd
NC	71	NC		NC	72	NC
Gnd	73	Gnd		Gnd	74	Gnd
NC	75	NC		NC	76	NC
Gnd	77	Gnd		Gnd	78	Gnd
Odd D16P/CLKP	79	CK0		Even D16P/CLKP	80	#S0
Gnd	81	Gnd		Gnd	82	Gnd
Odd D16N/CLKN	83	CK0#		Even D16N/CLKN	84	Gnd
Gnd	85	Gnd		Gnd	86	Gnd
Odd Ext. Ref.	87	NC		Even Ext. Ref.	88	NC
Gnd	89	Gnd		Gnd	90	Gnd
NC	91	NC		NC	92	NC
Gnd	93	Gnd		Gnd	94	Gnd
Gnd	95	Gnd		Gnd	96	Gnd
+5V	97	NC		+5V	98	NC
+5V	99	NC		+5V	100	NC

J2 - Lower Data bits and strobes

LA Odd input	Odd Side Pin	DDR Signal		LA Even input	Even Side Pin	DDR Signal
Gnd	1	Gnd		Gnd	2	Gnd
NC	3	NC		NC	4	NC
Gnd	5	Gnd		Gnd	6	Gnd
Odd D0	7	DQ0		Even D0	8	DQ13
Gnd	9	Gnd		Gnd	10	Gnd
Odd D1	11	DQ1		Even D1	12	DQ14
Gnd	13	Gnd		Gnd	14	Gnd
Odd D2	15	DQ2		Even D2	16	DQ15
Gnd	17	Gnd		Gnd	18	Gnd
Odd D3	19	DQ3		Even D3	20	DQS3
LA Odd input	**Odd Side Pin**	**DDR Signal**		**LA Even input**	**Even Side Pin**	**DDR Signal**
Gnd	21	Gnd		Gnd	22	Gnd
Odd D4	23	DQS0		Even D4	24	DQ16
Gnd	25	Gnd		Gnd	26	Gnd
Odd D5	27	DQ4		Even D5	28	DQ17

Gnd	29	Gnd		Gnd	30	Gnd
Odd D6	31	DQ5		Even D6	32	DQ18
Gnd	33	Gnd		Gnd	34	Gnd
Odd D7	35	DQ6		Even D7	36	DQ19
Gnd	37	Gnd		Gnd	38	Gnd
Odd D8	39	DQ7		Even D8	40	DQS4
Gnd	41	Gnd		Gnd	42	Gnd
Odd D9	43	DQS1		Even D9	44	DQ20
Gnd	45	Gnd		Gnd	46	Gnd
Odd D10	47	DQ8		Even D10	48	DQ21
Gnd	49	Gnd		Gnd	50	Gnd
Odd D11	51	DQ9		Even D11	52	DQ22
Gnd	53	Gnd		Gnd	54	Gnd
Odd D12	55	DQ10		Even D12	56	DQ23
Gnd	57	Gnd		Gnd	58	Gnd
Odd D13	59	DQ11		Even D13	60	DQS5
Gnd	61	Gnd		Gnd	62	Gnd
Odd D14	63	DQS2		Even D14	64	DQ24
Gnd	65	Gnd		Gnd	66	Gnd
Odd D15	67	DQ12		Even D15	68	DQ25
Gnd	69	Gnd		Gnd	70	Gnd
NC	71	NC		NC	72	NC
Gnd	73	Gnd		Gnd	74	Gnd
NC	75	NC		NC	76	NC
Gnd	77	Gnd		Gnd	78	Gnd
Odd D16P/CLKP	79	DQS0		Even D16P/CLKP	80	NC
Gnd	81	Gnd		Gnd	82	Gnd
Odd D16N/CLKN	83	#DQS0		Even D16N/CLKN	84	Gnd
Gnd	85	Gnd		Gnd	86	Gnd
Odd Ext. Ref.	87	NC		Even Ext. Ref.	88	NC
Gnd	89	Gnd		Gnd	90	Gnd
NC	91	NC		NC	92	NC
Gnd	93	Gnd		Gnd	94	Gnd
Gnd	95	Gnd		Gnd	96	Gnd
+5V	97	NC		+5V	98	NC
+5V	99	NC		+5V	100	NC

J3 Middle Data and strobes

LA Odd input	Odd Side Pin	DDR Signal		LA Even input	Even Side Pin	DDR Signal
Gnd	1	Gnd		Gnd	2	Gnd
NC	3	NC		NC	4	NC
Gnd	5	Gnd		Gnd	6	Gnd

Odd D0	7	DQ26		Even D0	8	DQ39
Gnd	9	Gnd		Gnd	10	Gnd
Odd D1	11	DQ27		Even D1	12	DQS9
Gnd	13	Gnd		Gnd	14	Gnd
Odd D2	15	DQS6		Even D2	16	DQ40
Gnd	17	Gnd		Gnd	18	Gnd
Odd D3	19	DQ28		Even D3	20	DQ41
Gnd	21	Gnd		Gnd	22	Gnd
Odd D4	23	DQ29		Even D4	24	DQ42
Gnd	25	Gnd		Gnd	26	Gnd
Odd D5	27	DQ30		Even D5	28	DQ43
Gnd	29	Gnd		Gnd	30	Gnd
Odd D6	31	DQ31		Even D6	32	DQS10
Gnd	33	Gnd		Gnd	34	Gnd
Odd D7	35	DQS7		Even D7	36	DQ44
Gnd	37	Gnd		Gnd	38	Gnd
Odd D8	39	DQ32		Even D8	40	DQ45
Gnd	41	Gnd		Gnd	42	Gnd
Odd D9	43	DQ33		Even D9	44	DQ46
Gnd	45	Gnd		Gnd	46	Gnd
Odd D10	47	DQ34		Even D10	48	DQ47
Gnd	49	Gnd		Gnd	50	Gnd
Odd D11	51	DQ35		Even D11	52	DQS11
Gnd	53	Gnd		Gnd	54	Gnd
Odd D12	55	DQS8		Even D12	56	DQ48
Gnd	57	Gnd		Gnd	58	Gnd
Odd D13	59	DQ36		Even D13	60	DQ49
Gnd	61	Gnd		Gnd	62	Gnd
Odd D14	63	DQ37		Even D14	64	DQ50
Gnd	65	Gnd		Gnd	66	Gnd
Odd D15	67	DQ38		Even D15	68	DQ51
Gnd	69	Gnd		Gnd	70	Gnd
NC	71	NC		NC	72	NC
Gnd	73	Gnd		Gnd	74	Gnd
NC	75	NC		NC	76	NC
LA Odd input	**Odd Side Pin**	**DDR Signal**		**LA Even input**	**Even Side Pin**	**DDR Signal**
Gnd	77	Gnd		Gnd	78	Gnd
Odd D16P/CLKP	79	TEST		Even D16P/CLKP	80	CK2
Gnd	81	Gnd		Gnd	82	Gnd
Odd D16N/CLKN	83	GND		Even D16N/CLKN	84	#CK2
Gnd	85	Gnd		Gnd	86	Gnd
Odd Ext. Ref.	87	NC		Even Ext. Ref.	88	NC
Gnd	89	Gnd		Gnd	90	Gnd

NC	91	NC		NC	92	NC
Gnd	93	Gnd		Gnd	94	Gnd
Gnd	95	Gnd		Gnd	96	Gnd
+5V	97	NC		+5V	98	NC
+5V	99	NC		+5V	100	NC

J4 Upper Data and strobes

LA Odd input	Odd Side Pin	DDR Signal		LA Even input	Even Side Pin	DDR Signal
Gnd	1	Gnd		Gnd	2	Gnd
NC	3	NC		NC	4	NC
Gnd	5	Gnd		Gnd	6	Gnd
Odd D0	7	DQS12		Even D0	8	DQS16
Gnd	9	Gnd		Gnd	10	Gnd
Odd D1	11	DQ52		Even D1	12	DQS17
Gnd	13	Gnd		Gnd	14	Gnd
Odd D2	15	DQ53		Even D2	16	CB0
Gnd	17	Gnd		Gnd	18	Gnd
Odd D3	19	DQ54		Even D3	20	CB1
Gnd	21	Gnd		Gnd	22	Gnd
Odd D4	23	DQ55		Even D4	24	CB2
Gnd	25	Gnd		Gnd	26	Gnd
Odd D5	27	DQS13		Even D5	28	CB3
Gnd	29	Gnd		Gnd	30	Gnd
Odd D6	31	DQ56		Even D6	32	CB4
Gnd	33	Gnd		Gnd	34	Gnd
Odd D7	35	DQ57		Even D7	36	CB5
Gnd	37	Gnd		Gnd	38	Gnd
Odd D8	39	DQ58		Even D8	40	CB6
Gnd	41	Gnd		Gnd	42	Gnd
Odd D9	43	DQ59		Even D9	44	CB7
LA Odd input	**Odd Side Pin**	**DDR Signal**		**LA Even input**	**Even Side Pin**	**DDR Signal**
Gnd	45	Gnd		Gnd	46	Gnd
Odd D10	47	DQS14		Even D10	48	SA0
Gnd	49	Gnd		Gnd	50	Gnd
Odd D11	51	DQ60		Even D11	52	SA1
Gnd	53	Gnd		Gnd	54	Gnd
Odd D12	55	DQ61		Even D12	56	SA2
Gnd	57	Gnd		Gnd	58	Gnd
Odd D13	59	DQ62		Even D13	60	SDA
Gnd	61	Gnd		Gnd	62	Gnd
Odd D14	63	DQ63		Even D14	64	WP
Gnd	65	Gnd		Gnd	66	Gnd
Odd D15	67	DQS15		Even D15	68	FETEN

Gnd	69	Gnd		Gnd	70	Gnd
NC	71	NC		NC	72	NC
Gnd	73	Gnd		Gnd	74	Gnd
NC	75	NC		NC	76	NC
Gnd	77	Gnd		Gnd	78	Gnd
Odd D16P/CLKP	79	CK1		Even D16P/CLKP	80	NC
Gnd	81	Gnd		Gnd	82	Gnd
Odd D16N/CLKN	83	#CK1		Even D16N/CLKN	84	NC
Gnd	85	Gnd		Gnd	86	Gnd
Odd Ext. Ref.	87	NC		Even Ext. Ref.	88	NC
Gnd	89	Gnd		Gnd	90	Gnd
NC	91	NC		NC	92	NC
Gnd	93	Gnd		Gnd	94	Gnd
Gnd	95	Gnd		Gnd	96	Gnd
+5V	97	NC		+5V	98	NC
+5V	99	NC		+5V	100	NC

4.4 Soft Touch Connectors

Use this section when Soft Touch connectors are used to connect the SUT to the logic analyzer, use section 5.4 for Soft Touch Pro. The connectors each provide for 32 signals plus two clocks. The Soft Touch system uses a micro spring pin technology to probe pads on the target board. No socket must be designed into the target board and no keep-out area is required on the back of the board. Mechanical documentation and layout information can be found on the Agilent web site.

4.5 Soft Touch Connector Placement Techniques

In general, connectors should be placed as close to the probe point as possible to minimize stubs. Refer to Section 4.1 for maximum recommended stub lengths. The following documentation details electrical and mechanical considerations:

E5387-97005 – "Agilent Technologies Soft Touch Connector less Probes

E5404-97001 – "Agilent Technologies E5400 Pro-series Soft Touch Connector less Probes"

The following tables describe an example pinout for the Soft Touch connectors

Lower data bits and strobes

LA input	Pad #	DDR signal		DDR signal	Pad #	LA input	
D1	A1	DQ1		DQ0	B1	D0	
D3	A2	DQ3		DQ2	B2	D2	
GND	A3	GND		GND	B3	GND	
D5	A4	DQ4		DQS0	B4	D4	
D7	A5	DQ6		DQ5	B5	D6	
GND	A6	GND		GND	B6	GND	**ODD**
D9	A7	DQS1		DQ7	B7	D8	
D11	A8	DQ9		DQ8	B8	D10	
GND	A9	GND		GND	B9	GND	
D13	A10	DQ11		DQ10	B10	D12	
D15	A11	DQ12		DQS2	B11	D14	
GND	A12	GND		GND	B12	GND	
Clock (-)	A13	#DQS0		DQS0	B13	Clock (+)	
GND	A14	GND		GND	B14	GND	
D1	A15	DQ14		DQ13	B15	D0	
D3	A16	DQS3		DQ15	B16	D2	
GND	A17	GND		GND	B17	GND	
D5	A18	DQ17		DQ16	B18	D4	
D7	A19	DQ19		DQ18	B19	D6	
GND	A20	GND		GND	B20	GND	**EVEN**
D9	A21	DQ20		DQS4	B21	D8	
LA input	**Pad #**	**DDR signal**		**DDR signal**	**Pad #**	**LA input**	
GND	A23	GND		GND	B23	GND	

D13	A24	DQS5	DQ23	B24	D12
D15	A25	DQ25	DQ24	B25	D14
GND	A26	GND	GND	B26	GND
Clock (-)	A27			B27	Clock (+)

Middle data bits and strobes

LA input	Pad #	DDR signal	DDR signal	Pad #	LA input	
D1	A1	DQ27	DQ26	B1	D0	
D3	A2	DQ28	DQS6	B2	D2	
GND	A3	GND	GND	B3	GND	
D5	A4	DQ30	DQ29	B4	D4	
D7	A5	DQS7	DQ31	B5	D6	
GND	A6	GND	GND	B6	GND	**ODD**
D9	A7	DQ33	DQ32	B7	D8	
D11	A8	DQ35	DQ34	B8	D10	
GND	A9	GND	GND	B9	GND	
D13	A10	DQ36	DQS8	B10	D12	
D15	A11	DQ38	DQ37	B11	D14	
GND	A12	GND	GND	B12	GND	
Clock (-)	A13	GND	TEST	B13	Clock (+)	
GND	A14	GND	GND	B14	GND	
D1	A15	DQS9	DQ39	B15	D0	
D3	A16	DQ41	DQ40	B16	D2	
GND	A17	GND	GND	B17	GND	
D5	A18	DQ43	DQ42	B18	D4	
D7	A19	DQ44	DQS10	B19	D6	
GND	A20	GND	GND	B20	GND	**EVEN**
D9	A21	DQ46	DQ45	B21	D8	
D11	A22	DQS11	DQ47	B22	D10	
GND	A23	GND	GND	B23	GND	
D13	A24	DQ49	DQ48	B24	D12	
D15	A25	DQ51	DQ50	B25	D14	
GND	A26	GND	GND	B26	GND	
Clock (-)	A27	#CK2	CK2	B27	Clock (+)	

Upper data bits and strobes

LA Signal	Pad #	DDR Label		DDR Label	Pad #	LA Signal	
D1	A1	DQ52		DQS12	B1	D0	
D3	A2	DQ54		DQ53	B2	D2	
GND	A3	GND		GND	B3	GND	
D5	A4	DQS13		DQ55	B4	D4	
D7	A5	DQ57		DQ56	B5	D6	
GND	A6	GND		GND	B6	GND	**ODD**
D9	A7	DQ59		DQ58	B7	D8	
D11	A8	DQ60		DQS14	B8	D10	
GND	A9	GND		GND	B9	GND	
D13	A10	DQ62		DQ61	B10	D12	
D15	A11	DQS15		DQ63	B11	D14	
GND	A12	GND		GND	B12	GND	
Clock (-)	A13	#CK1		CK1	B13	Clock (+)	
GND	A14	GND		GND	B14	GND	
D1	A15	DQS17		DQS16	B15	D0	
D3	A16	CB1		CB0	B16	D2	
GND	A17	GND		GND	B17	GND	
D5	A18	CB3		CB2	B18	D4	
D7	A19	CB5		CB4	B19	D6	
GND	A20	GND		GND	B20	GND	**EVEN**
D9	A21	CB7		CB6	B21	D8	
D11	A22	SA1		SA0	B22	D10	
GND	A23	GND		GND	B23	GND	
D13	A24	SDA		SA2	B24	D12	
D15	A25	FETEN		WP	B25	D14	
GND	A26	GND		GND	B26	GND	
Clock (-)	A27	N/C		N/C	B27	Clock (+)	

Command Bus

LA Signal	Pad #	DDR Label		DDR Label	Pad #	LA Signal	
D1	A1	A1		A0	B1	D0	
D3	A2	A3		A2	B2	D2	
GND	A3	GND		GND	B3	GND	
D5	A4	A5		A4	B4	D4	
D7	A5	A7		A6	B5	D6	
GND	A6	GND		GND	B6	GND	**ODD**
D9	A7	A9		A8	B7	D8	
D11	A8	A11		A10	B8	D10	
GND	A9	GND		GND	B9	GND	
D13	A10	A13		A12	B10	D12	
D15	A11	A15		A14	B11	D14	
GND	A12	GND		GND	B12	GND	
Clock (-)	A13	#CK0		CK0	B13	Clock (+)	
GND	A14	GND		GND	B14	GND	
D1	A15	#WE		CKE	B15	D0	
D3	A16	#RAS		#CAS	B16	D2	
GND	A17	GND		GND	B17	GND	
D5	A18	BA1		BA0	B18	D4	
D7	A19	#S1		BA2	B19	D6	
GND	A20	GND		GND	B20	GND	**EVEN**
D9	A21	NC		NC	B21	D8	
D11	A22	ODT1		ODT0	B22	D10	
GND	A23	GND		GND	B23	GND	
D13	A24	N/C		N/C	B24	D12	
D15	A25	N/C		N/C	B25	D14	
GND	A26	GND		GND	B26	GND	
Clock (-)	A27	GND		#S0	B27	Clock (+)	

4.6 SOFT TOUCH PRO

J1 - Command/Address signals

LA Signal	Pad #	DDR Label		DDR Label	Pad #	LA Signal	
D0	A1	A0		GND	B1	GND	
D1	A2	A1		A2	B2	D2	
GND	A3	GND		A3	B3	D3	
D4	A4	A4		GND	B4	GND	**Logic**
D5	A5	A5		A6	B5	D6	**Analyzer**
GND	A6	GND		A7	B6	D7	**ODD**
CK1+	A7	CK0		GND	B7	GND	**Pod**
GND/CK-	A8	#CK0		A8	B8	D8	
GND	A9	GND		A9	B9	D9	
D10	A10	A10		GND	B10	GND	
D11	A11	A11		A12	B11	D12	
GND	A12	GND		A13	B12	D13	
D14	A13	A14		GND	B13	GND	
D15	A14	A15		CKE	B14	D16	
GND	A15	GND		#WE	B15	D17	
D18	A16	#CAS		GND	B16	GND	
D19	A17	#RAS		BA0	B17	D20	
GND	A18	GND		BA1	B18	D21	**Logic**
D22	A19	BA2		GND	B19	GND	**Analyzer**
D23	A20	#S1		GND	B20	GND/CK2-	**EVEN**
GND	A21	GND		#S0	B21	CK2+	**Pod**
D24	A22	NC		GND	B22	GND	
D25	A23	NC		ODT0	B23	D26	
GND	A24	GND		ODT1	B24	D27	
D28	A25	N/C		GND	B25	GND	
D29	A26	N/C		N/C	B26	D30	
GND	A27	GND		N/C	B27	D31	

J2 - Lower Data bits and Strobes

LA Signal	Pad #	DDR Label		DDR Label	Pad #	LA Signal	
D0	A1	DQ0		GND	B1	GND	
D1	A2	DQ1		DQ2	B2	D2	
GND	A3	GND		DQ3	B3	D3	
D4	A4	DQS0		GND	B4	GND	**Logic**
D5	A5	DQ4		DQ5	B5	D6	**Analyzer**
GND	A6	GND		DQ6	B6	D7	**ODD**
CK1+	A7	DQS0		GND	B7	GND	**Pod**
GND/CK-	A8	#DQS0		DQ7	B8	D8	
GND	A9	GND		DQS1	B9	D9	
D10	A10	DQ8		GND	B10	GND	
D11	A11	DQ9		DQ10	B11	D12	
GND	A12	GND		DQ11	B12	D13	
D14	A13	DQS2		GND	B13	GND	
D15	A14	DQ12		DQ13	B14	D16	
GND	A15	GND		DQ14	B15	D17	
D18	A16	DQ15		GND	B16	GND	
D19	A17	DQS3		DQ16	B17	D20	
GND	A18	GND		DQ17	B18	D21	**Logic**
D22	A19	DQ18		GND	B19	GND	**Analyzer**
D23	A20	DQ19		GND	B20	GND/CK2-	**EVEN**
GND	A21	GND		N/C	B21	CK2+	**Pod**
D24	A22	DQS4			B22	GND	
D25	A23	DQ20		DQ21	B23	D26	
GND	A24	GND		DQ22	B24	D27	
D28	A25	DQ23		GND	B25	GND	
D29	A26	DQS5		DQ24	B26	D30	
GND	A27	GND		DQ25	B27	D31	

J3 - Middle Data bits and Strobes

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D0	A1	DQ26	GND	B1	GND	
D1	A2	DQ27	DQS6	B2	D2	
GND	A3	GND	DQ28	B3	D3	
D4	A4	DQ29	GND	B4	GND	**Logic**
D5	A5	DQ30	DQ31	B5	D6	**Analyzer**
GND	A6	GND	DQS7	B6	D7	**ODD**
CK1+	A7	TEST	GND	B7	GND	**Pod**
GND/CK-	A8	GND	DQ32	B8	D8	
GND	A9	GND	DQ33	B9	D9	
D10	A10	DQ34	GND	B10	GND	
D11	A11	DQ35	DQS8	B11	D12	
GND	A12	GND	DQ36	B12	D13	
D14	A13	DQ37	GND	B13	GND	
D15	A14	DQ38	DQ39	B14	D16	
GND	A15	GND	DQS9	B15	D17	
D18	A16	DQ40	GND	B16	GND	
D19	A17	DQ41	DQ42	B17	D20	
GND	A18	GND	DQ43	B18	D21	**Logic**
D22	A19	DQS10	GND	B19	GND	**Analyzer**
D23	A20	DQ44	#CK2	B20	GND/CK2-	**EVEN**
GND	A21	GND	CK2	B21	CK2+	**Pod**
D24	A22	DQ45	GND	B22	GND	
D25	A23	DQ46	DQ47	B23	D26	
GND	A24	GND	DQS11	B24	D27	
D28	A25	DQ48	GND	B25	GND	
D29	A26	DQ49	DQ50	B26	D30	
GND	A27	GND	DQ51	B27	D31	

Upper Data bits and Strobes

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D0	A1	DQS12	GND	B1	GND	
D1	A2	DQ52	DQ53	B2	D2	
GND	A3	GND	DQ54	B3	D3	
D4	A4	DQ55	GND	B4	GND	**Logic**
D5	A5	DQS13	DQ56	B5	D6	**Analyzer**
GND	A6	GND	DQ57	B6	D7	**ODD**
CK1+	A7	CK1	GND	B7	GND	**Pod**
GND/CK-	A8	#CK1	DQ58	B8	D8	
GND	A9	GND	DQ59	B9	D9	
D10	A10	DQS14	GND	B10	GND	
D11	A11	DQ60	DQ61	B11	D12	
GND	A12	GND	DQ62	B12	D13	
D14	A13	DQ63	GND	B13	GND	
D15	A14	DQS15	DQS16	B14	D16	
GND	A15	GND	DQS17	B15	D17	
D18	A16	CB0	GND	B16	GND	
D19	A17	CB1	CB2	B17	D20	
GND	A18	GND	CB3	B18	D21	**Logic**
D22	A19	CB4	GND	B19	GND	**Analyzer**
D23	A20	CB5		B20	GND/CK2-	**EVEN**
GND	A21	GND	N/C	B21	CK2+	**Pod**
D24	A22	CB6	GND	B22	GND	
D25	A23	CB7	SA0	B23	D26	
GND	A24	GND	SA1	B24	D27	
D28	A25	SA2	GND	B25	GND	
D29	A26	SDA	WP	B26	D30	
GND	A27	GND	FETEN	B27	D31	

Section 5: Logic Analyzer Features

5.1 TRIGGERING

When capturing DDR2 traffic the Agilent 16700 and 16900 logic analyzer modules can capture data at or above 200 MT/s, assuming proper high frequency design rules have been followed. At speeds above 300 MT/s the 16753-16756 and 16950 logic analyzer modules must be set to the 600 MHz State mode (i.e. "turbo mode"). The 16750-16752 logic analyzer modules must be set to the 400 MHz State mode for speeds above 200 MT/s, and the 450 MHz State mode for the 16910/911 for speeds above 450 MT/s. In these high-speed state modes the number of available sequence levels is reduced from 16 to 6, using time tags pod count is reduced by 2 pods or 1 pod pair.

5.2 DATA DISPLAY

5.2.1 FuturePlus FS1123 OR FS1124 Transaction Software

If the FuturePlus FS1123 or FS1124 software is installed, the bus transactions will be decoded and displayed. The logic analyzer contains a waveform viewer, and linear listing window to view sampled data.

If the FuturePlus FS1123 or FS1124 is not installed, the listing window will display the data as HEX, Binary, Octal, or Decimal. Symbols can be created by the user refer to Section 2.4

5.3 SIGNAL THRESHOLD VOLTAGE SETTINGS

5.3.1 Threshold Considerations for Tristate

Each DDR2 bus implementation will have different timing due to trace length variation on the motherboard, variations in bus loading for each DIMM configuration, and sensitivity to dynamic factors such as crosstalk or simultaneous switching noise. Many of these timing characteristics are fixed. These differences are difficult or impossible to predict in advance for a variety of implementations and configurations of DIMMs.

Eye Finder is used to measure the fixed component of these implementation dependent timing characteristics so that the analyzer can sample all DQS* strobed signals using the single strobe DQS0 (or any DQS chosen) and achieve reliable state capture.

Stimulus dependent timing is taken into account by running the Eye Finder while worst case bus traffic occurs. The worst case data valid window boundaries are found and the analyzer is set to sample data at the center of the actual data valid window of each signal for each specific DDR2 implementation and DIMM configuration.

Because the strobes are tri-stated between bursts, their logic value is undefined. Some systems will terminate the DDR2 bus to a voltage close to the Vref voltage, causing the strobes to sit right at the switching threshold. During read bursts, because read data (and strobes) are actually not valid until the reflected wave reaches the probe, DQS0 may also spend a significant amount of time at Voh/2 (close to Vref) between arrival of the incident wave and the reflected wave. Therefore, simply comparing the DQS0 signal to Vref will result in spurious analysis clocks being generated between bursts and during read bursts.

You can vary the logic analyzer threshold to avoid false clocking. Each time you vary the threshold, run Eye Finder. This will let you to determine the optimal threshold setting for data capture and correct clocking. Another approach to try on a differential data strobe pair that is used as a clock input, is to add a weak pull-up to Vdd and pull-down to Vss on the + and – line respectively. If pads are placed in the layout, then a small (0402) resistor can be experimented with, e.g.20K ohms, to keep each side of the differential line from "rattling around" when the strobes are not active. This can greatly increase the utility of this signal as a clock for Eye measurements of data activity.

All of these factors combine to add jitter to the read and write strobes. This jitter reduces the data valid window available to the logic analyzer. In some systems and DIMM configurations that have tight bus timing this may make it difficult to find an appropriate point to sample state data. This is especially true for read bursts, which usually have more complex strobe and data waveforms. Eye Finder will measure the data valid window available to the analyzer for each signal and clearly indicate which ones may have difficulty reliably sampling state data given actual DDR2 bus timing.

5.4 TRACING THE SERIAL PRESENCE DETECT SIGNALS

The Agilent Serial Analysis tool can be used to decode the Serial Presence Detect lines and view the SPD programming as bytes rather than as serial bits. This is best done by loading the timing config and using a slow sample rate about 4x the SPD clock rate.

5.5 CROSS BUS ANALYSIS

Real time acquisition of DDR2 traffic along with concurrent transactions on other system busses such as PCI-X, USB, SCSI and many others is supported. Use of an Agilent logic analyzer enables events on one bus to trigger measurements on other types of busses providing time-correlated views of all bus events. This capability is commonly referred to as cross-bus analysis. In addition, cross-triggering with global markers enables quick correlation between different buses.

FuturePlus Systems offers support for a wide variety of industry standard buses. To learn more please visit our web site at www.futureplus.com.

Logic Analyzer Card Configurations

5.6 LOGIC ANALYZER CARD REQUIREMENTS

Probing DDR2 requires two to four logic analyzer cards depending on the bus speed, whether state or timing measurements are being used, and the type of logic analyzer card being used. For full channel timing measurements, only two cards (configured as a single logic analysis module using one analyzer "machine") are necessary. For capturing simultaneous read/write data in state mode 4 logic analyzer cards are required. The preferred logic analyzer card is 16753 – 16756 or 16950 cards because of their lower signal loading characteristics, as well as their higher speed.

5.7 FS1123 OR FS1124 LOGIC ANALYZER CARD CONFIGURATION OPTIONS

DDR2 Bus Speed	16900 Analyzer Type	16700 Analyzer Type	Timing Analysis	State Analysis (with 2 GHz TimingZoom™)
400 MT/s	*16750/751/752 16753-756, *16910 w/ option 500	*16750-752 16753-756	2 cards configured as one module with one timing machine	• 4 cards configured as 1 module
	*16911 w/ option 500		2 cards configured as one module with one timing machine	• 3 cards configured as 1 module
Up to 533 MT/s	16753-756 16950	16753-756	2 cards configured as one module with one timing machine	• 4 cards configured as 1 module

Table 7-1

*** We do not recommend using these cards**

Section 6: Equipment Requirements for DDR2 Support

6.1 Supported Logic Analyzer Modules for DDR

The 16753-756 or 16950 logic analyzer family and higher are recommended for DDR2 applications. The frequency requirements, Eyescan feature and better setup and hold window makes the 16753-756 or 16950 or higher numbered state/timing modules necessary.

Timing analysis only requires 2 modules. State mode analysis of Read and Write Data simultaneously requires a 4 module solution. If only Read or Write State Data is required then only 3 state/timing modules are required and the double probing is eliminated, however the protocol decoder will not work.

Agilent Part #	***State Speed***	***Channels***	***Memory Depth***
16750/1/2A	400 MHz	68	4M / 16M / 32M State
*16753/4//5/6A	600 MHz	68	1M / 4M / 16M / 64M State
16910/911A	450 MHz	68/102	1M State
*169506A	600 MHz	68	1M / 4M / 16M / 64M State

*recommended

Agilent Part #	***Description***
16702B	Mainframe with display and touch-screen
16700B	Mainframe with no display
16701B	Expansion Frame
16902A	Mainframe with display and touch-screen
16900A	Mainframe with no display

6.2 Probing Part Numbers and Ordering Information

Agilent Part #	***Description***
E5378A	Termination Adapter, 100 pin to Samtec
E5385A	Termination Adapter, 40 pin to Samtec
E5390A	Termination Adapter, 100 pin to Soft Touch
E5394A	Termination Adapter, 40 pin to Soft Touch
E5404A	Termination Adapter, 40 pin to Soft Touch Pro
E5406A	Termination Adapter, 100 pin to Soft Touch Pro

6.3 Supplemental Documentation

Publication #	***Description***
5968-4632A	Probing Solutions for Agilent Technologies Logic Analysis Systems
5968-9661E	Agilent Technologies 16700 Series Logic Analysis System Product Overview
5989-0422EN	Agilent Technologies 16900 Series Logic Analysis System Product Overview
TN-47-01	Micron DDR2 Design Guide
JESD79-2	JEDEC DDR2 SDRAM Design Guide

6.4 TECHNICAL SUPPORT

FuturePlus Web Site: www.futureplus.com

Agilent Technologies Web Site: www.agilent.com

FuturePlus® Systems

Post Sales Technical Support:
TEL:603 471-2734 X16
FAX:603 471-2738
tech_sup@futureplus.com

Pre-Sales Technical Support:
TEL: 719 278-3540 x11, x12
FAX: 719 278-9586
www.futureplus.com/contact.html