

FuturePlus[®] Systems



Application Note: Embedded DDR1 SDRAM Special Connection Solutions

FS1107 Embedded DDR1 Analysis Software for 16700
FS1125 Embedded DDR1 Analysis Software for 16900

Version 1.5
October 12, 2004

FuturePlus Systems

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Section 1: DDR Logic Analysis Support

1.1 DESCRIPTION

This application note describes the methodology required to test a DDR SDRAM channel when a DIMM socket is not present. Placement of Mictor®, Samtec or Soft Touch connectors on the board under test is required. Included is a description of the design requirements for the test connection that will enable valid signal capture when using the Agilent Technologies 16700-Series Logic Analysis System. This application note is specific to the Agilent 16700 series of logic analyzers when using the 1675X or 16717/8/9 state/timing analysis modules.

FuturePlus Systems FS1107 and FS1125 embedded DDR SDRAM software license provides logic analyzer configuration and transaction level decode of the DDR SDRAM memory bus traffic. The transaction decode software includes all data commands and ECC signals.

The FS1107 and FS1125 Users Manuals are an additional valuable reference that should be used in conjunction with this application note.

A thorough knowledge of electrical engineering and PCB design is assumed. While this application note provides guidelines and suggestions, it is not a comprehensive step-by-step design guide. These recommendations assume standard engineering and safety practices. Because each design is unique FuturePlus Systems assumes no liability or responsibility for damage to the system or device under test. This document is subject to change and/or revision without notice.

1.2 FUTUREPLUS® SYSTEMS

FuturePlus Systems designs and manufactures Bus Analysis Probes that are used in conjunction with Agilent Technologies logic analyzers. Bus Analysis Probes are powerful and versatile tools that provide a mechanical, electrical, and software interface between the bus and the logic analyzer. These analysis probes enable the engineer to view bus activity - from basic timing waveforms to complete compliance verification. Our products provide measurement solutions for DDR SDRAM, PCI-X, USB 2.0, and many other buses.

FuturePlus Systems has been designing analysis probes since 1991. Our products are used worldwide by hundreds of different companies using standard industry buses in PC's, workstations and embedded processor systems. A bus analysis solution from FuturePlus Systems coupled with an Agilent Technologies logic analyzer is clearly the best development tool you can choose.

To learn more about these state of the art analysis tools, visit our website at www.futureplus.com, click on the Products button and select the computer bus of interest. Learn more about product features, specifications and ordering information. You will also find mechanical drawings, photographs of the product, downloadable software, and much more - all designed to help you choose the correct tool for your design.

FuturePlus Systems is proud to be a Premier Solutions Partner of Agilent Technologies' Value-Added Business Program.

1.3 ACKNOWLEDGEMENT

FuturePlus wishes to recognize and thank Perry Keller and Jennie Grosslight of Agilent Technologies for their work in helping to create this document. Without their hard work and technical expertise this document would not have been possible.

1.4 GLOSSARY OF TERMS

Terminology Description

<i>DDR</i>	Double Data Rate
<i>SDRAM</i>	Synchronous Dynamic Random Access Memory
<i>SUT</i>	Signal Under Test
<i>SMT</i>	Surface Mount
<i>PCB</i>	Printed Circuit Board
<i>LVTTTL</i>	Low Voltage TTL Logic
<i>SSTL-2</i>	Stub Series Terminated Logic (2.5 Volt)
<i>SSTL-3</i>	Stub Series Terminated Logic (3.3 Volt)
<i>Mictor™</i>	Matched Impedance Connector (Used with termination adapter cables)
<i>Samtec™</i>	Matched Impedance Connector (Used with termination adapter cables)
<i>Soft Touch</i>	Matched Impedance Connection System (Used with termination adapter cables)
<i>FS1107</i>	EmbeddedDDR1 software license, for 16700/02 (Agilent model number FSI-60063)
<i>FS1125</i>	EmbeddedDDR1 software license, for 16900/902 (Agilent model number FSI-60101)

Logic Analyzer Modules – “Module” – A set of logic analyzer card(s) that have been configured (via cables connecting multiple cards) to operate as a single logic analyzer whose total available channels is the sum of the channels on each card. A trigger within a module can be specified using all of the channels of that module. Each module may be further broken up into “Machines.” A single module may not extend beyond a single 5 card 16700 mainframe or a single 6 card 16900 mainframe.

Logic Analyzer Machines – “Machine” – A set of logic analyzer pods from a logic analyzer module grouped together to operate as a single state or timing analyzer. Each logic analyzer module may be partitioned into up to two independent “Machines” (either two state machines, or state and a timing machine), and the pods of a module may be assigned freely to either machine. Each state analyzer machine has its own state clock. Turbo mode (333 MHz for 1671x or 400 MHz for 1675x cards) operation restricts a module to having only one machine. Cross triggering between modules or machines is done via the Intermodule Bus or via the Flag bits, which will communicate across a 16700 frame and its expander, or across multiple frames if the Multiframe product is used.

Logic Analyzer Requirements – Only 16717/8/9A, 1675XA and 16950 modules will work for the solutions described in this application note. Only 16753-16756 modules can be mixed within a module.

For more information regarding the 16700 or 16900 Logic Analyzers please refer to the Agilent web site at www.agilent.com/find/logicanalyzer.

1.5 UNIQUE DDR PROBING CONSIDERATIONS

DDR has a differential clock CK0/CK0#. For the purpose of discussion in this document, the crossing of CK0 and CK0# will be considered to be the mid-point of CK0 rising.

DDR can be thought of as consisting of two buses; the command bus and the data bus. The DDR command bus is clocked on the rising edge of CK0. State or timing analysis of the command bus does not take any special considerations for logic analyzer operation.

The data bus is clocked from strobes derived from both the rising and falling edges of CK0. Strobe edges straddle the Data on READ and are centered about Data on WRITE. State mode analysis of the data bus demands special considerations, covered in Section 3 State Analysis Operation.

Timing analysis of the data bus does not require special clocking considerations for proper logic analyzer operation.

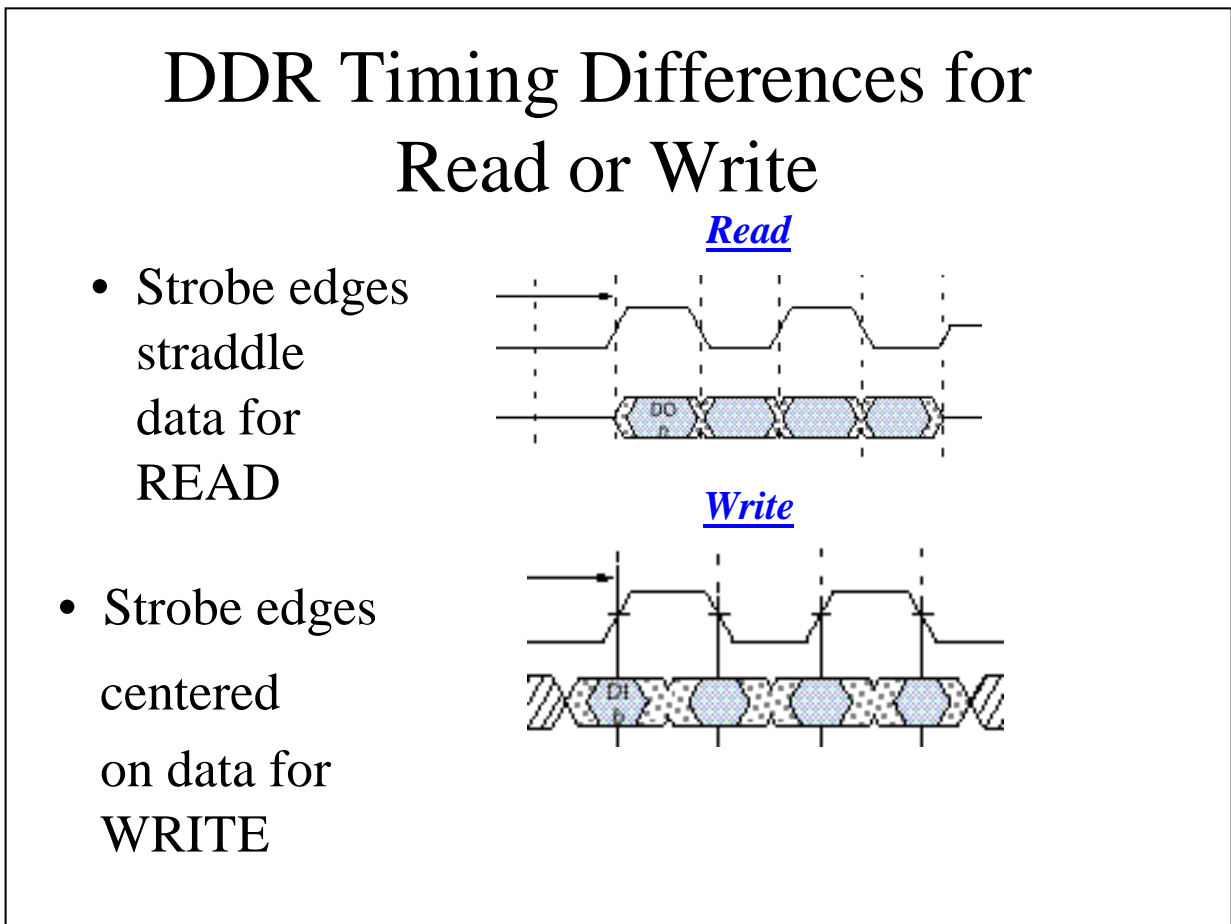


Figure 1-4

Section 2: Timing Analysis Operation

2.1 SELECT TERMINATION NETWORK AND ROUTE CONNECTORS

Refer to Section 4 for optimal termination network requirements and specified logic analyzer probe adapters. Refer to Section 5 for Mictor, Samtec and Soft Touch connector signal routing.

2.2 LOGIC ANALYZER MODULES AND CONFIGURATIONS

Refer to Section 7, Table 7-1 for logic analyzer modules and configurations

2.3 CONFIGURING THE LOGIC ANALYZER

Configuration of the logic analyzer can be performed by loading the appropriate FuturePlus FS1107 or FS1125 embedded DDR software license or by manually configuring the Agilent logic analyzer. For specific details on using the logic analyzer, for example creating symbols or loading files, refer to the 16700 or 16900 Users Manual.

2.3.1 Configuring the logic analyzer using the FS1107 or FS1125 software

2.3.1 Refer to the instructions in the FS1107 or FS1125 Users Manual

2.3.2 Configuring the logic analyzer manually

2.2.2.1 Select the module that you wish to use.

2.2.2.2 Select full channel timing in the setup window at the sampling tab.

2.2.2.3 Select the Format tab, set the labels and channel assignments per tables in Section 5 or to any unique format desired. Custom channel assignments may have some limitations with triggering.

2.2.2.4 At the Format tab, set the pod threshold levels. For most cases this will be 1.25V. See section 6.3 for a more detailed discussion on setting threshold.

2.2.2.5 Symbols can be created by selecting the Symbol tab, then select the User Definable tab, now the user can create custom symbols as explained in Section 2.3

2.2.2.6 Be sure to save your configuration! This is not a procedure you want to repeat every time you turn on your logic analyzer.

2.4 DECODING DDR COMMANDS

No Protocol Decoder is used for timing analysis. However, symbols are pre-defined in the FS1107 or FS1125 software.

SYMBOL	VALUE
NOP	111
ACTIVATE	011
READ	101
WRITE	100
BST	110

PRECHARGE	010
REFRESH	001
LOADMODE	000

Table 2-3

To use these symbols simply choose the label CMD and change HEX to SYMBOLS and choose the symbol you want.

Symbols can be manually created for the DDR Command bus. The RAS, CAS, and WE lines can be decoded to display the DDR Command as “Read”, “Write”, “Precharge”, etc., so you don’t have to refer to the DDR chip data sheet to see what command is being executed. Symbols can also be pre-defined for the read/write status.

These decoded values are displayed by setting the display base (in the listing window) or the label property (in the waveform window) to “Symbols”. The display base defaults to hexadecimal.

If you decide to create symbols, be sure to save them with your configuration.

2.5 TAKING A TRACE, TRIGGERING, AND SEEING MEASUREMENT RESULT

Timing analysis is the simplest setup, and there are no special factors involved in analyzer trigger setup, initiating a trace, and viewing results. For the Command bus you can use pre-defined symbols to specify mnemonically the command you wish to trigger on.

Section 3: State Analysis Operation

3.1 SELECT TERMINATION NETWORK AND ROUTE CONNECTORS

Refer to Section 4 for optimal termination network requirements and specified logic analyzer probe adapters. Refer to Section 5 for Mictor, Samtec and Soft Touch connection signal routing. See Section 4 for optimal termination network requirements.

3.2 LOGIC ANALYZER MODULES AND CONFIGURATIONS

Refer to Section 7, Table 7-1 for logic analyzer modules and configurations.

3.3 LOGIC ANALYZER OPERATING SYSTEM REQUIREMENTS

State analysis of DDR with 16717 or higher cards requires version A.02.80.00 (or later) of the 16700 System Operating Software. You can check to see if you already have the correct version by opening the "System Administration" dialog and selecting the "About" button. If you do not have the correct version then you must update your system software. Please consult the 16700 system documentation for the SW update procedure. Version A.02.80.00 or later is necessary to run dual sample for simultaneous read/write data capture in state mode. All versions of the 16900 operating system software are supported.

3.4 STATE CLOCK CONSIDERATIONS - PROBING A DIFFERENTIAL CLOCK

State capture of the Address and Command lines of the DDR bus requires one clock edge for reliable results. Since the DDR clock is differential, there are two possibilities for probing the clock:

- 1) CK0 can be used as the clock for the analyzer. It must be properly terminated to CK0# per normal DDR requirements. The proper termination is a 120-ohm resistor between CK0 and CK0#. This is required for proper operation of the differential clock. No extra termination is required for probing. Probe as close the termination resistor as possible. Match the stub lengths to the probe tips within 1/10 inch for CK0 and CK0#.
- 2) An alternate approach is to add a differential receiver to your board and convert CK0/CK0# to single ended form and connect the single ended clock to the analyzer clock input on the Mictor. Be sure to consider the skew added by the receiver.

3.5 STATE MODE TRACE CAPTURE

State mode analysis of DDR is performed with one machine. State analysis requires signals that are clocked on the both edges of CK0 (CK0/CK0# crossing). The FS1107 and FS1125 take advantage of a feature of the analyzer called dual sample. Dual sample allows signals to be sampled at different times. Because DDR is sampled differently between reads and writes dual sample is used to capture data for reads and data for writes. Two sets of labels are created, one set is calibrated to capture read data and another set is calibrated to capture write data, the protocol decoder will display the correct data with the correct command. In order for the data to be displayed correctly timing zoom is used to set the sample points for read and write data, additionally the user must set preferences in the protocol decoder (e.g. burst size, chip selects used, cas latency).

The FS1107 and FS1125 embedded DDR software will load the appropriate configuration files assigning all channels, predefine the clocks, and load symbols. The Protocol Decoder, which is automatically loaded as part of the configuration file, will decode the data and display it as transactions.

All single ended signals clocked from CK0 rising (Address, Bank Select, and RAS/CAS/WE etc) should be routed to one test connector. The suggested routing connection is listed in Section 5. If signals are

routed per table in the back then after loading the configuration file provided with the FS1107 and FS1125 no changes to the format is required, however if signals are not routed per table in this document then the user will need to make some changes to the configuration file to properly capture data.

3.5.1 State mode Capture of Data Signals

- 1) Route the DQ, DQS, and CB lines to your test connectors per Section 5.
- 2) Make sure that Pod 1 of the "master" analyzer card contains the DDR clock (CK0).
- 3) Connect the test connectors via terminated adapter to a separate set of analyzer cards configured into a single analyzer module. The number of cards depends on how many DDR signals you connect. You will need one card for the first test connector and one additional card for every two test connectors beyond that.

Because the Data straddles the strobe edges on READS and is centered on the strobe edges for WRITES, additional challenges are presented. There are four methods to work around this issue:

Note: Method 3 is the method the protocol decoder will work for.

Method 1 - Design a clock control/generation circuit to deal with the required delays and clock qualification to provide one clock out to the "J" Clock input to the logic analyzer. (FuturePlus does not provide design details on clock generation/recovery circuitry.)

Method 2 - Run traffic that generates only READ or WRITE traffic and make adjustment and measurements on either READ or WRITE traffic separately.

Decide whether you want to trace read or write bursts. Create DDR traffic that contains ONLY those kinds of bursts, and run Eye Finder on the data analyzer to set its sample position properly for that burst type. You may need to adjust the analyzer threshold to get a reliable data eye. This is because the DQS clock floats in between bursts and can generate false analyzer clocks if the analyzer threshold is close to Vref (1.25v).

Method 3 – This method uses the common clock (CK0) and not the strobes to latch DQ data. You must reconfigure the analyzer cards for the command and data analyzers into a single analyzer module. The original command analyzer card must be the master card of the module and CK0 must drive the "J" clock of the module.

Configure the LA cards as one four-card module and set the threshold to 1.25V. You will now be clocking the command bus at a 2x rate. That means every other command will be invalid. You will also be sampling the DQ data bus even when bursts are not occurring.

The invalid command bus states can be ignored by qualifying each command with a (J clock = 0) term which will cause the triggering system to honor the command bus values ONLY for the sample taken on the rise of CK0.

Method 4 – If you do not like double clocking the DDR command bus, you can modify method 3 to create method 4 which preserves the separate analyzer modules for command and data, and clocks the command module on the rise of CK0 as before. However the data module is clocked on both edges of #CK0.

This has the advantage of eliminating the over-sampling of the commands. The Method 3 approach is perfectly correlated because all channels are sampled in one analyzer module.

To enable the Method 4 approach, you need to connect the #CK0 clock to the K clock pin of the data bus Mictor. When using method 4 the analyzer pods would be connected to the Mictor in reverse order as compared to method 3 so that the #CK0 clock would appear on Pod 1 (the J clock) of the DDR data analyzer module. The format spec would be adjusted as well to indicate that pods 1 and 2 have been swapped.

Finally, for methods 3 and 4 the data bus calibration procedure must be modified. Because the analyzer will be sampling data continuously, regardless of whether a burst is active or not, a Timing Zoom trace must be inspected after capturing a real data burst with the data analyzer.

The time difference between the #CK0 signal and the DQS signals must be determined from the Timing Zoom trace. This allows the user to determine how to set the analyzer sample position so that data is sampled in the middle of the data eye for the desired burst type (read or write). The formula for this is:

Reads: Set the setup time in the setup/hold dialog to be equal to the time delay from #CK0 to the DQS signal + 500 pS.

Writes: Set the setup time to be the #CK0 to DQS delay minus 25% of the DDR clock period (1.25 ns for PC200, 900 ps for PC266), plus 500 pS.

Method 3 is the method the FS1107 and FS1125 were designed for. The software will determine when a command is valid and what data is valid when a read or write is identified. Preferences within the protocol decoder need to be set properly in order for the protocol decoder to display data correctly (please see the FS1107 and FS1125 manual for further details).

In order for method 3 to work the operating system on the 16700 or 16702 must be A.02.80.00. This operating system contains a feature called dual sampling. Dual sampling allows a duplicate set of signals to be sampled at a different time. The configuration file that comes with the FS1107 for state mode contains labels that are dual sampled, as an example there are two labels for the data bits, one for reads and one for writes. Once calibration has been completed by the user (see FS1107 manual for further details for calibration) the labels that capture write data will have a different sampling position than the data labels capturing read data. The protocol decoder will then take the data from the correct label and display it with the appropriate command based on the preference settings. For FS1125, all versions of the 16900 operating system are supported.

3.6 EYESCAN

Digital designers are becoming increasingly aware of design problems associated with crosstalk, intersymbol interference and clock and data jitter. A designer must understand the concept of a Data Eye when talking about high speed buses. It is important to consider not only the width of the data valid window, measured in time, but its height as well, measured in voltage. The Data Eye is the single measurement that captures both of these considerations. Finding and maintaining the size of the Eye is the principal challenge in designing and validating high speed busses.

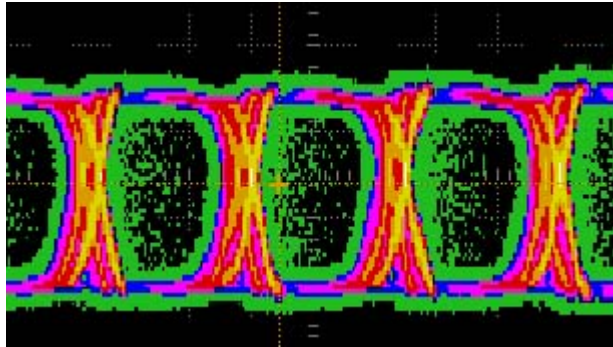
Measuring The Eye

If you put a scope in infinite persistence and let it run repetitively, you build up the familiar eye diagram. The name comes from the fact that it looks like an eye, but also through the eye you can see a lot about the performance characteristics of your circuit and how well it's meeting your signal integrity goals. However, using a scope on multiple signals of a high speed bus can take hours. Agilent has just introduced a new technology called "Eye Scan", which uses the 16700B / 16702B Logic Analysis System

to make the measurements. An Eye Scan of up to 169 signals can take as little as 5 minutes. A list of supported logic analysis modules can be found below. This feature has not yet been implemented in the 16900 series.

Eye Scan Benefits

- Compare signal quality on many signals in minutes
- Archive measurements for later examination
- Quickly verify signal integrity during environmental testing
- Reduce project risk due to signal integrity issues
- Deliver a more reliable product in less time



Section 4: Termination Networks

Termination networks are required for probing a digital signal. The termination network isolates the logic analyzer cabling and sensing circuitry from the signal under test and provides a high impedance, low capacitance load at the probe point.

When probing DDR without a DIMM socket there are two different approaches, (1) Mictor, Samtec or Soft Touch cables with built-in termination networks, and (2) discrete termination networks installed directly on the target system.

Built-in termination networks are incorporated in the Agilent termination adapter cables. Using built-in termination networks requires the least board space. Designers will need to layout the Mictor, Samtec or Soft Touch connectors and route the signals. Signal rise time and stub length to the connectors will determine the feasibility of using built-in terminations.

Discrete termination involves laying out connectors and discrete termination networks on the target system's PC board. This can take up more board space than using cables with built-in termination networks. The advantage of this method is placing the probing tip resistors as close to the controller or DRAM as possible for the optimum signal capture and minimizing stub lengths. Unlike the termination cables with built-in termination networks, the placement of the discrete termination tip resistors is the most critical component.

Additional information about probing with Agilent logic analyzers can be found at www.agilent.com/find/logicanalyzer.

4.1 TERMINATION ADAPTER CABLES WITH BUILT-IN TERMINATION NETWORKS (E5346A / E5380A MICTOR, E5378A / E5380A SAMTEC, E5390A / E5394A SOFT TOUCH, AND E5406 SOFT TOUCH PRO)

The simplest technique for probing the DDR channel is to use Agilent termination adapters with the termination networks built into the cable tip. The E5346A (FuturePlus FS1000) is for use with 16715-16752 logic analyzers. The E5380A (FuturePlus FS1023) is for use with 16753-16756 and 16950 logic analyzers. Both of these termination adapters connect to the Mictor connector.

If you choose to use the Samtec connector, the E5385A (FuturePlus FS1015) is for use with 16715-16752 logic analyzers and the E5378A (FuturePlus FS1014) is for use with 16753-16756 and 16950 logic analyzers.

If you choose to use the Soft Touch footprint (connectorless probing), the E5394A is for use with 16715-16752 logic analyzers and the E5390A is for use with 16753-16756 and 16950 logic analyzers.

If you choose to use the Soft Touch Pro footprint (connectorless probing), the E5406A is for use with 16753-16756 and 16950 logic analyzers.

Signals are routed on the PCB to the test connectors and terminated internally on the termination adapter connector. Connector placement is critical to minimize the stub length which will in turn minimize reflections on signals with fast rise times. However, even the best routing cannot eliminate the stubs completely since the path to the connector and the cable tip is a stub.

The general rule of thumb is to keep the stub length less than 1/5 the rise time of the signal under test (SUT). Refer to the following equations for deciding whether to use built in termination networks.

$$l_{\text{stub}} \leq 1/5 * t_{\text{risetime}} / U_{\text{prop}} \text{speed}$$

$$l_{\text{stub}} \leq 1/5 * t_{\text{risetime}} / v_{\text{prop}} \leq 1/5 * 1000\text{ps} / (150\text{ps} / \text{in}) \leq 1.3'' \quad (1 \text{ ns rise time})$$

$$l_{\text{stub}} \leq 1/5 * t_{\text{risetime}} / v_{\text{prop}} \leq 1/5 * 500\text{ps} / (150\text{ps} / \text{in}) \leq 0.65'' \quad (500 \text{ ps rise time})$$

Whenever it is possible to route the signals within the previous constraints, use the built in termination networks. They are designed for the Agilent logic analysis systems and are compensated to provide flat frequency response between the signal under test and the logic analyzer input comparators.

4.2 DISCRETE TERMINATION NETWORKS (E5351A CABLE WITHOUT TERMINATION)

When routing constraints prohibit using the built-in termination networks, external termination can be designed into the circuit to increase the length between the logic analyzer connector and the signals.

However, this is only recommended under rare cases when routing issues prohibit the use of standard cabling. Discrete termination networks are complex to design and beyond the scope of this document to treat in the general case. Two solutions are provided for signals with 500 and 1000 ps rise times.

The following sections describe the recommended termination network and how to select components for a target system.

4.2.1 Designing a Discrete RCR Termination Network

Refer to the following schematic diagram for designing a discrete termination network.

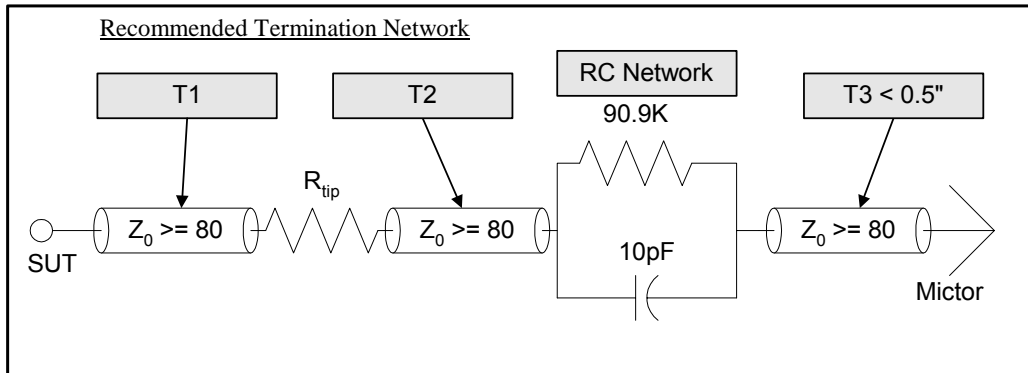


Figure 4-2

SUT Risetime	T1 Length	T2 Length	T3 Length	T1/T2/T3 Impedance	R _{tip}
>= 1ns	<= 1.4"	<= 1.4"	<= 0.5"	Z ₀ >= 80Ω	196Ω
>= 500ps	<= 0.7"	<= 0.7"	<= 0.5"	Z ₀ >= 80Ω	215Ω

Table 4-2

The key parameter to consider when designing a discrete probing network is the rise time of the signal under test. Maximum trace lengths and tip resistor values are dependant upon the rise time.

* Note: The previous values are derived from complex equations that are a function of the logic analyzer connector and cabling electrical characteristics, input network, standard component values, trace

impedance and length, and parasitic capacitance and inductance. It is beyond the scope of this document to provide these equations for general discussion. If the maximum trace lengths specified here are not sufficient to probe the signal under test, please consult an Agilent technical specialist.

T1, T2, and T3 are all 80 Ω or higher PCB traces on the target system that connect the various components in the probing network. It is important to keep the trace impedance as high as possible. It is recommended that outer layers be used which minimize the capacitance and maximize the impedance and propagation speeds. In general, design the trace on an outer layer with as high impedance as possible without implementing out of the ordinary design techniques such as ground plane cutouts. Keep the trace lengths within the tolerances specified in the table.

The tip resistor R_{tip} must be placed within $T1_{length}$ of the SUT. The trace length and tip resistor have been selected to provide maximum frequency response into the logic analyzer input network.

The RC network is connected to R_{tip} via a PCB trace T2 which should not exceed $T2_{length}$. Use precision 0402 or 0603 SMT components for this network (1% R, 5% C).

The connector should be placed as close to the RC network as possible, not to exceed $T3_{length} = 0.5''$ in PCB trace length. The input impedance of the connector and logic analyzer cable is 120Ω . In practice it is very difficult to achieve a matched impedance PCB trace, resulting in an inevitable mismatch. To keep the reflections from degrading the setup and hold margins, the maximum length of T3 has been specified in Table 4-2.

4.2.2 Equivalent Load

The discrete probing network and the logic analyzer input can be modeled as the following equivalent load.

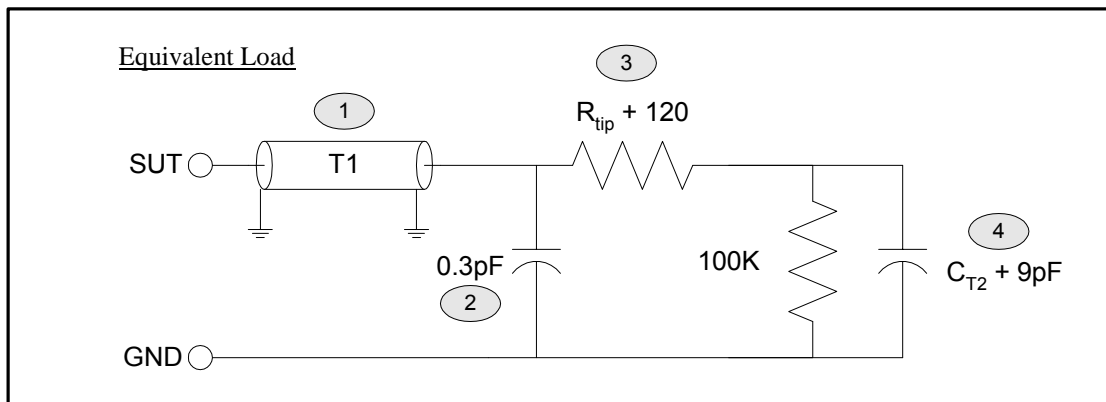


Figure 4 - 3

1. T1 is a PCB trace transmission line specified in Section 4.2.1. R_{tip} is the sum of the tip resistor and the logic analyzer cable impedance.
2. The 0.3pF capacitance is the parasitic capacitance of the tip resistor pads.
3. The equivalent series resistance is the sum of the tip resistor R_{tip} and the 120 Ω (DC component) logic analyzer cable impedance.
4. The capacitive load is the sum of the logic analyzer capacitance plus the T2 PCB transmission line lumped capacitance. Assuming T2 has a length of 1.4" and a 2pF per inch capacitance, the equivalent capacitive load can be calculated by the following equation:

$$C_{equiv} = 9pF + T2_{pF/in} * T2_{length} = 9pF + 2 pF/in * 1.4'' = 11.8 pF$$

4.2.3 Extrapolating T1 and T2 Trace Lengths

It is fairly straightforward to extrapolate the previous values for faster, slower, and intermediate rise times. For signals with rise times faster than 300 ps, a more detailed analysis must be performed. Refer to the following equations for calculating the optimal maximum trace length for the T1 and T2 PCB traces. Note that the following lengths are only approximations since the resistor values are selected to be compatible with industry standard components.

$$l_{\max} \approx t_{\text{risetime}} * (0.7'' / 500\text{ps}), \quad 300\text{ps} < t_{\text{risetime}} \leq 750\text{ps}, \quad R_{\text{tip}} = 215\Omega$$

$$t_{\text{risetime}} > 750\text{ps}, \quad R_{\text{tip}} = 196\Omega$$

4.3 ROUTING TECHNIQUES

Regardless of whether discrete networks are used or not, the following describes some general guidelines for probing high-speed signals and busses. SSTL logic busses are described here.

Note: The following schematics are meant to be a basic guide for probing placement, not a description of how to terminate transmission lines. Please refer to the vendor's documentation for exact termination techniques.

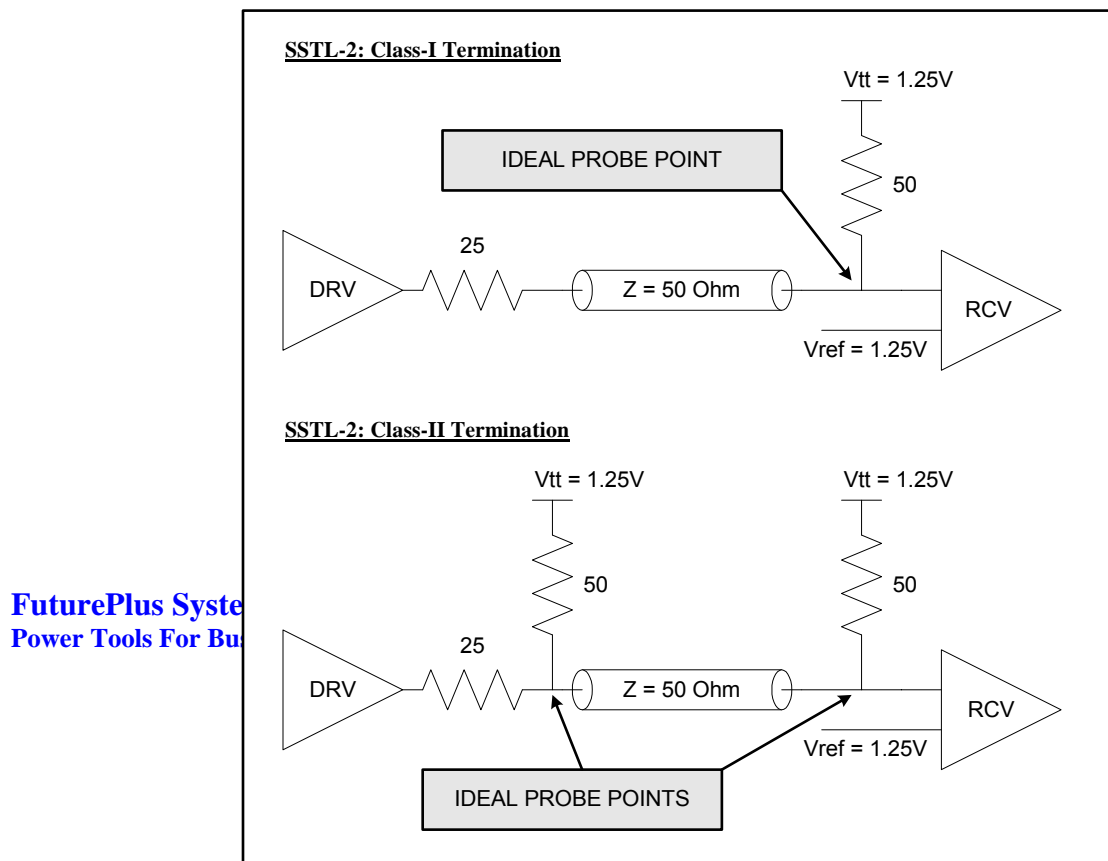
4.3.1 SSTL-2

While SSTL-2 provides excellent high-speed signal fidelity during transmission across a PCB board, issues arise that do not normally occur with single-ended LVTTTL logic.

The following diagram describes an SSTL-2 transmission line. Class-I termination specifies a 50Ω resistor to V_{tt} at the receiver. Class-II termination requires a 50Ω resistor to V_{tt} at both the source and receiver. A 25Ω series resistor is typically designed into the driver. In general, it is safe to probe the signal at or very near the load termination resistors, which may be either end for Class-II busses.

4.3.2 SSTL-3

The technique for termination and probing 3.3 V SSTL logic is the same, except the bias voltage is higher and the logic analyzer threshold must be set to 1.5 V instead of 1.25 V.



4.4 DDR PROBING EXAMPLE

DDR System Block Diagram

Due to loading restrictions and logic analyzer performance, probing DDR data and a differential DDR clock requires adherence to design guidelines. Refer to Sections 4.1 and 4.2 for component values and maximum transmission lengths. Simplified block diagrams of these connection schemes are shown:

DDR System Block Diagram for Probing
with the E5346A or E5378A

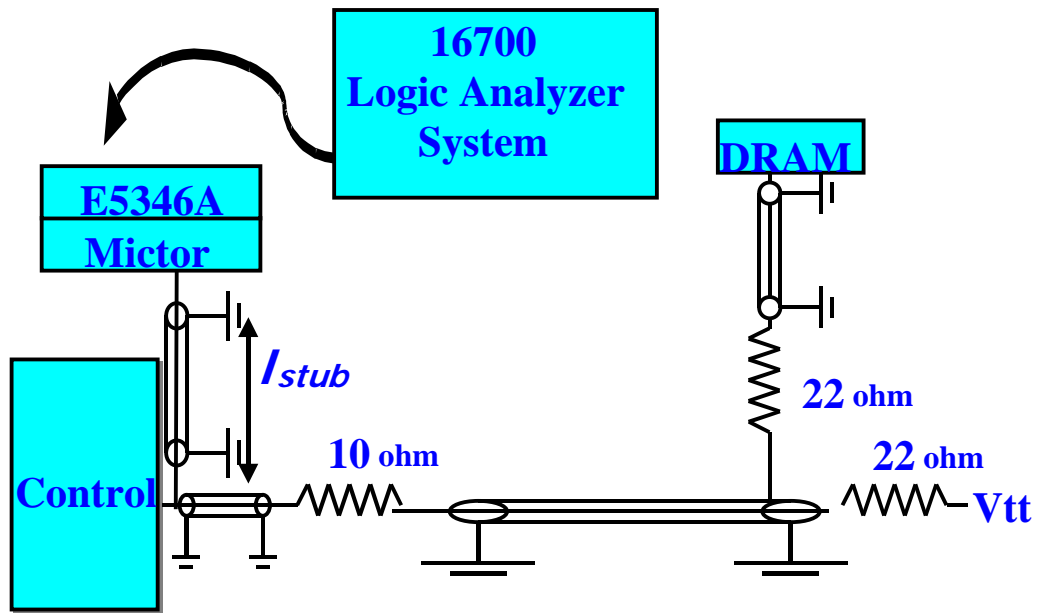


Figure 4-6

DDR System Block
Diagram for Probing with
the E5351A

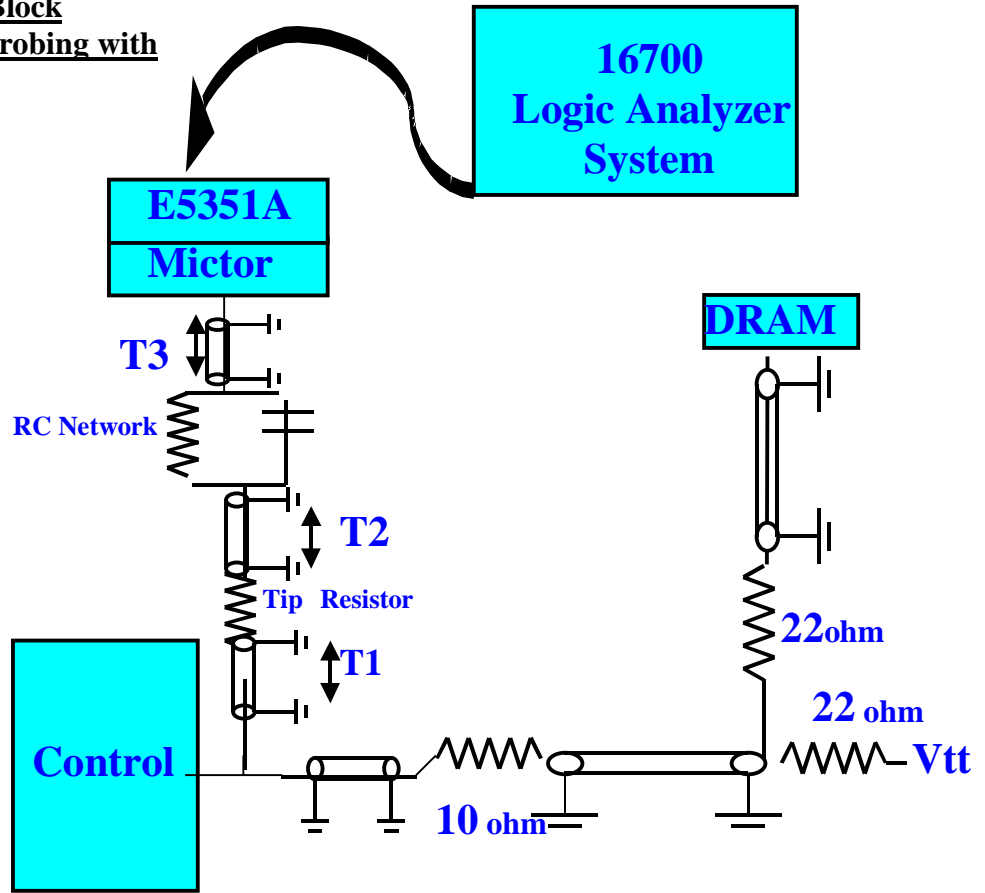


Figure 4-8

Section 5: Logic Analyzer Connectors

5.1 MICTOR CONNECTORS

Use this section when Mictor connectors are used to connect the SUT to the logic analyzer. The connectors each provide for 32 signals plus two clocks. The Mictor connectors each have 38 SMT pins plus 5 through-hole ground returns. Mechanical documentation and layout information can be found on the Agilent web site.

5.2 CONNECTOR PLACEMENT TECHNIQUES

In general, connectors should be placed as close to the probe point as possible to minimize stubs. Refer to Section 4.2 for maximum recommended stub lengths. If discrete termination networks are used because of real estate concerns, connector placement typically becomes less critical since the maximum distance is effectively doubled. Traces from the termination networks should be matched in length so that all signals have equal propagation delays and setup and hold margins are preserved.

5.3 MICTOR CONNECTOR PINOUT

The following tables describe an example pinout for the Mictor-38 connectors.

Agilent requires pins 1-4 to be left unconnected. In addition, the state analyzer clocks MUST be connected to pins 5 and 6. The 5 center plated mounting holes MUST be connected to ground. All other signals are user definable. Bussed signals should place the MSB on pin 7/8, descending downward to the LSB.

J1 - Mictor-38 Connector for the DDR Command Bus

LA Even Pod	Odd Pin Side	Signal	LA Odd Pod	Even Pin Side	Signal
+5V	1	NC	SCL	2	NC
GND DC	3	NC	SDA	4	NC
KCLK	5	#S0	JCLK	6	CK0
D15	7	NC	D15	8	AD15
D14	9	NC	D14	10	AD14
D13	11	NC	D13	12	AD13
D12	13	NC	D12	14	AD12
D11	15	NC	D11	16	AD11
D10	17	NC	D10	18	AD10
D9	19	#S3	D9	20	AD9
D8	21	#S2	D8	22	AD8
D7	23	#S1	D7	24	AD7
D6	25	BA2	D6	26	AD6
D5	27	BA1	D5	28	AD5
D4	29	BA0	D4	30	AD4
D3	31	#RAS	D3	32	AD3
D2	33	#CAS	D2	34	AD2
D1	35	#WE	D1	36	AD1
D0	37	CKE	D0	38	AD0

Table 5-1

IMPORTANT!! Group Data Strobes with associated data channels to minimize any added skew between the strobes and data channels displayed on the Logic Analyzer.

J2 - Mictor-38 Connector for the DDR Data Bus Lower Data Bits & Strobes

LA Even Pod	Odd Pin Side	Signal
+5V	1	NC
GND DC	3	NC
KCLK	5	NC
D15	7	DQ25
D14	9	DQ24
D13	11	DQS5
D12	13	DQ23
D11	15	DQ22
D10	17	DQ21
D9	19	DQ20
D8	21	DQS4
D7	23	DQ19
D6	25	DQ18
D5	27	DQ17
D4	29	DQ16
D3	31	DQS3
D2	33	DQ15
D1	35	DQ14
D0	37	DQ13

Signal	Even Pin Side	LA Odd Pod
NC	2	+5V
NC	4	GND DC
DQS0	6	JCLK
DQ12	8	D15
DQS2	10	D14
DQ11	12	D13
DQ10	14	D12
DQ9	16	D11
DQ8	18	D10
DQS1	20	D9
DQ7	22	D8
DQ6	24	D7
DQ5	26	D6
DQ4	28	D5
DQS0	30	D4
DQ3	32	D3
DQ2	34	D2
DQ1	36	D1
DQ0	38	D0

Table 5-2

J3 - Mictor-38 Connector for the DDR Data Bus Middle Data Bits & Strobes

LA Even Pod	Odd Pin Side	Signal
+5V	1	NC
GND DC	3	NC
KCLK	5	NC
D15	7	DQ51
D14	9	DQ50
D13	11	DQ49
D12	13	DQ48
D11	15	DQS11
D10	17	DQ47
D9	19	DQ46
D8	21	DQ45
D7	23	DQ44
D6	25	DQS10
D5	27	DQ43
D4	29	DQ42
D3	31	DQ41
D2	33	DQ40
D1	35	DQS9
D0	37	DQ39

Signal	Even Pin Side	LA Odd Pod
NC	2	+5V
NC	4	GND DC
NC	6	JCLK
DQ38	8	D15
DQ37	10	D14
DQ36	12	D13
DQS8	14	D12
DQ35	16	D11
DQ34	18	D10
DQ33	20	D9
DQ32	22	D8
DQS7	24	D7
DQ31	26	D6
DQ30	28	D5
DQ29	30	D4
DQ28	32	D3
DQS6	34	D2
DQ27	36	D1
DQ26	38	D0

Table 5-3

J4 - Mictor-38 Connector for the DDR Data Bus Upper Data Bits & Strobes

LA Even Pod	Odd Pin Side	Signal	Signal	Even Pin Side	LA Odd Pod
+5V	1	NC	NC	2	+5V
GND DC	3	NC	NC	4	GND DC
KCLK	5	NC	NC	6	JCLK
D15	7	FETEN	DQS15	8	D15
D14	9	WP	DQ63	10	D14
D13	11	SDA	DQ62	12	D13
D12	13	SA2	DQ61	14	D12
D11	15	SA1	DQ60	16	D11
D10	17	SA0	DQS14	18	D10
D9	19	CB7	DQ59	20	D9
D8	21	CB6	DQ58	22	D8
D7	23	CB5	DQ57	24	D7
D6	25	CB4	DQ56	26	D6
D5	27	CB3	DQS13	28	D5
D4	29	CB2	DQ55	30	D4
D3	31	CB1	DQ54	32	D3
D2	33	CB0	DQ53	34	D2
D1	35	DQS17	DQ52	36	D1
D0	37	DQS16	DQS12	38	D0

Table 5-4

5.4 100 PIN SAMTEC CONNECTOR PINOUT

Use this section when 100 pin Samtec connectors are used to connect the SUT to the logic analyzer. The following table describes the pinout required for the 100 pin Samtec connector used with the E5378A and E5380A cables. Refer to the following Agilent Application notes for additional information:

Publication # 5988-2989EN “Designing High Speed Digital Systems for Logic Analyzer Probing”

If the design does not use all signals listed in the pinout, e.g. less than 64 data bits on the target, then those pins on the connector should be grounded.

5.5 SAMTEC CONNECTIONS FOR E5378A OR E5380A CABLE ADAPTERS

J1 - Command Bus Connections

LA Odd Pod	Odd Side Pin	Signal
Gnd	1	Gnd
NC	3	NC
Gnd	5	Gnd
Odd D0	7	AD0
Gnd	9	Gnd
Odd D1	11	AD1
Gnd	13	Gnd
Odd D2	15	AD2
Gnd	17	Gnd
Odd D3	19	AD3
Gnd	21	Gnd
Odd D4	23	AD4
Gnd	25	Gnd
Odd D5	27	AD5
Gnd	29	Gnd
Odd D6	31	AD6
Gnd	33	Gnd
Odd D7	35	AD7
Gnd	37	Gnd
Odd D8	39	AD8
Gnd	41	Gnd
Odd D9	43	AD9
Gnd	45	Gnd
Odd D10	47	AD10
Gnd	49	Gnd
Odd D11	51	AD11
Gnd	53	Gnd
Odd D12	55	AD12
Gnd	57	Gnd
Odd D13	59	AD13
Gnd	61	Gnd
Odd D14	63	AD14
Gnd	65	Gnd
Odd D15	67	AD15
Gnd	69	Gnd
NC	71	NC
Gnd	73	Gnd
NC	75	NC
Gnd	77	Gnd
Odd D16P/CLKP	79	CK0
Gnd	81	Gnd
Odd D16N/CLKN	83	CK0#
Gnd	85	Gnd
Odd Ext. Ref.	87	NC
Gnd	89	Gnd
NC	91	NC
Gnd	93	Gnd
Gnd	95	Gnd
+5V	97	NC
+5V	99	NC

Signal	Even Side Pin	LA Even Pod
Gnd	2	Gnd
NC	4	NC
Gnd	6	Gnd
Even D0	8	CKE
Gnd	10	Gnd
Even D1	12	#WE
Gnd	14	Gnd
Even D2	16	#CAS
Gnd	18	Gnd
Even D3	20	#RAS
Gnd	22	Gnd
Even D4	24	BA0
Gnd	26	Gnd
Even D5	28	BA1
Gnd	30	Gnd
Even D6	32	BA2
Gnd	34	Gnd
Even D7	36	#S1
Gnd	38	Gnd
Even D8	40	#S2
Gnd	42	Gnd
Even D9	44	#S3
Gnd	46	Gnd
Even D10	48	NC
Gnd	50	Gnd
Even D11	52	NC
Gnd	54	Gnd
Even D12	56	NC
Gnd	58	Gnd
Even D13	60	NC
Gnd	62	Gnd
Even D14	64	NC
Gnd	66	Gnd
Even D15	68	NC
Gnd	70	Gnd
NC	72	NC
Gnd	74	Gnd
NC	76	NC
Gnd	78	Gnd
Even D16P/CLKP	80	#S0
Gnd	82	Gnd
Even D16N/CLKN	84	Gnd
Gnd	86	Gnd
Even Ext. Ref.	88	NC
Gnd	90	Gnd
NC	92	NC
Gnd	94	Gnd
Gnd	96	Gnd
+5V	98	NC
+5V	100	NC

J2 - Data Bus Lower Bits and Strobes

LA Odd Pod	Odd Side Pin	Signal
Gnd	1	Gnd
NC	3	NC
Gnd	5	Gnd
Odd D0	7	DQ0
Gnd	9	Gnd
Odd D1	11	DQ1
Gnd	13	Gnd
Odd D2	15	DQ2
Gnd	17	Gnd
Odd D3	19	DQ3
Gnd	21	Gnd
Odd D4	23	DQS0
Gnd	25	Gnd
Odd D5	27	DQ4
Gnd	29	Gnd
Odd D6	31	DQ5
Gnd	33	Gnd
Odd D7	35	DQ6
Gnd	37	Gnd
Odd D8	39	DQ7
Gnd	41	Gnd
Odd D9	43	DQS1
Gnd	45	Gnd
Odd D10	47	DQ8
Gnd	49	Gnd
Odd D11	51	DQ9
Gnd	53	Gnd
Odd D12	55	DQ10
Gnd	57	Gnd
Odd D13	59	DQ11
Gnd	61	Gnd
Odd D14	63	DQS2
Gnd	65	Gnd
Odd D15	67	DQ12
Gnd	69	Gnd
NC	71	NC
Gnd	73	Gnd
NC	75	NC
Gnd	77	Gnd
Odd D16P/CLKP	79	DQS0
Gnd	81	Gnd
Odd D16N/CLKN	83	Gnd
Gnd	85	Gnd
Odd Ext. Ref.	87	NC
Gnd	89	Gnd
NC	91	NC
Gnd	93	Gnd
Gnd	95	Gnd
+5V	97	NC
+5V	99	NC

Signal	Even Side Pin	LA Even Pod
Gnd	2	Gnd
NC	4	NC
Gnd	6	Gnd
Even D0	8	DQ13
Gnd	10	Gnd
Even D1	12	DQ14
Gnd	14	Gnd
Even D2	16	DQ15
Gnd	18	Gnd
Even D3	20	DQS3
Gnd	22	Gnd
Even D4	24	DQ16
Gnd	26	Gnd
Even D5	28	DQ17
Gnd	30	Gnd
Even D6	32	DQ18
Gnd	34	Gnd
Even D7	36	DQ19
Gnd	38	Gnd
Even D8	40	DQS4
Gnd	42	Gnd
Even D9	44	DQ20
Gnd	46	Gnd
Even D10	48	DQ21
Gnd	50	Gnd
Even D11	52	DQ22
Gnd	54	Gnd
Even D12	56	DQ23
Gnd	58	Gnd
Even D13	60	DQS5
Gnd	62	Gnd
Even D14	64	DQ24
Gnd	66	Gnd
Even D15	68	DQ25
Gnd	70	Gnd
NC	72	NC
Gnd	74	Gnd
NC	76	NC
Gnd	78	Gnd
Even D16P/CLKP	80	NC
Gnd	82	Gnd
Even D16N/CLKN	84	Gnd
Gnd	86	Gnd
Even Ext. Ref.	88	NC
Gnd	90	Gnd
NC	92	NC
Gnd	94	Gnd
Gnd	96	Gnd
+5V	98	NC
+5V	100	NC

J3 - Data Bus Middle Bits and Strobes

LA Odd Pod	Odd Side Pin	Signal
Gnd	1	Gnd
NC	3	NC
Gnd	5	Gnd
Odd D0	7	DQ26
Gnd	9	Gnd
Odd D1	11	DQ27
Gnd	13	Gnd
Odd D2	15	DQS6
Gnd	17	Gnd
Odd D3	19	DQ28
Gnd	21	Gnd
Odd D4	23	DQ29
Gnd	25	Gnd
Odd D5	27	DQ30
Gnd	29	Gnd
Odd D6	31	DQ31
Gnd	33	Gnd
Odd D7	35	DQS7
Gnd	37	Gnd
Odd D8	39	DQ32
Gnd	41	Gnd
Odd D9	43	DQ33
Gnd	45	Gnd
Odd D10	47	DQ34
Gnd	49	Gnd
Odd D11	51	DQ35
Gnd	53	Gnd
Odd D12	55	DQS8
Gnd	57	Gnd
Odd D13	59	DQ36
Gnd	61	Gnd
Odd D14	63	DQ37
Gnd	65	Gnd
Odd D15	67	DQ38
Gnd	69	Gnd
NC	71	NC
Gnd	73	Gnd
NC	75	NC
Gnd	77	Gnd
Odd D16P/CLKP	79	NC
Gnd	81	Gnd
Odd D16N/CLKN	83	Gnd
Gnd	85	Gnd
Odd Ext. Ref.	87	NC
Gnd	89	Gnd
NC	91	NC
Gnd	93	Gnd
Gnd	95	Gnd
+5V	97	NC
+5V	99	NC

Signal	Even Side Pin	LA Even Pod
Gnd	2	Gnd
NC	4	NC
Gnd	6	Gnd
Even D0	8	DQ39
Gnd	10	Gnd
Even D1	12	DQS9
Gnd	14	Gnd
Even D2	16	DQ40
Gnd	18	Gnd
Even D3	20	DQ41
Gnd	22	Gnd
Even D4	24	DQ42
Gnd	26	Gnd
Even D5	28	DQ43
Gnd	30	Gnd
Even D6	32	DQS10
Gnd	34	Gnd
Even D7	36	DQ44
Gnd	38	Gnd
Even D8	40	DQ45
Gnd	42	Gnd
Even D9	44	DQ46
Gnd	46	Gnd
Even D10	48	DQ47
Gnd	50	Gnd
Even D11	52	DQS11
Gnd	54	Gnd
Even D12	56	DQ48
Gnd	58	Gnd
Even D13	60	DQ49
Gnd	62	Gnd
Even D14	64	DQ50
Gnd	66	Gnd
Even D15	68	DQ51
Gnd	70	Gnd
NC	72	NC
Gnd	74	Gnd
NC	76	NC
Gnd	78	Gnd
Even D16P/CLKP	80	NC
Gnd	82	Gnd
Even D16N/CLKN	84	Gnd
Gnd	86	Gnd
Even Ext. Ref.	88	NC
Gnd	90	Gnd
NC	92	NC
Gnd	94	Gnd
Gnd	96	Gnd
+5V	98	NC
+5V	100	NC

J4 - Data Bus Upper Bits and Strobes

LA Odd Pod	Odd Side Pin	Signal
Gnd	1	Gnd
NC	3	NC
Gnd	5	Gnd
Odd D0	7	DQS12
Gnd	9	Gnd
Odd D1	11	DQ52
Gnd	13	Gnd
Odd D2	15	DQ53
Gnd	17	Gnd
Odd D3	19	DQ54
Gnd	21	Gnd
Odd D4	23	DQ55
Gnd	25	Gnd
Odd D5	27	DQS13
Gnd	29	Gnd
Odd D6	31	DQ56
Gnd	33	Gnd
Odd D7	35	DQ57
Gnd	37	Gnd
Odd D8	39	DQ58
Gnd	41	Gnd
Odd D9	43	DQ59
Gnd	45	Gnd
Odd D10	47	DQS14
Gnd	49	Gnd
Odd D11	51	DQ60
Gnd	53	Gnd
Odd D12	55	DQ61
Gnd	57	Gnd
Odd D13	59	DQ62
Gnd	61	Gnd
Odd D14	63	DQ63
Gnd	65	Gnd
Odd D15	67	DQS15
Gnd	69	Gnd
NC	71	NC
Gnd	73	Gnd
NC	75	NC
Gnd	77	Gnd
Odd D16P/CLKP	79	NC
Gnd	81	Gnd
Odd D16N/CLKN	83	Gnd
Gnd	85	Gnd
Odd Ext. Ref.	87	NC
Gnd	89	Gnd
NC	91	NC
Gnd	93	Gnd
Gnd	95	Gnd
+5V	97	NC
+5V	99	NC

Signal	Even Side Pin	LA Even Pod
Gnd	2	Gnd
NC	4	NC
Gnd	6	Gnd
Even D0	8	DQS16
Gnd	10	Gnd
Even D1	12	DQS17
Gnd	14	Gnd
Even D2	16	CB0
Gnd	18	Gnd
Even D3	20	CB1
Gnd	22	Gnd
Even D4	24	CB2
Gnd	26	Gnd
Even D5	28	CB3
Gnd	30	Gnd
Even D6	32	CB4
Gnd	34	Gnd
Even D7	36	CB5
Gnd	38	Gnd
Even D8	40	CB6
Gnd	42	Gnd
Even D9	44	CB7
Gnd	46	Gnd
Even D10	48	SA0
Gnd	50	Gnd
Even D11	52	SA1
Gnd	54	Gnd
Even D12	56	SA2
Gnd	58	Gnd
Even D13	60	SDA
Gnd	62	Gnd
Even D14	64	WP
Gnd	66	Gnd
Even D15	68	FETEN
Gnd	70	Gnd
NC	72	NC
Gnd	74	Gnd
NC	76	NC
Gnd	78	Gnd
Even D16P/CLKP	80	NC
Gnd	82	Gnd
Even D16N/CLKN	84	Gnd
Gnd	86	Gnd
Even Ext. Ref.	88	NC
Gnd	90	Gnd
NC	92	NC
Gnd	94	Gnd
Gnd	96	Gnd
+5V	98	NC
+5V	100	NC

5.6 SOFT TOUCH CONNECTION (CONNECTORLESS PROBING)

Use this section when Soft Touch connections are used to connect the SUT to the logic analyzer. The connections each provide for 32 signals plus two clocks. The Soft Touch system uses a micro spring pin technology to probe pads on the target board. No socket must be designed into the target board, but a retention module is required. No keepout area is required on the back of the board. Mechanical documentation and layout information can be found on the Agilent web site.

5.7 SOFT TOUCH CONNECTION PLACEMENT TECHNIQUES

In general, connections should be placed as close to the probe point as possible to minimize stubs. Refer to Section 4.2 for maximum recommended stub lengths.

The following tables describe an example pinout for the Soft Touch connectors.

J1 - Soft Touch Connections for the DDR Command Bus:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D1	A1	AD1	AD0	B1	D0	
D3	A2	AD3	AD2	B2	D2	
GND	A3			B3	GND	
D5	A4	AD5	AD4	B4	D4	
D7	A5	AD7	AD6	B5	D6	
GND	A6			B6	GND	ODD
D9	A7	AD9	AD8	B7	D8	
D11	A8	AD11	AD10	B8	D10	
GND	A9			B9	GND	
D13	A10	AD13	AD12	B10	D12	
D15	A11	AD15	AD14	B11	D14	
GND	A12			B12	GND	
Clock (-)	A13	CK0n	CK0	B13	Clock (+)	
GND	A14			B14	GND	
D1	A15	#WE	CKE	B15	D0	
D3	A16	#RAS	#CAS	B16	D2	
GND	A17			B17	GND	
D5	A18	BA1	BA0	B18	D4	
D7	A19	#S1	BA2	B19	D6	
GND	A20			B20	GND	EVEN
D9	A21	#S3	#S2	B21	D8	
D11	A22	N/C	N/C	B22	D10	
GND	A23			B23	GND	
D13	A24	N/C	N/C	B24	D12	
D15	A25	N/C	N/C	B25	D14	
GND	A26			B26	GND	
Clock (-)	A27	GND	#S0	B27	Clock (+)	

J2 - Soft Touch Connections for the DDR Lower Data Bits and Strobes:

Lower data bits and strobes

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D1	A1	DQ1	DQ0	B1	D0	
D3	A2	DQ3	DQ2	B2	D2	
GND	A3			B3	GND	
D5	A4	DQ4	DQS0	B4	D4	
D7	A5	DQ6	DQ5	B5	D6	
GND	A6			B6	GND	ODD
D9	A7	DQS1	DQ7	B7	D8	
D11	A8	DQ9	DQ8	B8	D10	
GND	A9			B9	GND	
D13	A10	DQ11	DQ10	B10	D12	
D15	A11	DQ12	DQS2	B11	D14	
GND	A12			B12	GND	
Clock (-)	A13	GND	DQS0	B13	Clock (+)	
GND	A14			B14	GND	
D1	A15	DQ14	DQ13	B15	D0	
D3	A16	DQS3	DQ15	B16	D2	
GND	A17			B17	GND	
D5	A18	DQ17	DQ16	B18	D4	
D7	A19	DQ19	DQ18	B19	D6	
GND	A20			B20	GND	EVEN
D9	A21	DQ20	DQS4	B21	D8	
D11	A22	DQ22	DQ21	B22	D10	
GND	A23			B23	GND	
D13	A24	DQS5	DQ23	B24	D12	
D15	A25	DQ25	DQ24	B25	D14	
GND	A26			B26	GND	

J3 - Soft Touch Connections for the DDR Middle Data Bits and Strobes:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D1	A1	DQ27	DQ26	B1	D0	
D3	A2	DQ28	DQS6	B2	D2	
GND	A3			B3	GND	
D5	A4	DQ30	DQ29	B4	D4	
D7	A5	DQS7	DQ31	B5	D6	
GND	A6			B6	GND	ODD
D9	A7	DQ33	DQ32	B7	D8	
D11	A8	DQ35	DQ34	B8	D10	
GND	A9			B9	GND	
D13	A10	DQ36	DQS8	B10	D12	
D15	A11	DQ38	DQ37	B11	D14	
GND	A12			B12	GND	
Clock (-)	A13	N/C	N/C	B13	Clock (+)	
GND	A14			B14	GND	
D1	A15	DQS9	DQ39	B15	D0	
D3	A16	DQ41	DQ40	B16	D2	
GND	A17			B17	GND	
D5	A18	DQ43	DQ42	B18	D4	
D7	A19	DQ44	DQS10	B19	D6	
GND	A20			B20	GND	EVEN
D9	A21	DQ46	DQ45	B21	D8	
D11	A22	DQS11	DQ47	B22	D10	
GND	A23			B23	GND	
D13	A24	DQ49	DQ48	B24	D12	
D15	A25	DQ51	DQ50	B25	D14	
GND	A26			B26	GND	
Clock (-)	A27	N/C	N/C	B27	Clock (+)	

J4 - Soft Touch Connections for the DDR Upper Data Bits and Strobes:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D1	A1	DQ52	DQS12	B1	D0	
D3	A2	DQ54	DQ53	B2	D2	
GND	A3			B3	GND	
D5	A4	DQS13	DQ55	B4	D4	
D7	A5	DQ57	DQ56	B5	D6	
GND	A6			B6	GND	ODD
D9	A7	DQ59	DQ58	B7	D8	
D11	A8	DQ60	DQS14	B8	D10	
GND	A9			B9	GND	
D13	A10	DQ62	DQ61	B10	D12	
D15	A11	DQS15	DQ63	B11	D14	
GND	A12			B12	GND	
Clock (-)	A13	N/C	N/C	B13	Clock (+)	
GND	A14			B14	GND	
D1	A15	DQS17	DQS16	B15	D0	
D3	A16	CB1	CB0	B16	D2	
GND	A17			B17	GND	
D5	A18	CB3	CB2	B18	D4	
D7	A19	CB5	CB4	B19	D6	
GND	A20			B20	GND	EVEN
D9	A21	CB7	CB6	B21	D8	
D11	A22	SA1	SA0	B22	D10	
GND	A23			B23	GND	
D13	A24	SDA	SA2	B24	D12	
D15	A25	FETEN	WP	B25	D14	
GND	A26			B26	GND	
Clock (-)	A27	N/C	N/C	B27	Clock (+)	

5.8 SOFT TOUCH PRO CONNECTION (CONNECTORLESS PROBING)

Use this section when Soft Touch Pro connections are used to connect the SUT to the logic analyzer. The connections each provide for 32 signals plus two clocks. The Soft Touch system uses a micro spring pin technology to probe pads on the target board. No socket must be designed into the target board, but a retention module is required. No keepout area is required on the back of the board. Mechanical documentation and layout information can be found on the Agilent web site.

5.9 SOFT TOUCH PRO CONNECTION PLACEMENT TECHNIQUES

In general, connections should be placed as close to the probe point as possible to minimize stubs. Refer to Section 4.2 for maximum recommended stub lengths.

J1 - Soft Touch Pro Connections for the Command and Address Bus:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D0	A1	AD0		B1	GND	
D1	A2	AD1	AD2	B2	D2	
GND	A3		AD3	B3	D3	
D4	A4	AD4		B4	GND	Logic Analyzer ODD Pod
D5	A5	AD5	AD6	B5	D6	
GND	A6		AD7	B6	D7	
CK1+	A7	CK0		B7	GND	
GND/CK-	A8	CK0n	AD8	B8	D8	
GND	A9		AD9	B9	D9	
D10	A10	AD10		B10	GND	
D11	A11	AD11	AD12	B11	D12	
GND	A12		AD13	B12	D13	
D14	A13	AD14		B13	GND	
D15	A14	AD15	CKE	B14	D16	
GND	A15		#WE	B15	D17	
D18	A16	#CAS		B16	GND	
D19	A17	#RAS	BA0	B17	D20	
GND	A18		BA1	B18	D21	Logic Analyzer EVEN Pod
D22	A19	BA2		B19	GND	
D23	A20	#S1	GND	B20	GND/CK2-	
GND	A21		#S0	B21	CK2+	
D24	A22	#S2		B22	GND	
D25	A23	#S3	N/C	B23	D26	
GND	A24		N/C	B24	D27	
D28	A25	N/C		B25	GND	
D29	A26	N/C	N/C	B26	D30	
GND	A27		N/C	B27	D31	

J2 - Soft Touch Pro Connections for the Lower Data Bits and Strobes:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D0	A1	DQ0		B1	GND	
D1	A2	DQ1	DQ2	B2	D2	
GND	A3		DQ3	B3	D3	
D4	A4	DQS0		B4	GND	Logic Analyzer ODD Pod
D5	A5	DQ4	DQ5	B5	D6	
GND	A6		DQ6	B6	D7	
CK1+	A7	DQS0		B7	GND	
GND/CK-	A8	GND	DQ7	B8	D8	
GND	A9		DQS1	B9	D9	
D10	A10	DQ8		B10	GND	
D11	A11	DQ9	DQ10	B11	D12	
GND	A12		DQ11	B12	D13	
D14	A13	DQS2		B13	GND	
D15	A14	DQ12	DQ13	B14	D16	
GND	A15		DQ14	B15	D17	
D18	A16	DQ15		B16	GND	
D19	A17	DQS3	DQ16	B17	D20	
GND	A18		DQ17	B18	D21	Logic Analyzer EVEN Pod
D22	A19	DQ18		B19	GND	
D23	A20	DQ19		B20	GND/CK2-	
GND	A21		N/C	B21	CK2+	
D24	A22	DQS4		B22	GND	
D25	A23	DQ20	DQ21	B23	D26	
GND	A24		DQ22	B24	D27	
D28	A25	DQ23		B25	GND	
D29	A26	DQS5	DQ24	B26	D30	
GND	A27		DQ25	B27	D31	

J3 - Soft Touch Pro Connections for the Middle Data Bits and Strobes:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D0	A1	DQ26		B1	GND	
D1	A2	DQ27	DQS6	B2	D2	
GND	A3		DQ28	B3	D3	
D4	A4	DQ29		B4	GND	Logic Analyzer ODD Pod
D5	A5	DQ30	DQ31	B5	D6	
GND	A6		DQS7	B6	D7	
CK1+	A7	N/C		B7	GND	
GND/CK-	A8	N/C	DQ32	B8	D8	
GND	A9		DQ33	B9	D9	
D10	A10	DQ34		B10	GND	
D11	A11	DQ35	DQS8	B11	D12	
GND	A12		DQ36	B12	D13	
D14	A13	DQ37		B13	GND	
D15	A14	DQ38	DQ39	B14	D16	
GND	A15		DQS9	B15	D17	
D18	A16	DQ40		B16	GND	
D19	A17	DQ41	DQ42	B17	D20	
GND	A18		DQ43	B18	D21	Logic Analyzer EVEN Pod
D22	A19	DQS10		B19	GND	
D23	A20	DQ44	N/C	B20	GND/CK2-	
GND	A21		N/C	B21	CK2+	
D24	A22	DQ45		B22	GND	
D25	A23	DQ46	DQ47	B23	D26	
GND	A24		DQS11	B24	D27	
D28	A25	DQ48		B25	GND	
D29	A26	DQ49	DQ50	B26	D30	
GND	A27		DQ51	B27	D31	

J4 - Soft Touch Pro Connections for the Upper Data Bits and Strobes:

LA Signal	Pad #	DDR Label	DDR Label	Pad #	LA Signal	
D0	A1	DQS12		B1	GND	
D1	A2	DQ52	DQ53	B2	D2	
GND	A3		DQ54	B3	D3	
D4	A4	DQ55		B4	GND	Logic Analyzer ODD Pod
D5	A5	DQS13	DQ56	B5	D6	
GND	A6		DQ57	B6	D7	
CK1+	A7	N/C		B7	GND	
GND/CK-	A8	N/C	DQ58	B8	D8	
GND	A9		DQ59	B9	D9	
D10	A10	DQS14		B10	GND	
D11	A11	DQ60	DQ61	B11	D12	
GND	A12		DQ62	B12	D13	
D14	A13	DQ63		B13	GND	
D15	A14	DQS15	DQS16	B14	D16	
GND	A15		DQS17	B15	D17	
D18	A16	CB0		B16	GND	
D19	A17	CB1	CB2	B17	D20	
GND	A18		CB3	B18	D21	Logic Analyzer EVEN Pod
D22	A19	CB4		B19	GND	
D23	A20	CB5	N/C	B20	GND/CK2-	
GND	A21		N/C	B21	CK2+	
D24	A22	CB6		B22	GND	
D25	A23	CB7	SA0	B23	D26	
GND	A24		SA1	B24	D27	
D28	A25	SA2		B25	GND	
D29	A26	SDA	WP	B26	D30	
GND	A27		FETEN	B27	D31	

Section 6: Logic Analyzer Features

6.1 TRIGGERING

When capturing DDR traffic the Agilent 16700 and 16900 logic analyzers can capture data at or above 200 MT/s, assuming proper high frequency design rules have been followed. At speeds >300Mt/s the 16753-16756 and 16950 logic analyzer modules must be set to the 600 MHz State mode(i.e. “turbo mode”). The 16750-16752 logic analyzer modules must be set to the 400 MHz State mode for speeds >200Mt/s, and the 333 MHz State mode for the 16717/18/19 for speeds >266Mt/s. In these high-speed state modes the number of available sequence levels is reduced from 16 to 6, using time tags pod count is reduced by 2 pods or 1 pod pair.

6.2 DATA DISPLAY

6.2.1 FuturePlus FS1107 and FS1125 Protocol Decode Software

If the FuturePlus FS1107 or FS1125 software is loaded, the bus transactions will be decoded and displayed. The logic analyzer contains a waveform viewer, and linear listing window to view sampled data.

If the FuturePlus FS1107 or FS1125 is not installed the listing window will display the data as HEX, Binary, Octal, or Decimal. Symbols can be created by the user refer to Section 2.4

6.3 SIGNAL THRESHOLD VOLTAGE SETTINGS

6.3.1 Threshold Considerations for Discrete Probing Network

Because of the higher data transfer rate the probe signal conditioning circuitry can be optimized for the data bus pods. This will alter the divider ration presented to the logic analyzer.

If you choose to select discrete probing circuitry described in Section 4.3, the logic analyzer user interface must be configured with a threshold setting that compensates for the 10:1 divider ratio expected by the logic analyzer.

6.3.2 Threshold Considerations for Tri-state

Each DDR bus implementation will have different timing due to trace length variation on the motherboard, variations in bus loading for each DIMM configuration, and sensitivity to dynamic factors such as crosstalk or simultaneous switching noise. Many of these timing characteristics are fixed. These differences are difficult or impossible to predict in advance for a variety of implementations and configurations of DIMMs.

Eye Finder is used to measure the fixed component of these implementation dependent timing characteristics so that the analyzer can sample all DQS* strobed signals using the single strobe DQS0 (or any DQS chosen) and achieve reliable state capture.

Stimulus dependent timing is taken into account by running the Eye Finder while worst case bus traffic occurs. The worst case data valid window boundaries are found and the analyzer is set to sample data at the center of the actual data valid window of each signal for each specific DDR implementation and DIMM configuration.

Because the strobos are tri-stated between bursts, their logic value is undefined. Some systems will terminate the DDR bus to a voltage close to the Vref voltage, causing the strobos to sit right at the switching threshold. During read bursts, because read data (and strobos) are actually not valid until the reflected wave reaches the probe, DQS0 may also spend a significant amount of time at Voh/2 (close to Vref) between arrival of the incident wave and the reflected wave. Therefore, simply comparing the DQS0 signal to Vref will result in spurious analysis clocks being generated between bursts and during read bursts.

You can vary the logic analyzer threshold to avoid false clocking. Each time you vary the threshold, run Eye Finder. This will let you to determine the optimal threshold setting for data capture and correct clocking.

All of these factors combine to add jitter to the read and write strobes. This jitter reduces the data valid window available to the logic analyzer. In some systems and DIMM configurations that have tight bus timing this may make it difficult to find an appropriate point to sample state data. This is especially true for read bursts, which usually have more complex strobe and data waveforms. Eye Finder will measure the data valid window available to the analyzer for each signal and clearly indicate which ones may have difficulty reliably sampling state data given actual DDR bus timing.

6.4 TRACING THE SERIAL PRESENCE DETECT SIGNALS

The Agilent Serial Analysis tool can be used to decode the Serial Presence Detect lines and view the SPD programming as bytes rather than as serial bits. This is best done by loading the timing config and using a slow sample rate about 4x the SPD clock rate.

6.5 CROSS BUS ANALYSIS

Real time acquisition of DDR traffic along with concurrent transactions on other system busses such as PCI-X, USB, SCSI and many others is supported. Use of an Agilent logic analyzer enables events on one bus to trigger measurements on other types of busses providing time-correlated views of all bus events. This capability is commonly referred to as cross-bus analysis. In addition, cross-triggering with global markers enables quick correlation between different buses.

FuturePlus Systems offers support for a wide variety of industry standard buses. To learn more please visit our web site at www.futureplus.com.

Section 7: Logic Analyzer Card Configurations

7.1 LOGIC ANALYZER CARD REQUIREMENTS

Probing DDR requires two to four logic analyzer cards depending on the bus speed, whether state or timing measurements are being used, and the type of logic analyzer card being used. For full channel timing measurements, only two cards (configured as a single logic analysis module using one analyzer “machine”) are necessary. For capturing simultaneous read/write data in state mode 4 logic analyzer cards are required. The preferred logic analyzer card is 16753 – 16756; these modules support Eyescan feature from Agilent technologies. The 16950 card used in the 16900 mainframe is also preferred, although the Eyescan feature has not been implemented yet.

When running at 266 MHz data rates, or when using the 16717/8/9 cards, the analyzer capturing Data bursts must be configured to run in its high-speed (Turbo) mode.

FS1107 Logic Analyzer Card Configuration Options

DDR Bus Speed	16700 Analyzer Type	Timing Analysis	State Analysis (with 2 GHz TimingZoom™)
200 MHz (PC1600) and above	16717-719 16740-742 16750-16756	2 cards configured as one module with one timing machine	4 Cards configured as 1 module
400 Mb/s (embedded)	16753/4/5/6	2 cards configured as one module with one timing machine	4 Cards configured as 1 module

Table 7-1

FS1125 Logic Analyzer Card Configuration Options

DDR Bus Speed	16900 Analyzer Type	Timing Analysis	State Analysis (with 2 GHz TimingZoom™)
200 MHz (PC1600) and above	16740-742 16750-16756 16910-911 16950	2 cards configured as one module with one timing machine	4 Cards configured as 1 module
400 Mb/s (embedded)	16753/4/5/6 16950	2 cards configured as one module with one timing machine	4 Cards configured as 1 module

Table 7-2

Section 8: Equipment Requirements for DDR Support

8.1 SUPPORTED LOGIC ANALYZER MODULES FOR DDR

The 16753-756 and 16950 logic analyzer modules are recommended for DDR applications. The frequency requirements, Eyescan feature and better setup and hold window makes the 16753 or 16950 state/timing modules necessary.

Timing analysis only requires 2 modules. State mode analysis requires a 4 module solution. If the clock recovery circuit is implemented as explained in Method 1 of section 4.4.2 then only 3 state/timing modules are required and the double probing is eliminated, however the protocol decoder will not work. Cards below the 16753 module can be used up to 400 Mt/s (except for the 16740 modules as they do not have turbo mode) in state mode, but they do not have the Eyescan feature and less setup/hold time. For slower speed applications (< =266) the 16717 cards will work fine and should provided plenty of setup/hold.

<i>Agilent Part #</i>	<i>State Speed</i>	<i>Channels</i>	<i>Memory Depth</i>
16717A	333 MHz	68	2M State
16750/1/2A	400 MHz	68	4M / 16M / 32M State
16753/4//5/6A	600 MHz	68	1M / 4M / 16M / 64M State
16950A	600 MHz	68	1M / 4M / 16M / 64M State

<i>Agilent Part #</i>	<i>Description</i>
16700B	Mainframe with no display
16701B	Expansion Frame
16702B	Mainframe with display and touch-screen
16900A	Mainframe with display and touch-screen
16902A	Mainframe with no display

8.2 TERMINATION ADAPTER NUMBERS AND ORDERING INFORMATION

<i>Agilent Part #</i>	<i>FuturePlus Part #</i>	<i>Description</i>
E5346A	FS1000	40 pin to Mictor
E5378A	FS1014	100 pin to Samtec
E5380A	FS1023	100 pin to Mictor
E5385A	FS1015	40 pin to Samtec
E5351A	none	40 pin to Mictor (requires discrete termination)
E5390A	none	100 pin to Soft Touch
E5394A	none	40 pin to Soft Touch
E5404A	none	40 pin to Soft Touch Pro
E5406A	none	100 pin to Soft Touch Pro

8.3 SUPPLEMENTAL AGILENT DOCUMENTATION

<i>Publication #</i>	<i>Description</i>
5968-4632A	Probing Solutions for Agilent Technologies Logic Analysis Systems
5968-9661E	Agilent Technologies 16700 Series Logic Analysis Systems Product Overview
5989-0422EN	Agilent Technologies 16900 Series Logic Analysis Systems Product Overview
E5404-97001	Agilent Technologies E5400-Pro Series Soft Touch Connectorless Probes

8.4 TECHNICAL SUPPORT

FuturePlus Web Site: www.futureplus.com

Agilent Technologies Web Site: www.agilent.com

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