

DisplayPort Logic Analyzer Probing Design Guide for the FS4431/36

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1.0 Introduction

The FuturePlus Systems® flexible Serial Probe is a low-cost logic analyzer Preprocessor capable of non-intrusively probing 8 channels of serial communication interfaces. Through the use of a flexible SERDES device and FPGA, it is able to receive and decode a variety of single and multi-lane protocols. The FS4431 supports Agilent Logic Analyzers and the FS4436 Supports Tektronix Logic Analyzers.

The FS4431/36 is the DisplayPort/FDI version of the product and supports serial data rates of 1.62 and 2.7 Gbps along with the probing and analysis of the Auxiliary Channel for DisplayPort and for FDI the sideband signals . Probing options for the high speed main link are mid-bus connectorless footprint (half-sized), flying leads and cable interposer. The Auxiliary Channel probing is provided by a stake pin receptacle at the end of a 3 foot cable directly attached to the FS4431/36 Preprocessor unit. The FDI sideband signals are probed in a similar manner.

1.1 DisplayPort

The FS4431/36 is designed to handle one, two or four lanes of the high speed main link for DisplayPort and one connection to the Auxiliary Channel (Aux) and one for Hot Plug Detect. The preprocessor hardware and Protocol Decode software treat the Aux and Main Link individually. For analysis of interactions between the two, the logic analyzer inter-machine triggering function is used.

1.2 FDI

For FDI there is no Auxiliary Port or Hot Plug Detect connection but there is a connection for the sideband signals. The Main Link for FDI can be one through four lanes. Two FDI Main Links can be handled by one FS4431/36 at a time.

Given the similarity between DisplayPort/FDI and PCI Express Gen 1, users are expected to be familiar with and have applied the guidelines from the Intel PCI Express™ Board Layout Guide to their design and to have performed electrical simulation to ensure proper signal quality.

1.3 Objectives

This document is intended to provide Intel with information needed for the integration of Logic Analyzer Probing for DisplayPort/FDI into their designs. Please refer to the FuturePlus Systems web site at www.FuturePlus.com for more information on the products that attach to the probing specified in this document. Although information concerning DisplayPort and FDI topology and specifications will be given, this document is not intended to take the place of other DisplayPort or FDI design documentation.

It is assumed that a design team utilizing this document for their design constraints will validate their designs through pre and post route electrical simulation and keepout volume analysis.

1.4 Nomenclature

A “channel” refers to a differential pair for a given lane. A “link” is the set of differential pairs (lane) that makes up the DisplayPort Main Link.

1.5 Revisions

January 2009 1.0 – Initial release

March 23, 2009 1.1 – Added change for low voltage FDI sideband probing, revised Aux and HPD electrical load models, clarified eye requirements for the main high speed link, removed references to Plan A probe and removed reference clock requirements.

2.0 Overview of Probing Choices

The FS4431/36 DisplayPort Preprocessor offers 3 methods of probing the high speed Main Link on the target. They are:

- Mid-Bus Connectorless Probing
- High Speed Flying Lead Set
- Cable Interposer

Auxillary Channel/Hot Plug detect and the FDI Sideband Signals are probed via stake pin headers.

2.1 SSC Support

Spread Spectrum Clocking is not supported . SSC must be turned off in order to use the DisplayPort/FDI Preprocessor on the Main Link.

2.2 Reference Clock Requirements

No reference clock is required for monitoring the Auxiliary Channel. The Reference clock for the FS4431/36 is derived from the main link by circuitry on the FS4431/36 thus no target supplied reference clock is necessary.

3.0 The Jitter Spectrum of the Main Link

In order for the FS4431/36 to achieve a low error rate for the acquired data on the DisplayPort/FDI Main Link the Jitter Spectrum for the target must be within the jitter tolerance specified in figure 5. **Users not adhering to this specification do so with the knowledge that errors may be seen on the FS4431/36 and incorrect protocol decode may result.**

4.0 Mid-Bus Connectorless Probing of the High Speed Main Link

The FS4431/36 provides support for the half size mid-bus direct probing solution. Flexibility is given to the platform designer to configure a probing solution that best meets the needs of the system. The following flexibility applies to the signals on the mid-bus footprint:

- P/N pairs reversed

The FS4431/36 supports the standard patterns of channel assignments to the pads of the PCI E Mid-Bus probe footprint. Detail concerning the exact configuration of the footprint pinout is given in this document. Additional unspecified pinout patterns may also be supported. Contact FuturePlus Systems directly for more information.

4.1 Mechanical Design of the Mid-Bus Probing Solution

This section contains mechanical design details (footprint dimensions, keepout volumes, and part numbers) of the midbus connection. The FuturePlus Systems FS1032 utilizes the Samtec “Spirit” probing technology in a half sized configuration.

4.1.1 ½ Size midbus Footprint Dimensions and Specifications

The following footprint (Fig. 1) is compatible with the FS1032 product.

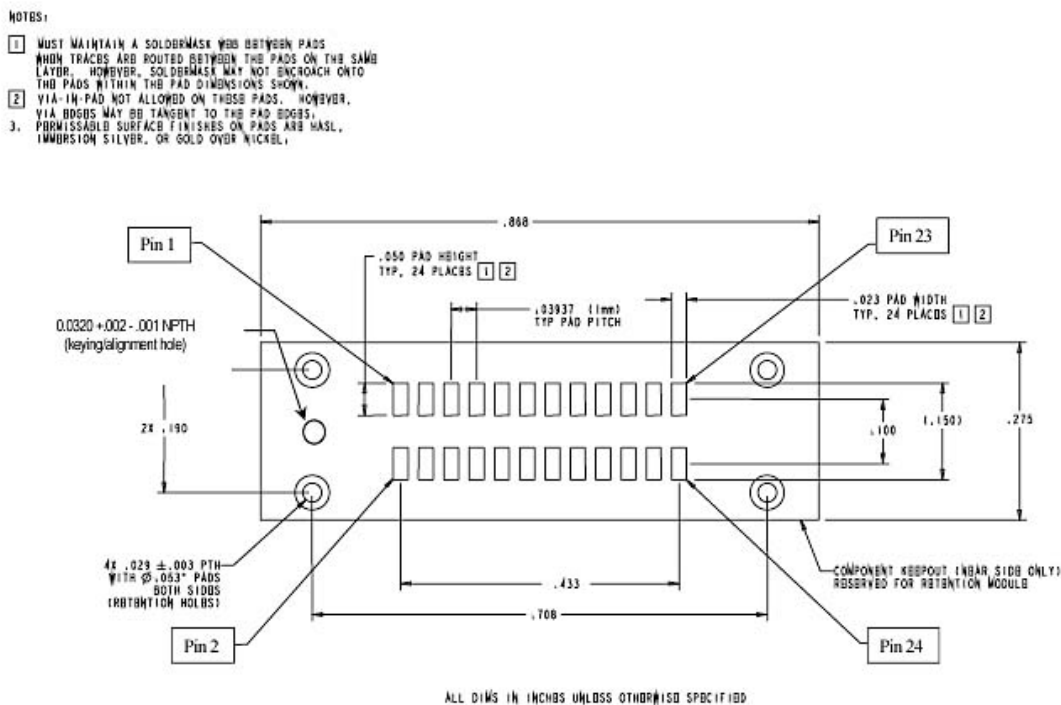


Figure 1 - PCI Express industry standard half size footprint dimensions, pin numbering, and specification

4.1.2 Keepout Volume- Half Size footprint

Keepout volume for the FS1032 half size footprint cable header is given in Figure 2.

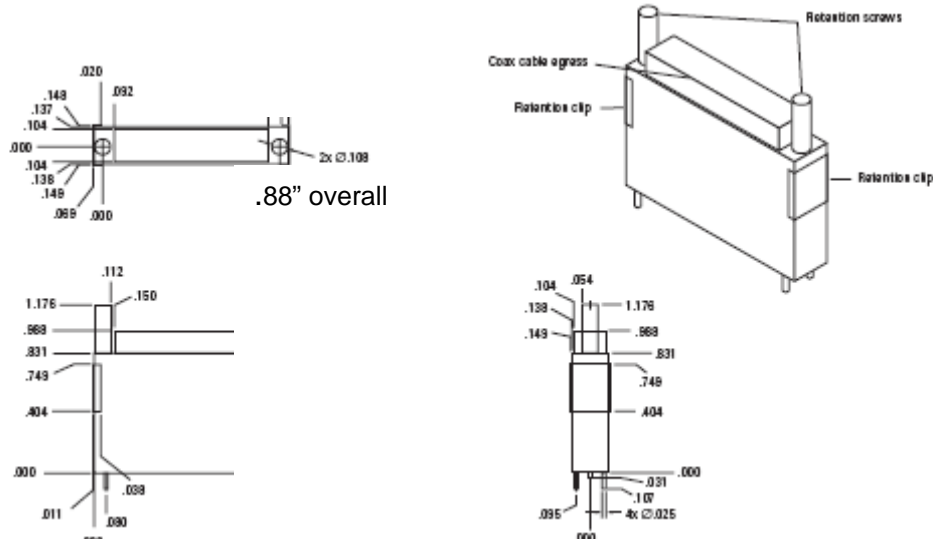


Figure 2- Half size Footprint Keepout Volume

4.2 Mid-bus Probing

Logical probing of the high speed Main Link is achieved through tapping a small amount of energy off the probed signals and channeling this energy to the Preprocessor. In order to avoid excessive loading conditions, the use of tip, or isolation, resistors is employed. These tip resistors are part of the probing interface. These relatively high impedance tip resistors enable the logic analyzer to sample bus traffic without significantly loading the probed signals. A high-level block diagram of a generic PCI Express with a logic analyzer interface is given in Figure 3. Note that this would be the same concept for the high speed Main Link.

Although the name 'mid-bus' implies a center position on the etch run, it is not meant to restrict the placement of the footprint. The footprint may be positioned anywhere on the etch run that a proper eye meeting this specification will be seen by the FS4431/36.

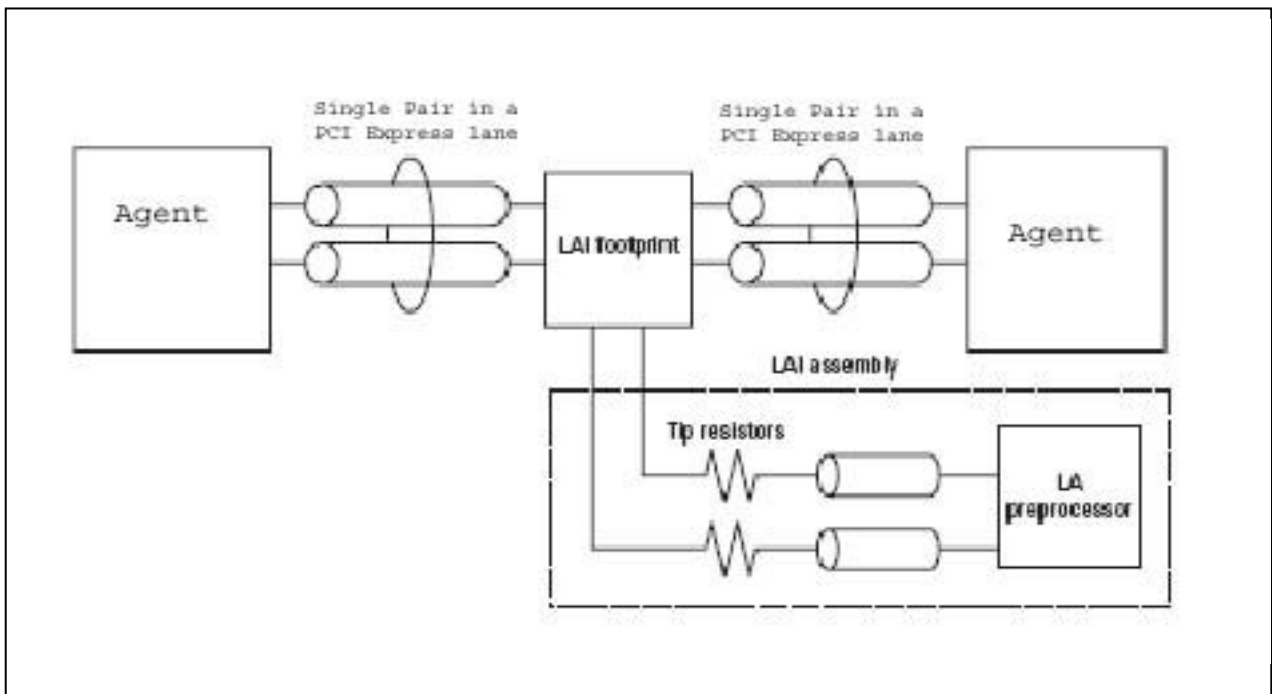


Figure 3- Block diagram example of a generic PCI Express bus with a FS1032

In order for the FS4431/36 to reliably capture logical transactions on the bus, adequate signal eye must be made available. It is incumbent upon the platform designers to ensure that sufficient signal eye is available to the footprint while the FS1032 load is in place. This must be verified via electrical simulation utilizing the load model provided in Figure 8.

4.2.1 Eye Specification

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are listed in Table 1 and described pictorially in Figure 4. The shape of the eye as seen by the FS4431/36 must closely resemble the waveshape in figure 4. **Specifically the eye opening must not show a decrease in amplitude prior to reaching the center of the unit interval.**

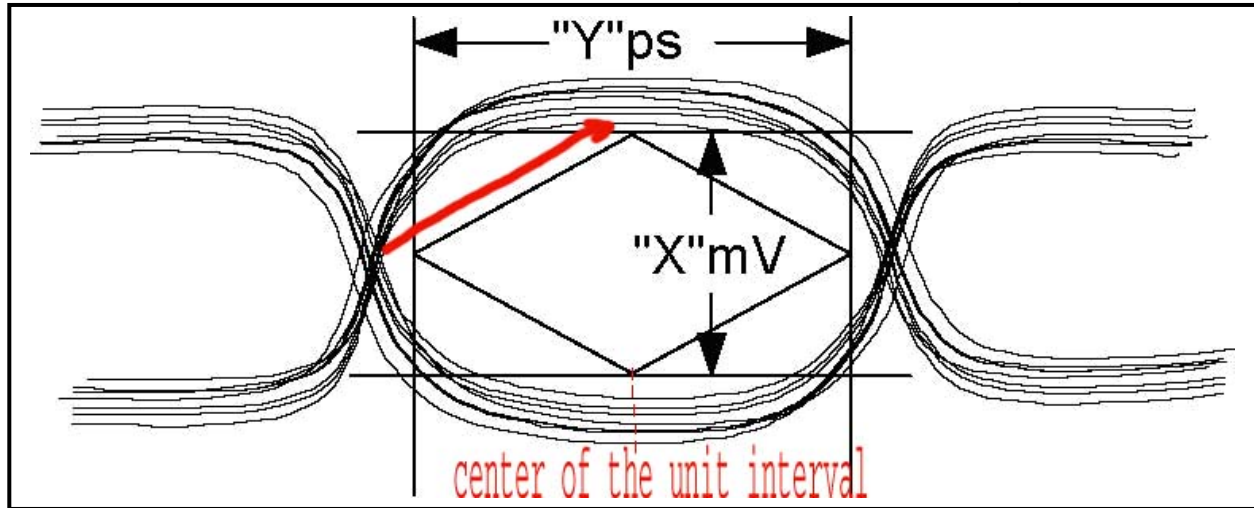


Figure 4-Example of eye specifications as seen at the footprint pad

| Description | Specification for 2.7Gbps |
|--|--|
| Min Eye height at footprint pad ¹ | 175mV Vdiff p-p |
| Min Eye Width at footprint pad | .45 UI (Jitter tolerance of 0.55UI) ³ |
| Length Matching Requirements-Differential Pair | +/-5mil ² |
| Skew tolerated between lanes of a link | 24 ns |

Table 1 details the specific eye requirements for the FS4431/36.

Note:

1. Measured in differential units, e.g. Vdiff p-p = 2x single ended swing
2. Interconnect must length match within 5 mils from midbus probe pads to the nearest discontinuities in both directions, e.g. via, capacitor, driver or receiver. Matching

within 5 mils on every segment of the PCIe trace is highly recommended. Segments are bounded by: drivers, receivers, capacitors, vias and mid bus probe pads.

3. The FS4431/36 probe can be operated at 1.2 – 2.8Gbps. Operation above 2.5Gbps requires a minimum eye width of **167ps**.

The eye characteristics given in Table 1 must be maintained for all probed links. Overall, these placement specifications limit the electrical distance between the driver pin and the footprint attach point. The same eye requirements exist for all links substrates (e.g. FR4, cables, etc.)

4.2.2 The Jitter Spectrum of the Main Link

In order for the FS4431/36 to achieve a low error rate for the acquired data on the DisplayPort/FDI Main Link the Jitter Spectrum for the target must be within the jitter tolerance specified in figure 5. **Users not adhering to this specification do so with the knowledge that errors may be seen on the FS4431/36 and incorrect protocol decode may result.**

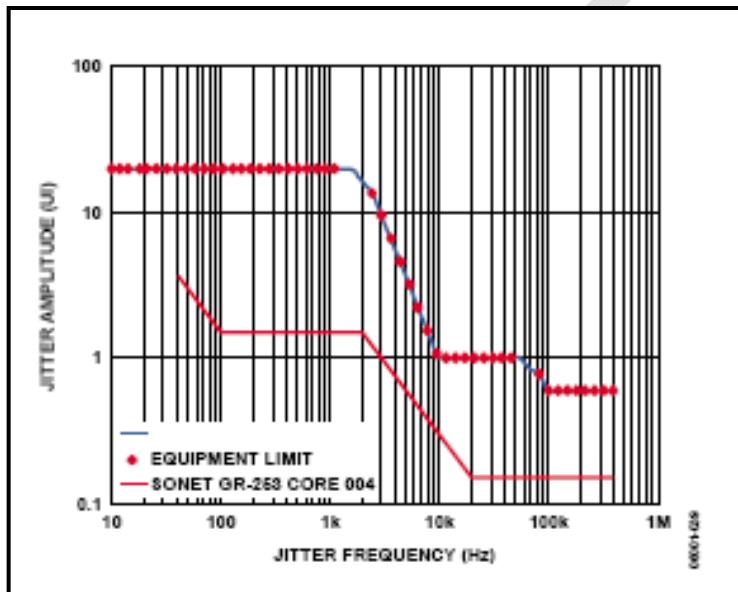


Figure 5-Jitter Tolerance Curve for the FS4431/36 Plan B Preprocessor (Equipment Limit)

4.2.3 Impact on the High Speed Main Link due to the Mid-Bus Probe Presence

The FS4431/36 should provide minimal impact on the target if the guidelines in this document are adhered to. However, FuturePlus Systems does not guarantee that the probe will not affect system operation when placed in the circuit. With the FS4431/36 installed a system may see a slight increase in BER and may activate receiver detect on unconnected links.

4.2.4 Routing Considerations Near/Through the Footprint

The following sections show examples of best practices for laying out the midbus footprint. In general the following recommendations are strongly suggested:

- no layer changes for the serial link.
- via adjacent to pad with no stringers
- 1 via and one pad per signal
- Pad in via is recommended for the footprint pad with the via filled and plated

4.2.4.1 Surface Layer Routing (on same side as the footprint)

Figure 6 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the same side of the board as the footprint.

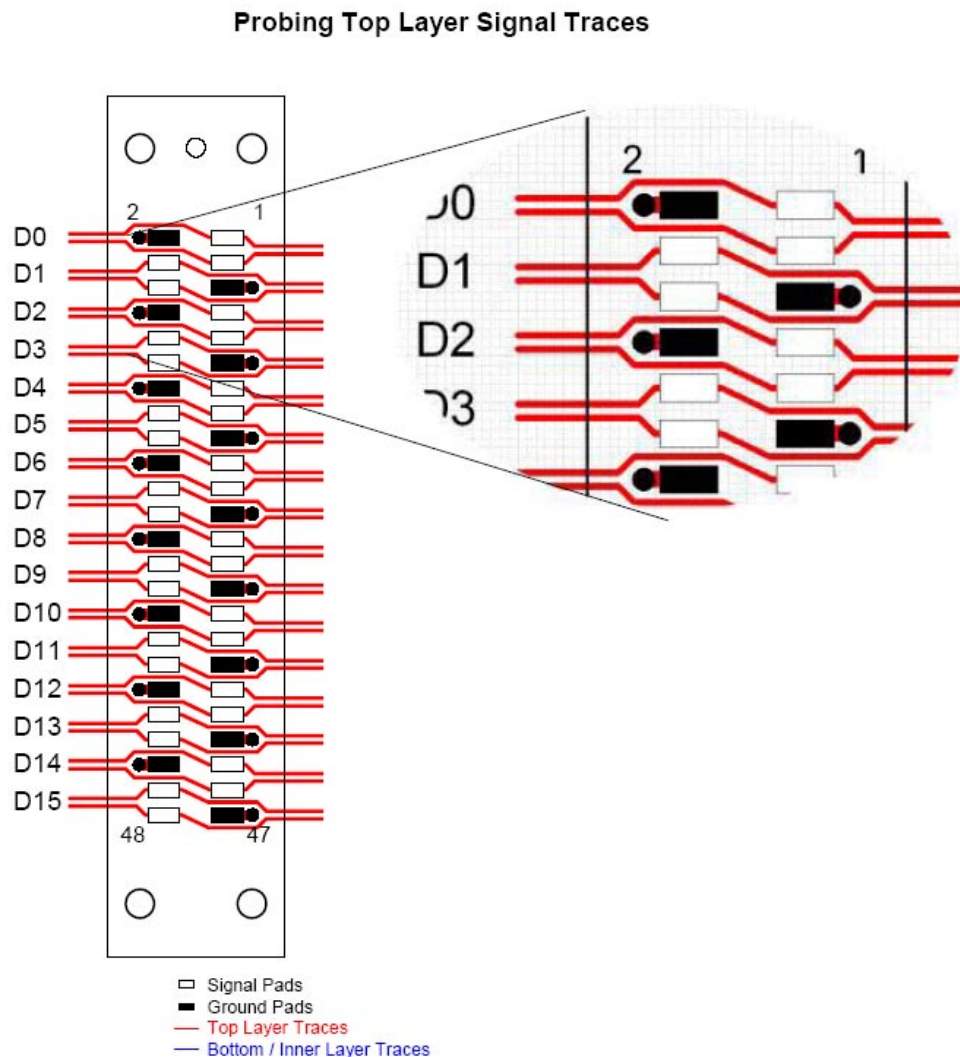


Figure 6-Suggested routing for microstrip traces on same layer as the footprint

4.2.4.2 Inner layer and secondary side routing (surface layer opposite of footprint)

Figure 7 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the opposite side of board as the footprint.

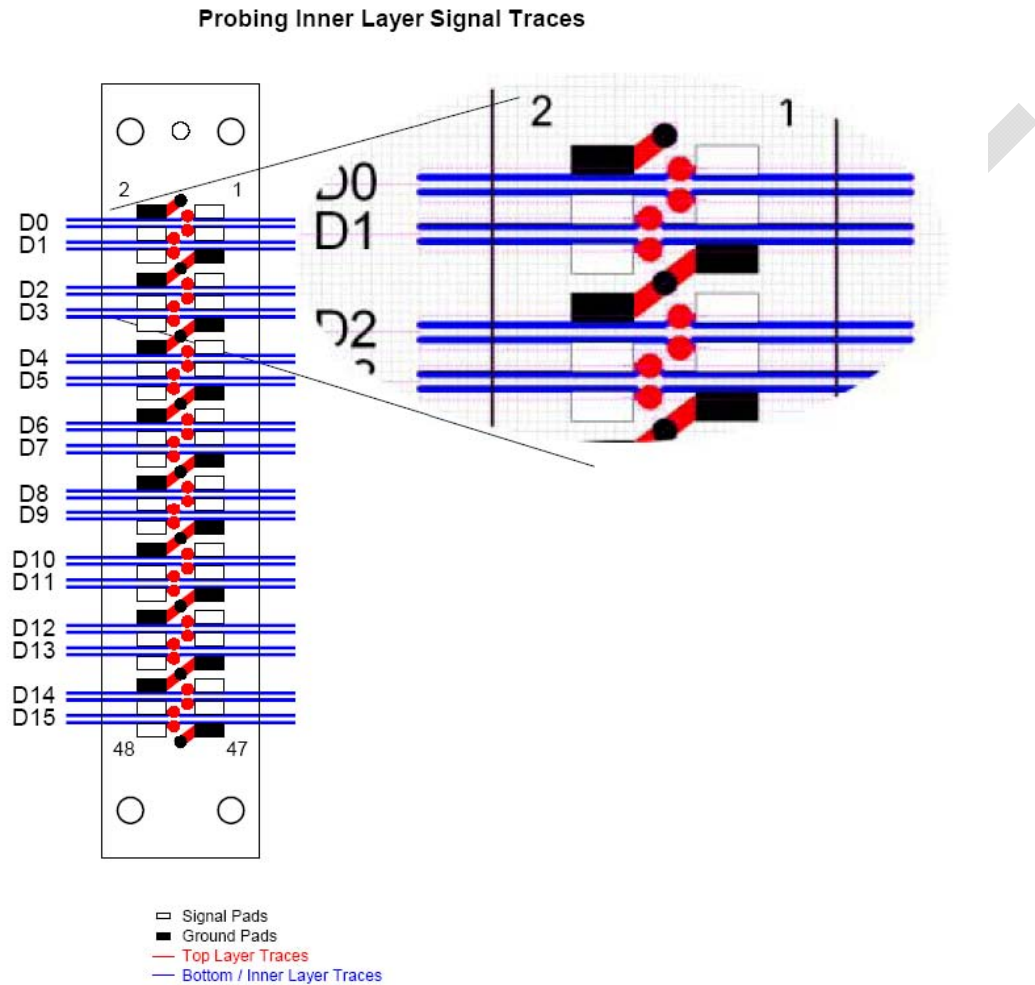


Figure 7-Suggested routing for stripline traces on inner layer and microstrip traces on surface layer opposite of footprint

4.2.5 Load Models

4.2.5.1 FS4431/36 Load Model

The load model for the FS1032 is given in Figure 8. A Touchstone file of this model is available from Samtec.

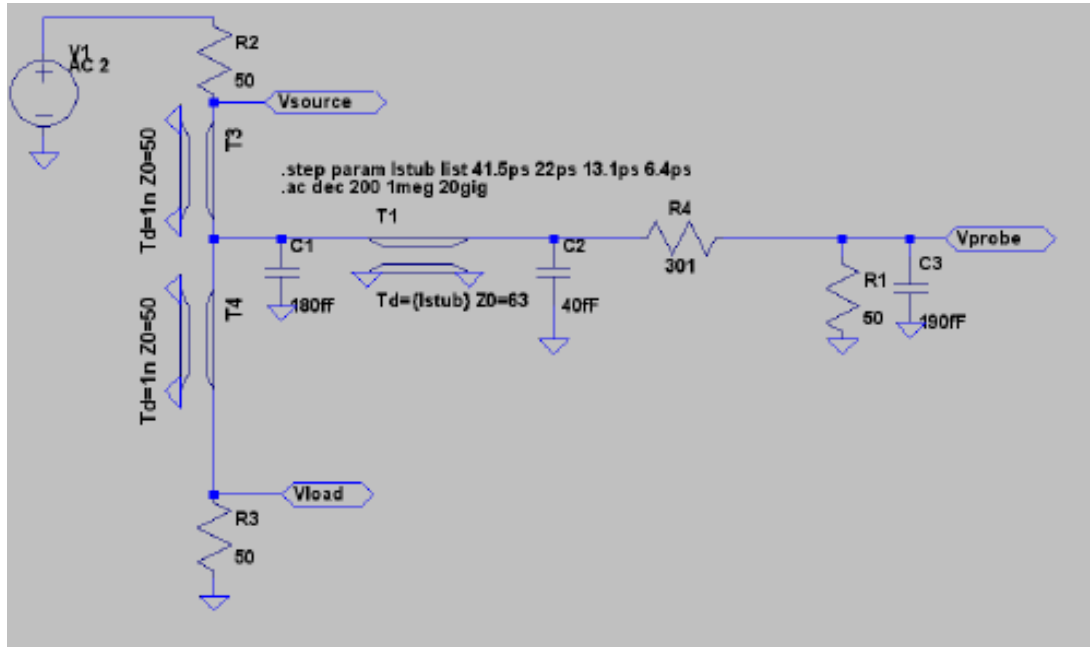


Figure 8 - Load model for the Mid-Bus cable FS1032

4.2.5.2 Load Model without FS1032 Installed

The model of the parasitic load on the system due to the midbus footprint only (i.e. no FS1032 installed) is represented simply by a 0.2pF capacitor to ground. Note that if vias are associated with tapping the link for the footprint, those via parasitics would also need to be considered here in addition to the 0.2pF pad load.

4.2.6 Mid-bus footprint Pad Assignments

The half sized mid-bus footprints is an industry standard footprint used initially for PCI Express probing. It has since been used to probe other serial architectures including Serial Rapid IO and DisplayPort.

Even though the locations of generic GND and Differential Signal pads are fixed, there is some flexibility in the assignment of specific lanes to signal pads. See the charts on the following pages for details.

Additional flexibility is provided by the probe. Some of the lane-to-pad assignment options can be varied by the user under Probe Manager control when the probe is run:

- Each lane may individually be inverted or not (p and n signals may be swapped).

The FuturePlus FS1032 serial probe head is from Samtec and it is the Spirit probe. It is a PCIe Gen1 compatible connectorless probe. It has its own retention mechanism that comes with the product. If customers require additional retention mechanisms, FuturePlus will supply them at a nominal cost. The probe head is a ½ size and is compatible with the PCIe Gen 2 ½ size footprint as well as the PCIe Gen1 ½ size

footprint. The probe head will not make a connection to the extra PCIE Gen2 ground signals.

Table 2 shows the generic location of probe points in the half sized footprint.

Channel= either direction A OR direction B differential pair for a given lane. C<letter>= the designator for a Channel which accepts a given differential pair of signals
 C<letter><p or n>= the two signals of the differential pair.

If interested in any arrangement not specified on the following pages, please contact FuturePlus Systems directly for possible support.

Table 2- General 8 Channel PCI Express Pinout

| Pin # | Signal Name | Pin # | Signal Name |
|-------|------------------|-------|------------------|
| 2 | GND | 1 | C _A p |
| 4 | C _B p | 3 | C _A n |
| 6 | C _B n | 5 | GND |
| 8 | GND | 7 | C _C p |
| 10 | C _D p | 9 | C _C n |
| 12 | C _D n | 11 | GND |
| 14 | GND | 13 | C _E p |
| 16 | C _F p | 15 | C _E n |
| 18 | C _F n | 17 | GND |
| 20 | GND | 19 | C _G p |
| 22 | C _H p | 21 | C _G n |
| 24 | C _H n | 23 | GND |

1,2

Table 3- x4 High Speed Main Link Pinout

| Pin # | Signal Name | Pin # | Signal Name |
|-------|------------------|-------|------------------|
| 2 | GND | 1 | C0p- Main Link A |
| 4 | C0p- Main Link B | 3 | C0n- Main Link A |
| 6 | C0n- Main Link B | 5 | GND |
| 8 | GND | 7 | C1p- Main Link A |
| 10 | C1p- Main Link B | 9 | C1n- Main Link A |
| 12 | C1n- Main Link B | 11 | GND |
| 14 | GND | 13 | C2p- Main Link A |
| 16 | C2p- Main Link B | 15 | C2n- Main Link A |
| 18 | C2n- Main Link B | 17 | GND |
| 20 | GND | 19 | C3p- Main Link A |
| 22 | C3p- Main Link B | 21 | C3n- Main Link A |
| 24 | C3n- Main Link B | 23 | GND |

Notes:

1. DisplayPort: A or B but not both simultaneously. FDI: may use A and B simultaneously.
2. Polarity (p and n) of any differential pair may be swapped

Table 4 – x3 High Speed Main Link Pinout^{1,2,3}

| Pin # | Signal Name | Pin # | Signal Name |
|-------|------------------|-------|------------------|
| 2 | GND | 1 | C0p- Main Link A |
| 4 | C0p- Main Link B | 3 | C0n- Main Link A |
| 6 | C0n- Main Link B | 5 | GND |
| 8 | GND | 1 | C1p- Main Link A |
| 10 | C1p- Main Link B | 3 | C1n- Main Link A |
| 12 | C1n- Main Link B | 5 | GND |
| 14 | GND | 1 | C2p- Main Link A |
| 16 | C2p- Main Link B | 3 | C2n- Main Link A |
| 18 | C2n- Main Link B | 5 | GND |
| 20 | GND | 1 | NC |
| 22 | NC | 3 | NC |
| 24 | NC | 5 | GND |

Notes:

1. DisplayPort: A or B but not both simultaneously. FDI: may use A and B simultaneously.
2. Polarity (p and n) of any differential pair may be swapped
3. All pads for the unselected pins on the footprint must be present and will be connected to the inputs of the FS1032. All grounds will be present.

Table 5- x2 High Speed Main Link Pinout^{1,2,3}

| Pin # | Signal Name | Pin # | Signal Name |
|-------|------------------|-------|------------------|
| 2 | GND | 1 | C0p- Main Link A |
| 4 | C0p- Main Link B | 3 | C0n- Main Link A |
| 6 | C0n- Main Link B | 5 | GND |
| 8 | GND | 7 | C1p- Main Link A |
| 10 | C1p- Main Link B | 9 | C1n- Main Link A |
| 12 | C1n- Main Link B | 11 | GND |
| 14 | GND | 1 | NC |
| 16 | NC | 3 | NC |
| 18 | NC | 5 | GND |
| 20 | GND | 7 | NC |
| 22 | NC | 9 | NC |
| 24 | NC | 11 | GND |

Notes:

1. DisplayPort: A or B but not both simultaneously. FDI: may use A and B simultaneously.
2. Polarity (p and n) of any differential pair may be swapped

- All pads for the unselected pins on the footprint must be present and will be connected to the inputs of the FS1032. All grounds will be present.

Table 6 - x1 High Speed Main Link Pinout^{1,2,3}

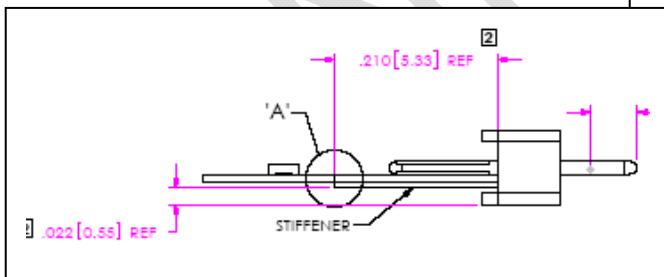
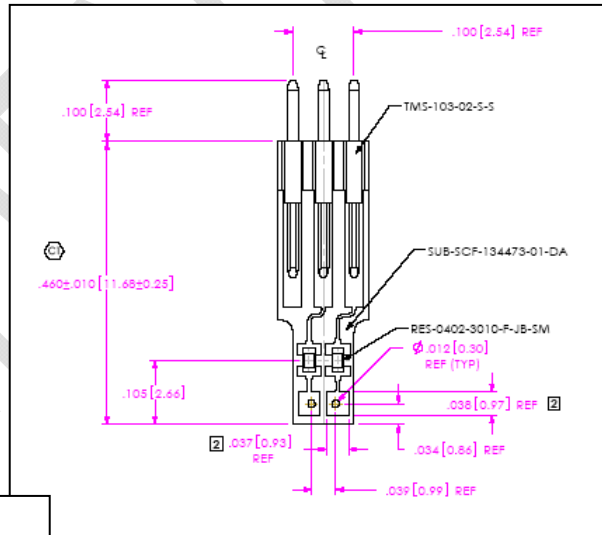
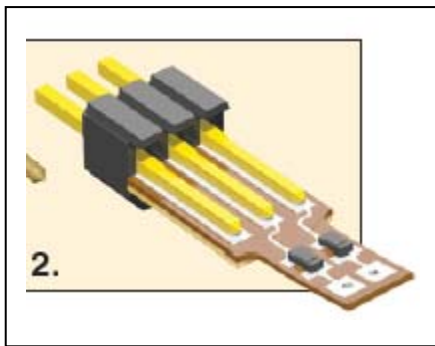
| Pin # | Signal Name | Pin # | Signal Name |
|-------|------------------|-------|------------------|
| 2 | GND | 1 | C0p- Main Link A |
| 4 | C0p- Main Link B | 3 | C0n- Main Link A |
| 6 | C0n- Main Link B | 5 | GND |
| 8 | GND | 1 | NC |
| 10 | NC | 3 | NC |
| 12 | NC | 5 | GND |
| 14 | GND | 1 | NC |
| 16 | NC | 3 | NC |
| 18 | NC | 5 | GND |
| 20 | GND | 1 | NC |
| 22 | NC | 3 | NC |
| 24 | NC | 5 | GND |

Notes:

- DisplayPort: A or B but not both simultaneously. FDI: may use A and B simultaneously.
- Polarity (p and n) of any differential pair may be swapped
- All pads for the unselected pins on the footprint must be present and will be connected to the inputs of the FS1032. All grounds will be present.

5.0 Probing the High Speed Main Link with the FS1036 Flying Lead Set

The FuturePlus FS1036 high speed flying lead probe can be connected anywhere on the target that the user feels an adequate eye can be obtained. The FS1036 was designed to be used right at the AC coupling capacitors incorporated into the DisplayPort Main Link traces. In some Intel implementations 0 ohm resistors were placed in the FDI link to facilitate the connection of the FS1036. **It is imperative that any pads inserted into the FDI link be simulated and that the same electrical recommendations for the footprint be followed.** The FS1036 flying lead cable assembly allows the FS4431/36 preprocessor to connect to components on the target board by means of directly soldering a flex pcb to a component or feature on the target pcb, then connecting the header on the flying lead cable to the other end of the flex pcb. The specification for the eye necessary for the FS4431/36 to capture using the FS1036 is contained in section 4.2 table 1.



FS1036 is for use on the Main Link not the Aux Channel or Hot Plug Detect

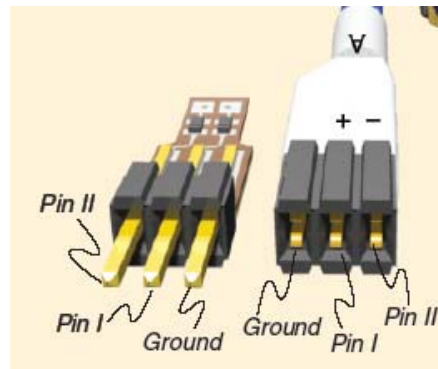


Figure 9-Mechanical details for the FS1036

A few general guidelines about the use of the flying lead cable

1. There is an instruction booklet with the FS1036 cable that provides detail on how to solder the flex pcb to your board. Refer to this document.
2. Polarity matters. Make sure you know how the + and – sides of the signal are connected. Adjustment to polarity can be made in the Probe manager.
3. The ground of the FS1036 is not connected to the target but to the shield of the cable and to the ground of the Preprocessor.

The FS1036 flying lead cable has 8 pairs of channel connectors which are labeled A-C-E-G for up to 4 channels of a link and B-D-F-H which can be used for another link. For DisplayPort only one set of these 4 can be connected at any one time. **Channel A (or B) must be connected to lane 0.**

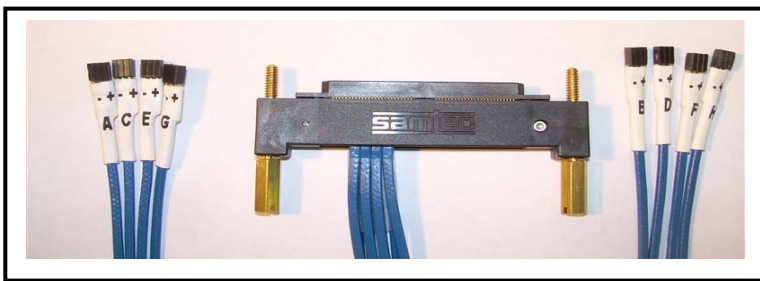


Figure 10- The high speed flying lead set FS1036

Users should simulate their system to ensure that the FS1036 will not interfere with the target and the appropriate eye will be presented at the probe tip. The below model can be used for this simulation

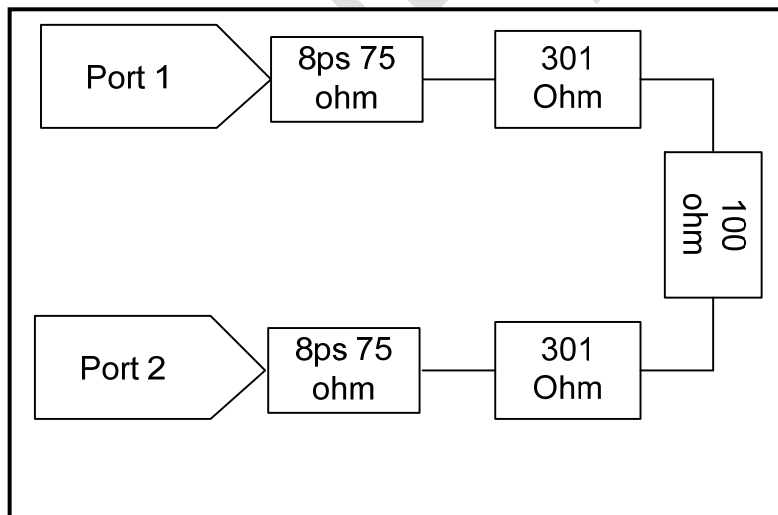


Figure 11-Load model for the high speed flying lead set FS1036

6.0 Probing the Aux Channel and Hot Detect Plug (HPD)

The Aux channel and HPD are probed using a standard stake pin connection. There are two cables from the FS4431/36 box for this purpose. The grounds on these cables are tied to the shield of the cable.

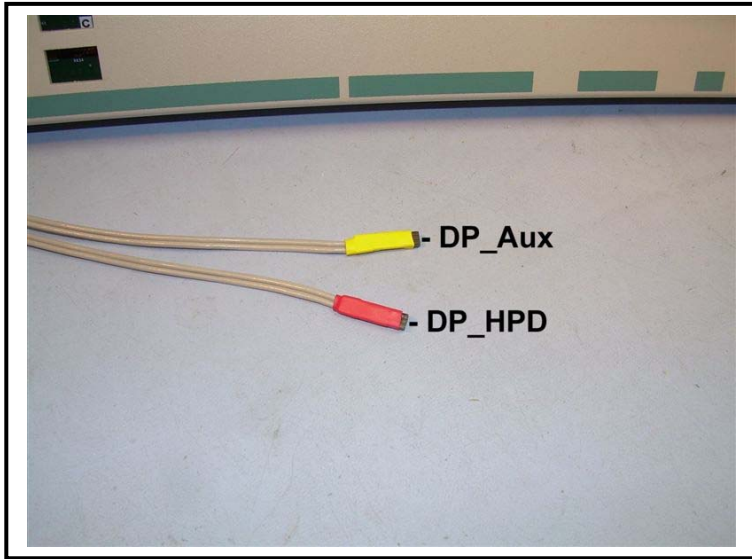


Figure 12- Photo of the Aux Channel and Hotplug Detect connections

The KOV for these cable headers is shown below. The mating 3 pin header is part number:

Through-hole: Samtec TMS-103-02-S-S Surface mount: Samtec FTR-103-02-S-S .

The pinout for the mating 3 pin header is shown in tables 7 and 8.

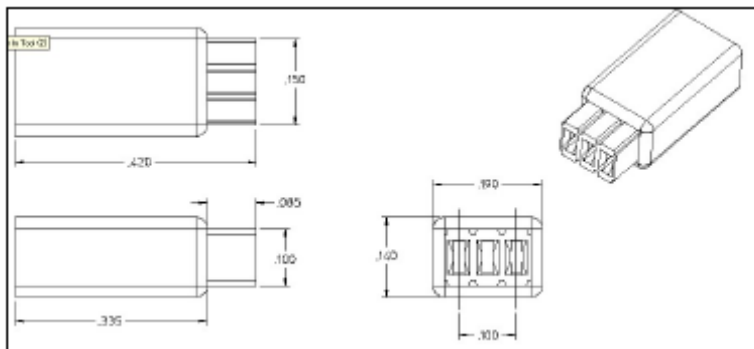


Figure 13- KOV for the Aux Channel and HPD cable headers

Table 7 – DisplayPort Auxiliary Channel – MUST be plugged in correct orientation

| Pin 1 | Pin 2 | Pin 3 |
|----------|-------|----------|
| DP_AUX_P | NC | DP_AUX_N |

Table 8 – DisplayPort Hot Plug Detect

| Pin 1 | Pin 2 | Pin 3 |
|--------|-------|-------|
| DP_HPD | GND | NC |

6.1 Electrical Load Model

These signals are a probed with a 1K ohm resistor in series with 4' of 26 gauge cable. For Aux the cable is then connected to a MC100EP16VADT and for HPD the cable is connected to a SN74AVC1T45. There are no eye requirements for these signals since they are not high speed. The FS4431/36 requires a monotonic waveform that is clean with no shoulders or glitches.

7.0 Probing the FDI Sideband Signals

The FDI sideband signals are low voltage signals and not used by the FS4431/36 for protocol disassembly. If the user wishes to probe the signals FuturePlus recommends the P6960 with the P6960 01 flying lead adapter if using Tektronix logic analyzers and the E5382A single-ended flying lead set if using Agilent logic analyzers.

8.0 Probing with the FS1040 Cable Interposer

The FS1040 is a DisplayPort cable interposer that allows for probing of the DisplayPort bus between the motherboard and the monitor. One end of the interposer has a short cable with a DisplayPort connector that will mate with the motherboard. The other end of the FS1040 will have a DisplayPort connector that mates with the display device (monitor). The body of the FS1040 will be pcb that allows the probing of the high speed Main Link, Aux Channel and HPD. Aux Channel and HPD will have the 3 pin header stake pins described in this document. These will mate with the two cables from the FS4431/36. The high speed Main Link will be tapped and go to a soldered on cable. The other end of the cable will go to the FS4431/36 instrument end header. Thus no additional cable purchase will be required when using the FS1040 in order to probe the DisplayPort bus.

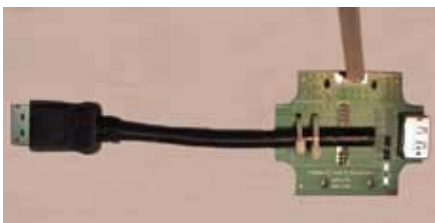


Figure 14- FS1040 DisplayPort Cable Interposer