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## Moving up to DDR2 at printed circuit board layout

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Designing faster processors is the order of the day in the computing industry. However, processor speeds continue to exceed memory latency improvements. Although [CPU](#) speeds double every eighteen months, memory speed takes about ten years to double. This has given rise to the term "memory wall" to describe how overall system performance is bottlenecked by memory latency. Because of this, next-generation systems call for newer memory architectures able to withstand increasing demands of [bandwidth](#) and speed.

DDR2 is an evolutionary improvement over its predecessor, DDR, and is the next memory standard, as defined by JEDEC (Joint Electronic Device Engineering Council) document JESD79-D. To design a successful DDR2 interface to SDRAMs (synchronous DRAMs), the skew between data and strobe, power supply jitter, crosstalk, reflections, attenuation and other considerations must be balanced. If certain design rules are not followed, the consequences may affect the interface's functionality. This article explains how a DDR2 system works and describes from a designer's point of view the correct way to implement it on a pc board.

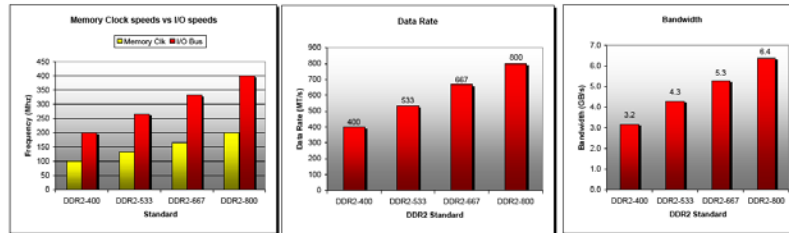
DDR2 is similar to DDR in that it is also a source synchronous interface; the clock is sourced by the same device that generates data signals. It also uses the same process to read and write data on the clock signal's rising and falling edges. But DDR2 can process 4 bits of information per [clock](#) cycle, in comparison to DDR's 2 bits. DDR2 also includes other improvements over its parent that help create a more efficient memory [architecture](#) in the areas of data transfer power-saving: in particular, on-die terminations (ODTs), additive latency and power consumption.

ODT is built into the DDR2 [chip](#) module. A termination resistor is placed on the module to eliminate the need for any termination on the motherboard. This helps move data signals to and from the DRAM without injecting excessive noise. What's more, a DDR2 memory interface provides additional latency by delaying a read command internally before being executed. This eliminates the occurrence of data collisions and provides a more reliable memory interface. Last, DDR2 operates at a lower voltage (1.8 V versus DDR's 2.5 V) and thus runs cooler.

A typical DDR2 interface comprises a memory interface [controller](#) (MIC), DRAMs and a [buffer](#) chip that redistributes clock and address to the DRAMs. The DDR2 memory [bus](#) is comprised of signals divided into data, address and command, control and clock groups.

The data group is composed of bidirectional data bits (DQ). Each DQ group shares the same strobe signal (DQS) and a data mask [bit](#) (DM). This group is referred to as a [byte](#) lane. During a write operation, DQS is sourced by the MIC. During the read operation, DRAM sources DQS. Data is sampled on both the rising and falling edges.

DDR2-STANDARD	MODULE	MEMORY CLK(MHz)	I/O BUS (MHz)	DATA RATE (MT/s)	BANDWIDTH (GB/s)
DDR2-400	PC2-3200	100	200	400	3.2
DDR2-533	PC2-4300	133	266	533	4.3
DDR2-667	PC2-5300	166	333	667	5.3
DDR2-800	PC2-6400	200	400	800	6.4



DDR2 Specifications for the 4 standards.

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Address and command signals are unidirectional and always sourced by the MIC. They run at half the frequency of the I/O bus when using 2T clocking (a 2-cycle command delay before the MIC can start sending signals to the memory bank), or the same frequency as that of the I/O bus (when using 1T).

The control group includes chip select (CS), clock enable (CKE) and ODT signals. This group runs at 1T clocking. ODT signals are used to enable or disable ODT. Clock signals (CK) are usually sourced by the MIC and sample the data (address and control) only on the rising edge.

### Layout guidelines

A DDR2 subsystem requires clean reference signals, reduced setup and hold times and length matching to reduce signal skew effects. The layout should be done using controlled impedance traces of  $Z_0 = 50$  ohms. For proper optimization of DDR2 interface, the following routing sequence of the different DDR groups is recommended: data, Address/command, control and clock

It is highly preferable to route the data group first, for it constitutes the largest portion of the memory bus. Moreover, it operates at twice the clock speed of other groups, and its signal integrity is of most concern.

In a typical DDR2 system, data is captured by the MIC (using the DQS rather than the clock) on both the rising and falling edges of the strobe. Each 8-bit datum (DQ0 to DQ7) has an associated strobe and mask. It is crucial that this "byte lane" be matched in length with the lowest tolerance achievable. Ideally, but less importantly, all byte lanes should be length-matched to each other. It is also important that the board designer provide these signals with a solid reference plane to control the characteristic impedance and provide a smaller loop area between the signals and the return currents. Preferably, no vias should be used on these signals, avoiding additional capacitive loading.

Crosstalk is another major concern in a DDR2 layout, where signals of different frequencies are routed in close proximity to each other. It is thus imperative that board designers keep the data group away from all other groups by at least five times the trace width. It is also important to keep a 3x clearance between traces within each byte lane.

Conductor and dielectric losses are one of the top contributors to jitter in the DDR2 interface. Conductor losses are caused by the "skin effect," or the tendency of electrons to flow on the surface of the conductors, away from the center, at higher frequencies. This effect increases with signal frequency. Skin effect can be reduced by increasing the trace widths of the conductors, but the trace width nevertheless must be maintained to a certain value to achieve the controlled impedance.

Dielectric losses result from molecular vibrations of the dielectric near the conductors carrying electrons. This causes some of the energy of the electrons to be absorbed by the dielectric, producing attenuation. This effect is also a function of signal frequency. Dielectric losses can be reduced by using certain advanced materials with lower loss tangents (or the dissipation factor). Mindful of the timing budget, board designers must balance the cost/performance relationship by application.

On a DDR2 memory bus, the address/command group is sourced by the MIC and captured at the DRAM using the memory clocks. Usually, termination resistors are used for these signals and placed behind the last DIMM slot. Their value depends on bus topology.

From a layout perspective, it is important to provide a power/ground reference to these signals to get a solid return path. It is also important to keep these signals away from the data group, avoiding crosstalk. Because the address/command group is captured by the memory clock, they must also maintain a length relationship with the clock signals, depending upon the application.

Most notable of the control signals are the ODTs, which enable and disable the on-die termination on the data group. DDR2 does not require the use of serial or parallel termination on the data lines, unlike DDR. Rather, DDR2 has this termination built in by using ODT. Like the address/command group, these signals also require a termination resistor placed after the last DIMM slot.

Other similarities to the address/command group include the need for a solid reference plane, clearance requirements with the data lines and maintenance of a length relationship with the memory clock. One thing different about the control group is that it is routed point to point, unlike other signal groups, which are daisy-chained.

Meanwhile, DDR2 features differential clock inputs (CK and CK#) to diminish variations in the duty cycle of the clocks. Because the clocks are used to capture command and address data, they must maintain the length relationship to the address/command group. Moreover, during a write cycle, the MIC must satisfy the timing specs between DQS and CK to facilitate the reliable transfer of data. As a result, two main concerns exist when connecting the clocks from the MIC to the DIMM: clock timing and differential impedance.

Board designers should ensure that clock lines are routed differentially and correct trace widths/clearances maintained to achieve the target differential impedance of 70 ohms. Routing the signals differentially also reduces the flight time of the clocks when compared to the single ended signals.

Because of this, most DDR2 design guides recommend that clock signals be routed at the same length or longer than the address, control and command signals to compensate for this timing variation. To satisfy the clock to strobe (DQS) relationship, it is preferable that all clocks be between the shortest and longest strobe lengths. It is also recommended that all clock signals are length-matched to each other within a tolerance of 25 mils.

### **Power system**

A DDR2 power system requires three supplies: VDD, VREF and VTT.

VDD is the main 1.8-V supply for the MIC and DRAM. Board designers, much like other designers of high-speed technology, should provide a low impedance power system on the board while meeting every device's switching needs, something that requires both judicious layout of the decoupling capacitors near the device power pins and the creation of robust planes to provide solid references to all signals.

VREF is used as a reference voltage by the differential receivers in the DRAM and the MIC. This is done to discriminate between the logic high and low levels at the receiver input. The value is half of VDD (0.9 V). Again, the placement of the decoupling capacitor near the regulator, DRAM and MIC is very important. Any degradation of the VREF input voltage will affect the setup and hold times of the DDR2 device.

VTT is the termination supply of the bus that is required at the midpoint voltage. Its value must be within an 80-mV range of VREF. From a layout perspective, the VTT generators must be placed close to the termination resistors to provide a low impedance path (VTT and VREF must be able to track any variations in VDD).

As manufacturers rapidly progress toward faster and faster processors, the need for low-latency memories will continue to rise, and new architectures will from time to time be introduced, ensuring that incorporating these new interfaces into new designs will become increasingly difficult for board designers. Problems such as power supply jitter, reflections and crosstalk will continue to plague memory structures. DDR2 is still relatively new in the industry, and it will be around for awhile. It behooves layout designers to completely comprehend the interface before doing layout so that the boards they design will be "right the first time."



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